

that performs the PCM encoding and decoding is called a *codec* (coder/decoder). The codec is explained in detail in Chapter 17.

Sample-and-Hold Circuit

The purpose of the sample-and-hold circuit is to sample periodically the continually changing analog input signal and convert the sample to a series of constant-amplitude PAM levels. For the ADC to accurately convert a signal to a digital code, the signal must be relatively constant. If not, before the ADC can complete the conversion, the input would change. Therefore, the ADC would continually be attempting to follow the analog changes and never stabilize on any PCM code.

Figure 16-3 shows the schematic diagram of a sample-and-hold circuit. The FET acts like a simple switch. When turned "on," it provides a low-impedance path to deposit the analog sample across capacitor C1. The time that Q1 is "on" is called the *aperture* or *acquisition time*. Essentially, C1 is the hold circuit. When Q1 is "off," the capacitor does not have a complete path to discharge through and therefore stores the sampled voltage. The *storage time* of the capacitor is also called the *A/D conversion time* because it is during this time that the ADC converts the sample voltage to a digital code. The acquisition time should be very short. This assures that a minimum change occurs in the analog signal while it is being deposited across C1. If the input to the ADC is changing while it is performing the conversion, distortion results. This distortion is called *aperture distortion*. Thus, by having a short aperture time and keeping the input to the ADC relatively constant, the sample-and-hold circuit reduces aperture distortion. If the analog signal is sampled for a short period of time and the sample voltage is held at a constant amplitude during the A/D conversion time, this is called *flat-top sampling*. If the sample time is made longer and the analog-to-digital conversion takes place with a changing analog signal, this is called *natural sampling*. Natural sampling introduces more aperture distortion than flat-top sampling and requires a faster A/D converter.

Figure 16-4 shows the input analog signal, the sampling pulse, and the waveform developed across C1. It is important that the output impedance of voltage follower Z1

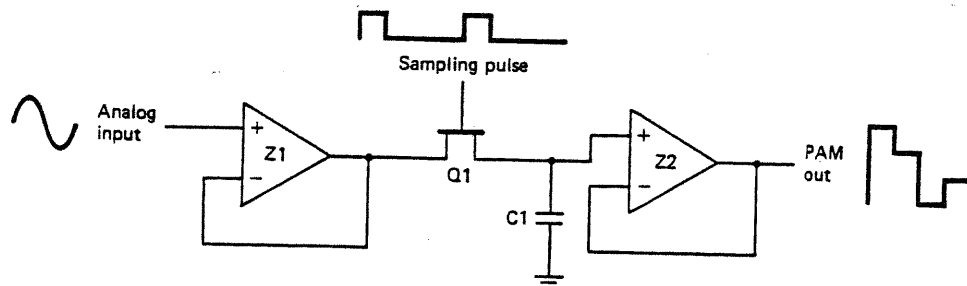


FIGURE 16-3 Sample-and-hold circuit.

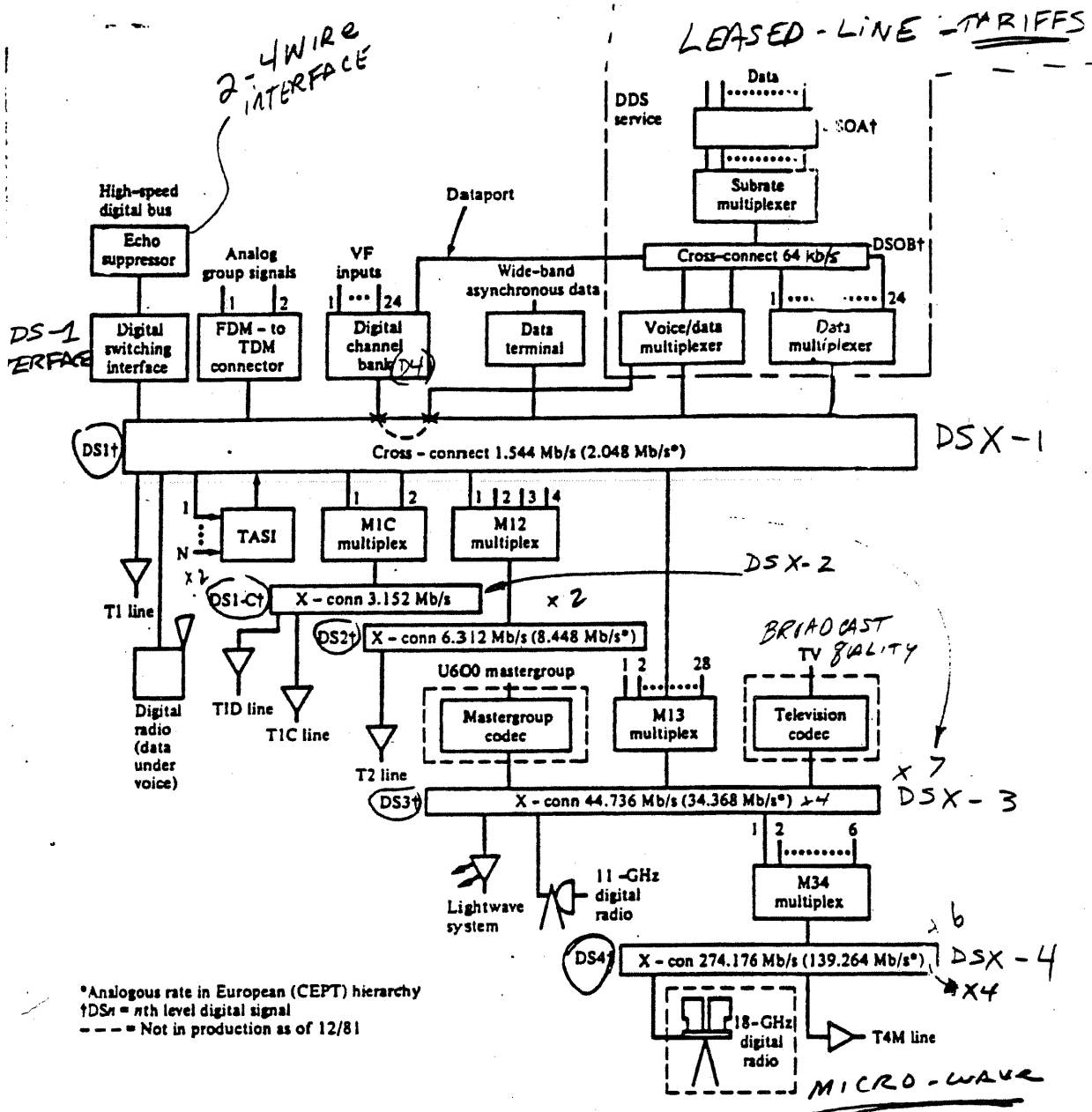


FIGURE 6.11. AT&T TDM hierarchy.

capacity transmission for today's long-haul telecommunications system. Each facility is given a designation that indicates the capacity provided. Thus the *T1 carrier* provides a 1.544-Mbps service, using the DS-1 transmission format. The column labeled transmission denotes whether an analog or digital transmission service is provided. As was mentioned in Chapter 2, analog service implies analog signaling, but a digital transmission service can be provided with either analog or digital service. For example, the T4 service uses digital signaling over coaxial cable, but the FT3 and 11-GHz digital services use analog signaling.

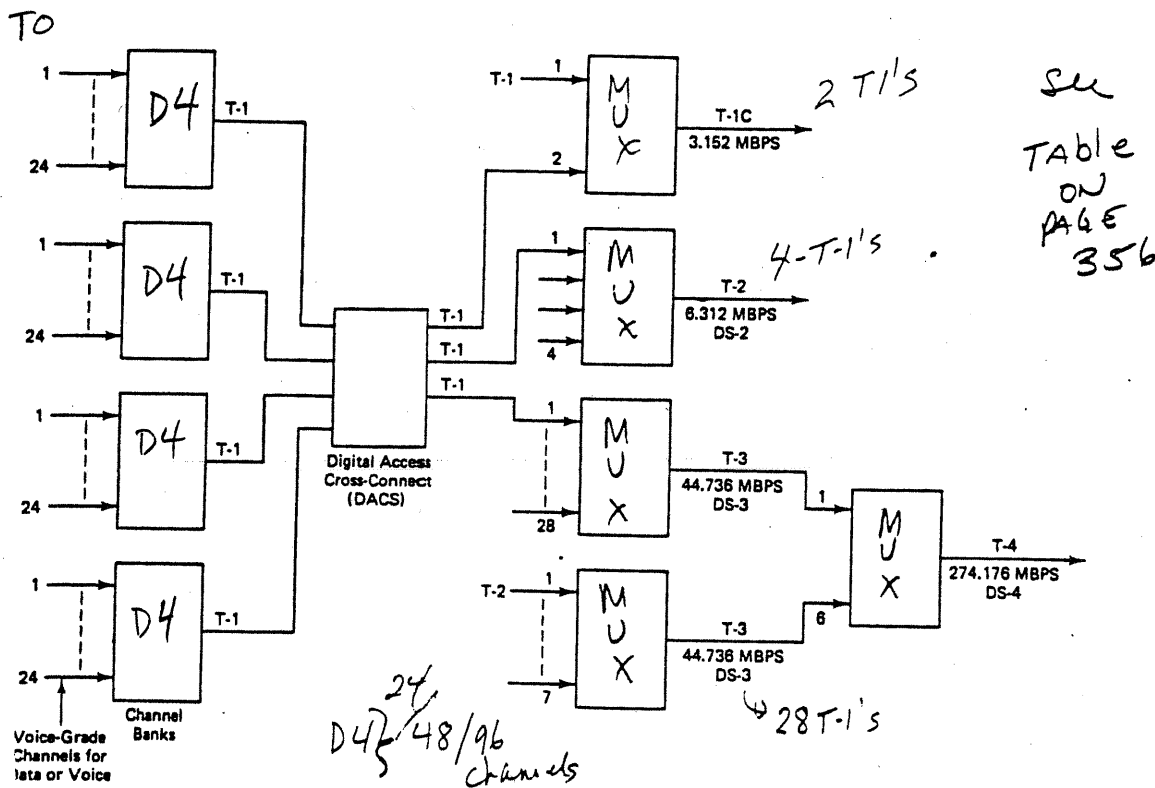


FIGURE 16-2
Digital Hierarchy

There is another upgrade that AT&T is beginning to incorporate into the network today, called the *extended superframe* (ESF), which is also based on DS-1 requirements, but the 193rd bit is used differently. ESF was originally proposed in 1979 to find line problems while the circuit was still in service. A detailed description of this operation will be incorporated into Section E of this chapter.

It is anticipated that continuing upgrades will be made in the network, especially as the need for ISDN services grows. It is also quite possible that these upgrades may mean substantial replacements of existing equipment. The changes may not be readily incorporated due to the investment involved in existing equipment. Therefore, the potential network user must constantly be aware of the status of circuits being interfaced because different levels or capabilities of service may be available at different locations, and they may not be compatible with each other in terms of their capabilities. What this means is that all of the features available at one end may not be available at the other end of the circuit, and therefore you may not be able to take full advantage of the capabilities being offered.

to be intermixed with other T-3 channels. Another use for a DACS will be for routing around circuit breaks.

Multiplexers

The multiplexers actually do just that. If you refer back to Fig. 16-2 you will see the digital hierarchy in which the various multiplexers are described with each of their capacities. For convenience they are listed here in tabular form.

CIRCUIT DESIGNATION	DIGITAL SIGNAL DESIGNATION	DATA RATE	EQUIVALENT VOICE CHANNELS
T-0		64 KBPS	1
T-1	DS-1	1.544 MBPS	24—PCM/48 ADPCM*
T-1C	DS-1C	3.152 MBPS	48
T-2	DS-2	6.312 MBPS	96
T-3	DS-3	44.736 MBPS	672
T-4	DS-4	274.176 MBPS	4032

*PCM: Pulse Code Modulation; requires 64 KBPS for digitized voice

ADPCM: Adaptive Differential Pulse Code Modulation; requires 32 KBPS for digitized voice

There is another set of multiplexers for digital transmission that can be utilized by the end user. The first one is a standard point-to-point multiplexer that supports a single active T-1 link supplying access to each of the individual 24 channels at the user's own facilities. This type of multiplexer is called a *T-1 multiplexer* and is described in Chapter 11.

The second type of multiplexer is known as a *drop-and-insert* multiplexer, shown in Fig. 16-5. The drop-and-insert multiplexer is utilized where the user needs to remove some DS-0 channels, add others, and at the same time maintain T-1 capacity between the individual locations along a circuit path. The drop-and-insert locations are normally geographically dispersed, so a substantial amount of network capacity can be incorporated into the system by utilizing the available DS-0 channels that exist in each point-to-point connection. The result is that there may be a single T-1 capacity connection on an end-to-end basis, but the individual point-to-point connections may have different users in the individual DS-0 channels.

A third type of multiplexer sometimes used is called a *networking multiplexer*, with which several T-1 circuits can be configured with a DCS such that entire DS-1 channels or individual DS-0 channels may be switched at individual user locations.

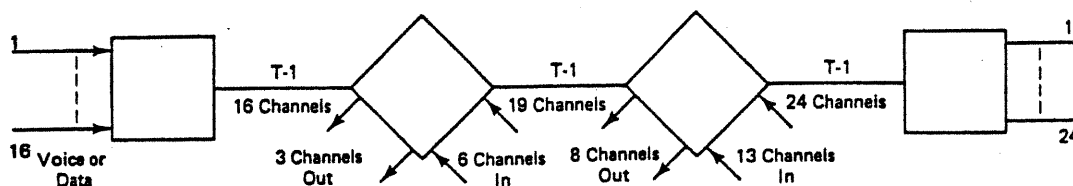


FIGURE 16-5
Drop-and-Insert Multiplexers

D

DIGITAL SERVICES

DDS and DDS-2

There are two primary services that are being provided by AT&T initially, Dataphone Digital Service and dial digital. Dataphone Digital Service (DDS) involves providing a four-wire leased circuit to the customer premises with connection to the digital network on an end-to-end basis. Figure 16-1 is representative of what such a circuit would look like. Digital circuits are available anywhere the local telephone companies have the ability to provide both a digital local loop and connection to a long-distance digital carrier, but keep in mind that many areas of the country will not be capable of accommodating digital service until their Class 5 central offices are replaced. If you can't get to the local telephone office digitally, and the AT&T Point of Presence (POP) is not close enough, you may not be able to obtain digital service at all (unless you go via direct satellite). Many people are surprised to find out that the local telephone company cannot provide the level of service they need when they build new facilities in suburban or rural areas. It wasn't until 1987 that Chicago became the first major city in the United States to be capable of providing digital service to all locations in that area, so even though there may be digital service around you, you need to find out from either the local or the long-distance carrier whether digital service will be available for your specific facilities.

DDS involves specific rates of data transmission: 2400, 4800, 9600, and 56000 BPS. In 1987 it was announced that 19.2 KBPS would soon be available, and 64 KBPS clear channel will eventually be available also. Each one of these substrates requires a full 64 KBPS DS-0 channel within which the specific substrate being used is identified. Information is routed through the digital network using only digital transmission, resulting in a very low error rate. Under certain conditions it is possible that there may be an analog link somewhere in the circuit; if so, it is strongly recommended that you not go digital at all because the analog distortion will cause additional errors in the data being transmitted.

One of the new features available with DDS is the ability to provide multiplexing for you in the carrier's office. This means you can then have circuits in

connect equipment. Because the interfaces of each of these equipments remove bipolar violations the customer has no access to performance statistics internal to the provider's facilities. Determination of end-to-end error rate performance in this environment requires taking at least a portion of the T1 circuit out of service (for which there is usually no spare).

ESF allows customers to achieve end-to-end in service performance monitoring by redefining the 8-kbps F bit of each DS1 frame to consist of a 2-kbps framing channel, a 4-kbps data link channel, and a 2-kbps CRC channel representing a check sum over all information bits. Because the CRC channel is carried intact from one customer location to another channel errors occurring in any intermediate facility produce CRC errors at the far end.

The data link supports numerous services, one of which is the ability to interrogate the far end, or any intermediate equipment, for performance statistics. Thus the data link provides both the customer and the service provider with an extremely useful tool for isolating faulty span lines or equipment.

As indicated in Table 4.8 obtained from reference [32], the three subchannels are established by "extending" the D4 superframe format to encompass 24 DS1 frames. Because the actual framing bits occur only once every four DS1 frames there are 771 bits intervening between bits carrying the Frame Pattern Sequence (FPS) = 001011.

The 6 CRC bits (C_1 to C_6) of each extended superframe represent a CRC check of all 4608 information bits in the previous superframe.* Besides providing end-to-end performance monitoring, the CRC virtually precludes the chances of false framing on a data bit position. Even though static user data can easily simulate the FPS, it is extremely unlikely that user data can spuriously generate valid CRC codes in successive superframes. (Six bits of random data match a 6-bit code with a probability of 1 in 64.)

The performance parameters measured and reported by the 4-kbps data link (DL) are framing bit errors, CRC errors, out-of-frame (OOF) events, line code (bipolar) violations, and controlled slip events (described in Chapter 7). Individual events are reported as well as event summaries. The four performance summaries reported are

1. Errored seconds (ESs) (ES = at least one CRC event).
2. Bursty second (BSs) (BS = 2-319 ESs).
3. Severely errored seconds (SESSs) (SES = > 319 ESs or OOF).
4. Failed seconds state (FS) (10 consecutive SES).

ESF CSUs typically determine the above parameters on 15-min intervals and store them for up to 24 hr for polling by a controller [38]. The SES report conforms to CCITT recommendation G.821.

*Calculation of the CRC code is not shown.

TABLE 4.8 Extended Superframe Framing Channel Format*

ESF Frame Number	ESF Bit Number	F-Bit Assignment	
		FPS	FDL
1	0	—	m
2	193	—	—
3	386	—	m
4	579	0	—
5	772	—	m
6	965	—	—
7	1158	—	m
8	1351	0	—
9	1544	—	m
10	1737	—	—
11	1930	—	m
12	2123	1	—
13	2316	—	m
14	2509	—	—
15	2702	—	m
16	2895	0	—
17	3088	—	m
18	3281	—	—
19	3474	—	m
20	3667	1	—
21	3860	—	m
22	4053	—	—
23	4246	—	m
24	4439	1	—

*FPS, framing pattern sequence (...001011...); FDL, 4 kbps facility data link (message bits m); CRC, CRC-6 cyclic redundancy check (check bits CB1-CB6).

In addition to supporting remote interrogation of performance statistics the data link carries alarm information, loopback commands, and protection switching commands.

4.7 TIME DIVISION MULTIPLEX LOOPS

In Chapter 2 it is mentioned that time division multiplexing is not as amenable to applications with distributed sources and sinks of traffic as is frequency division multiplexing. In this section a particular form of a TDM network is described that is quite useful in interconnecting distributed nodes. The basic

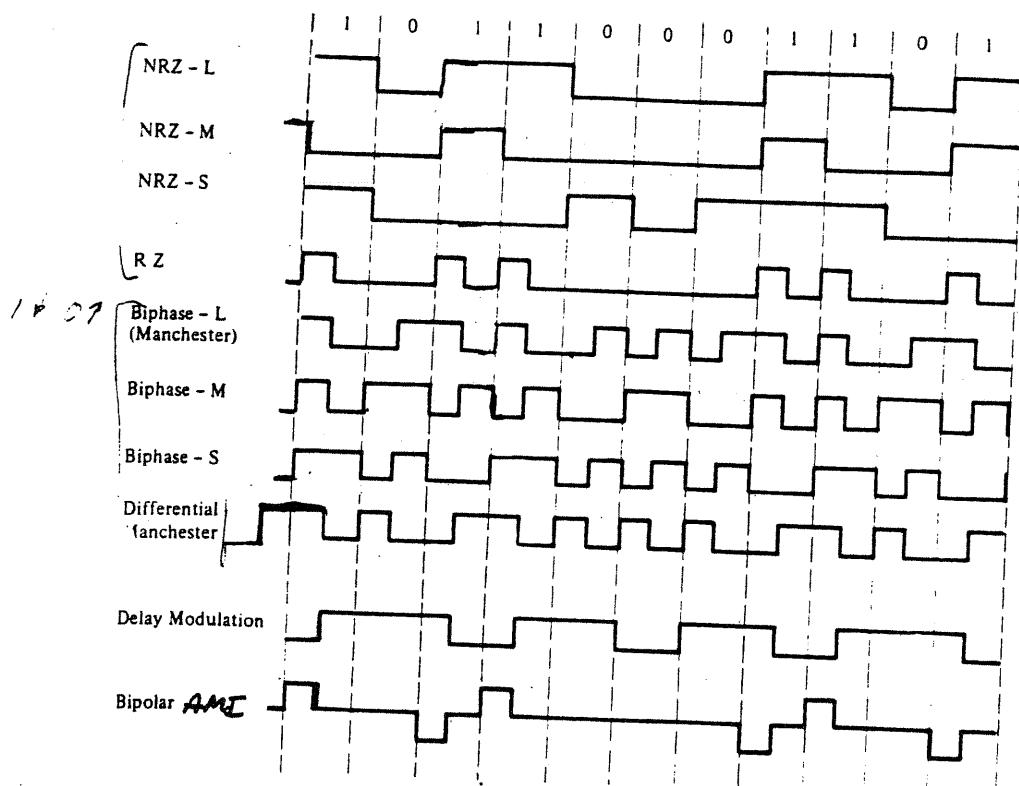


FIGURE 3-2. Digital signal encoding formats.

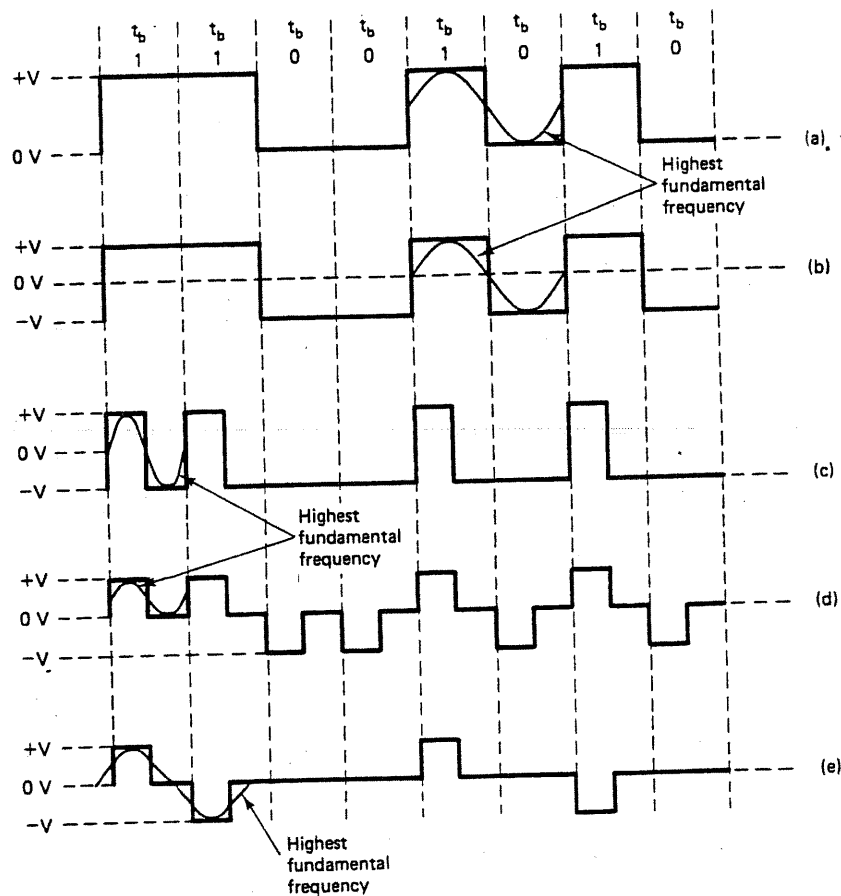


FIGURE 17-18 Line-encoding formats: (a) UPNRZ; (b) BPNRZ; (c) UPRZ; (d) BPRZ; (e) BPRZ-AMI.

Bandwidth Considerations

To determine the minimum bandwidth required to propagate a line-encoded signal, you must determine the highest fundamental frequency associated with it (see Figure 17-18). The highest fundamental frequency is determined from the worst-case (fastest transition) binary bit sequence. With UPNRZ, the worst-case condition is an alternating 1/0 sequence; the highest fundamental frequency takes the time of 2 bits and is therefore equal to one-half the bit rate. With BPNRZ, again the worst-case condition is an alternating 1/0 sequence and the highest fundamental frequency is one-half of the bit rate. With UPRZ, the worst-case condition is two successive 1's. The minimum bandwidth is therefore equal to the bit rate. With BPRZ, the worst-case condition is either successive

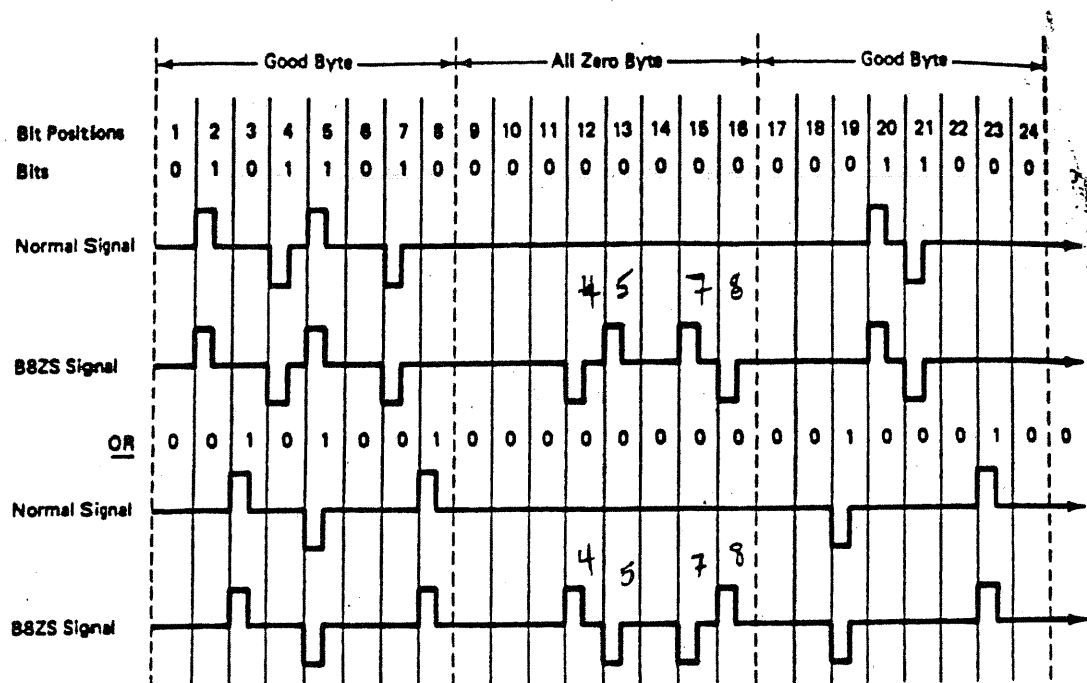


FIGURE 16-11
B8ZS—Zero Bit Suppression

DIGITAL ACCESS AND CROSSCONNECT SYSTEMS

AT&T DACS II - Digital Access Crossconnect Systems II represent an auxiliary switching technology in the PSTN and leased line product set.

DACS provide on demand wideband, narrowband, asynchronous, synchronous, analog or digital service to switched and private line users.

DACS has a basis in North American Digital hierarchy. This is based on 56-kb/s or 64-kb/s primary rate. PCM (pulse code modulation) scheme is used to convert the analog signal to digital by sampling it 8000 times per second. A sample value is assigned (0 -255). This value is converted to an 8 bit binary value represented by a combination of 1s and 0s.

This 8 bit value is sampled 8000 times per second equalling 64,000 bit per second to convert a voice grade/analog signal to digital. Using a scheme called "maintaining ones density" each 8th bit is forced to a value of 1. This is used for synchronization. As a result, from each chunk capable of transmitting 64,000 kb/s only 56,000 are available. (DS0)

The 56/64-kb/s channels are combined into bundles and given a digital designation under the North American digital scheme. The DACS interfaces with channels designated as DS1 or T1 or 1.544 mb/s. Under the North American scheme a 1.544 mb/s link can be divided into 24 voice grade channels or 23 data channels.

European CCITT (International Consultative Committee on Telegraphy & Telephony) digital standards use levels to designate their digital hierarchy - E1, etc. Each E1 channel rated at 2.048 mb/s is capable of supporting 32 (fully usable 64-kb/s) channels. Note CCITT and NA digital standards are not compatible. DACS IIs can interface with both sets of digital standards and make the necessary conversions.

DACSS differ from central offices switches in a number of import ways:

CO switches are optimized for short duration, switched analog traffic.

Xconnects are more suited for private line, data links and wideband services. Duration hours - months.

DIGITAL ACCESS AND CROSSCONNECT SYSTEMS

CO v. DACS -

CO OAM&P (operations, administration, maintenance and provisioning) is centralized. DACS support both centralized and decentralized OAM&P.

XCONNECT TECHNOLOGY:

Muxes over mixed transmission facilities - analog or digital, guided or unguided.

Standard rate is 64-kb/s. 1.544 or DS1 forms the base which is demuxed or broken into smaller 64-kb/s chunks.

Channels are xconnected using a TSI (Time Slot Interchange) scheme.

DACSs functions are controlled and executed by microprocessors and associated software.

DACS were developed by AT&T in the early 1970s and became commercially available in 1981. These early xconnects were cumbersome to operate and large.

The first generation of DACSs had 24/32 signals sent to a centralized location, demuxed for analog signals, xconnected, circuit conditioning, and maintenance. These signals were then remuxed to the primary rate and transmitted. This was both economically and labor intensive.

Current generation of DACSs use a more modular architectures based on shelves. Card sizes for each DACS is less than 20 square inches, non-blocking 32 bit microprocessor. Use of software makes upgrades, changes or customization simple. When DACS functionality evolves, new features are added by software. Main processor upgrades all others.

The heart of the DACS is the digital signal processing unit or DSPU. The DSPU supports the following functions:

- Digital multipoint bridging
- Voiceband data conferences
- Subrate multiplexing
- Multipoint junction for subrate muxed channels

DIGITAL ACCESS AND CROSSCONNECT SYSTEMS

FACILITY TERMINATION & XCONNECT:

Terminates both CCITT and North American primary rates.

Direct termination of North American DS-3 (45-mb/s) digital services. Eliminates the need for external muxes.

Extensive maintenance and performance monitoring for terminations.

Current DACS configurations can support 512 E1 or 640 DS-1 signals.

Multiple xconnects can be interconnected if more capacity is needed.

By 1991, DACS will be able to support 2,048 E1 or 2,560 DS-1 circuits.

Xconnects perform gateway functions- conversions to other nets.

Two command languages are used with the xconnect architecture:

PDS (program documentation Standards) - domestic

Man-Machine Language - CCITT and Bell Labs.

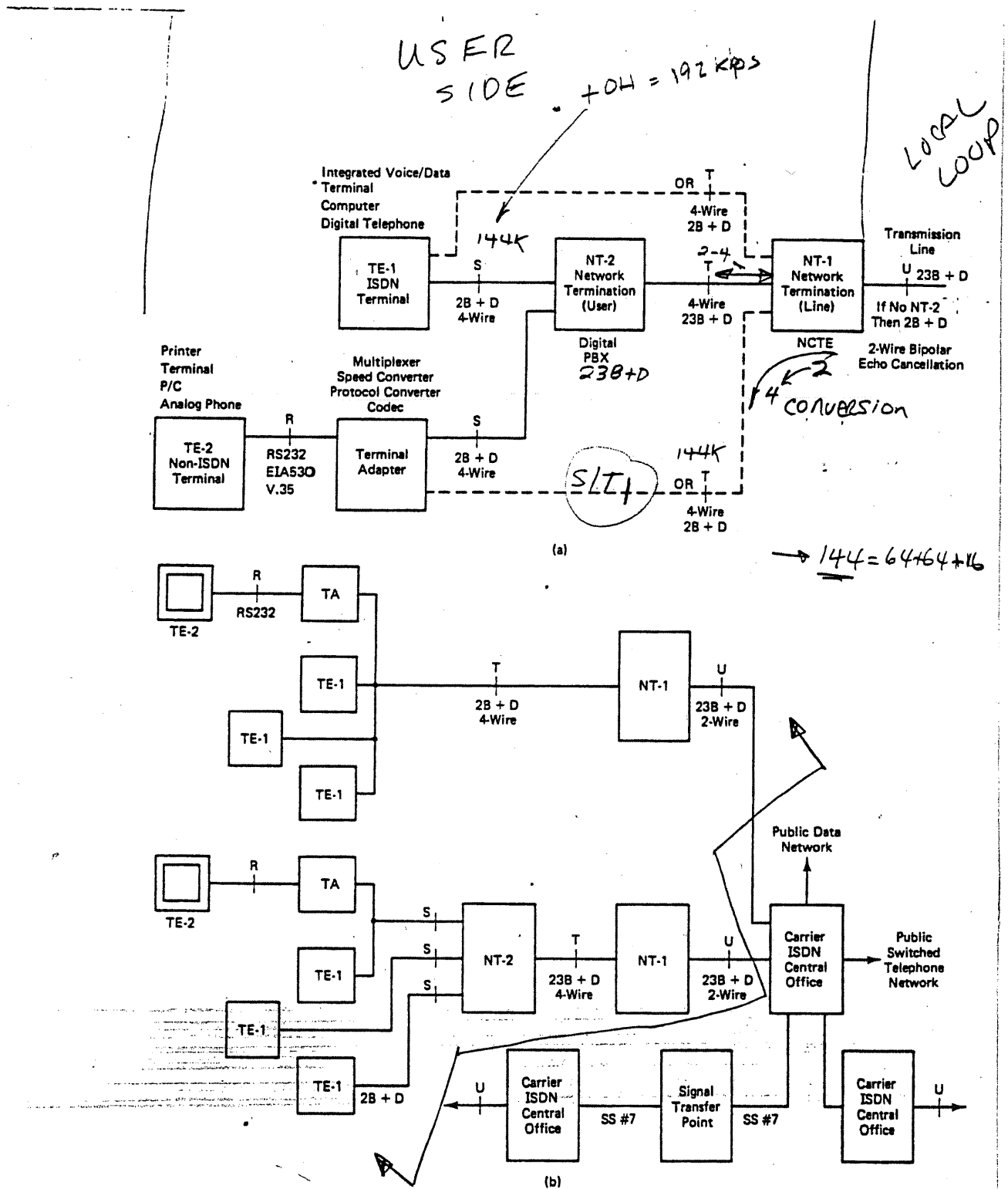


FIGURE 16-13
(a) ISDN Terminal Interfaces; (b) ISDN Network Interfaces.