

W5100S Errata Sheet

Document History

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Erratum 1	
Phenomenon	When SPI N bytes data Read Access operation, Data Invalid found
Condition	When reading N bytes of data using SPI ¹ , Data Invalid occurs over a certain clock speed after the first byte access and before the second byte access.
	In the case of W5100S SPI Read Timing, the first byte data requires a minimum delay of "6xSYS_CLK2" + 30ns" for data validation, and from the second byte, a delay of at least "3xSYS_CLK" is required between bytes.
Solution & Recommendat	CSn TCSS TCSN TCSN TCSN TCSN TCSN TCSN TCSN
IOII	TFDR(Frist Data Ready time): 6xSYS_CLK + 30ns TDR(Data Ready time): 3xSYS_CLK This issue can be resolved by inserting an additional delay of at least
	"3xSYS_CLK" between bytes during SPI read access operations. (Detailed timing information can be found in 7.4.3 SPI Access Timing in the W5100S datasheet).

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¹ The SPI provided by W5100S can access arbitrary length from 1 byte to N bytes depending on the memory size and register specified by the user.

 $^{^2}$ The W5100S defaults to SYS_CLK operation at 100 MHz, but clock switching allows for 25 MHz operation.