CIS-350 INFRASTRUCTURE TECHNOLOGIES

Study Guide for Test 2

Closed book, closed notes. You may use a calculator only for calculations. You may have a "cheat sheet", i.e., an index card 3"×5" filled up on one side with anything you want. The other side of the card should be blank. You need to turn this card with the test or show it to me after the test.

Materials covered:

(1) Chapters 7-11 to the extent they were covered in class or assigned explicitly for reading. Use lecture notes and/ slides posted for these chapters on BB as well as associated reading. There may also be a limited number of questions about the material in the textbook that we did not cover explicitly in class. For example, from some sections in chapter 10 on peripheral devices and chapter 11.
(2) Review Homeworks 4-5 as well as In-class Activities 4 and 5. The solutions for Homeworks and In-class Activities are posted on BB in the Assignments and Course Documents folders, respectively.

Test format:

(1) The test format will be similar to Test 1
(2) Multiple choice questions on all the mentioned material like in Sample Test 2 which follows.
(3) Short essay questions, similar to those in Homeworks as well as from the Reading Review Questions and Exercises following each chapter.
(4) Short numerical problems to work, similar to those in In-class Activity 5.
(5) Working the machine cycle for the LMC instruction (LDA, STO, ADD, SUB, or branch) like in In-class Activity 4.
(6) Fill in blanks and matching questions. Memorize the description of the keywords (those in bold) used in textbook.

This Sample Test 2 is very comprehensive and longer that the real Test 2 is going to be. You should be able to work this test in about 90 minutes maximum, including 3-5 essay questions. Test 2 is likely to be shorter and suitable for 75 minutes allocated for it. Good luck!

Sample Test 2

I. Multiple Choice Questions.

1. On the IBM Mainframe computer, memory to register (M ↔ R) instructions typically require _____ memory access(es).
a. 1 b. 0 c. 2 d. 4

2. A privileged instruction such as SVC 33 (request to increase storage) can be issued within the application program, but program control is always surrendered to _____ to execute the instruction.
a. the user b. the application program
c. the operating system d. the programmer

3. The _____ stores an address of the current/next instruction to execute.
a. instruction register b. accumulator c. control Unit d. ALU
e. program/instruction counter

4. The _____ executes an instruction and performs arithmetic and logic operations.
a. instruction register b. accumulator c. control unit d. ALU
e. program/instruction counter

5. The _____ holds the address of a memory location at which the instruction or data is stored.
a. MAR b. MDR c. instruction counter d. accumulator

6. The MAR and MDR act as an _____ between CPU and memory.
a. interfaces b. intermediaries c. buffers d. bridges e. caches

7. If the size of the MAR is 20 bits, it can address _____ unique memory locations.
a. 262144 b. 524288 c. 1048576 d. 2097152 e. 4194304

8. Access time to flash memory is about 120 _____.
a. seconds (s) b. milliseconds (ms) c. microseconds (μs) d. nanoseconds (ns)

9. A bus can carry _____.
a. instructions b. data c. addresses d. control signals
e. all the above

10. Programs always use _____ addresses, computer hardware needs _____ addresses.
a. physical/logical b. logical/physical c. indirect/direct d. immediate/indexed

11. Access time to registers is _____.
a. measured in milliseconds b. measured in microseconds
c. measured in seconds d. almost instant

12. In _____ network, signals sent by a particular computer on a network are received by every other computer connected to the network.
a. Ethernet b. LAN c. WAN d. MAN e. token ring

13. _____ buses are subject to radio-generated electrical interference which limits their speed and length.
a. Serial b. Parallel c. Full-duplex d. Multi-point e. Simplex

14. The interfaces between buses are called _____.
a. buffers b. tokens c. bridges d. rings e. lines

15. Which of the following is the privileged instruction?
a. RETURN b. CALL c. ADD d. SVC e. LDA

16. Which of the following data storage structure operates in a LIFO manner?
a. stack b. 1-dimensional array c. 2-dimensional array d. list
e. queue

17. Relatively slow data memory accesses could be reduced by increasing the number of _____.
a. flag registers b. instruction pointer registers c. MAR
d. general purpose registers e. instruction registers

18. In the Transmeta Crusoe CPU the instruction bundle consist of _____ bits.
a. 64 b. 128 c. 256 d. 32 e. 16

19. In which of the following architectures a 5-bit template tells the CPU how to handle the instructions?
a. very long instruction word (VLIW) architecture
b. explicitly parallel instruction computer (EPIC) - Intel Itanium architecture
c. Intel 32-bit architecture d. Pentium architecture

20. _____ create problems in pipelining.
a. Branching and stalling b. Branching and reordering
c. Stalling and reordering d. branching and hyperthreading

21. In _____ method, memory is partitioned into subsections, each with its own memory address register (MAR) and memory data register (MDR).
a. wide path memory access b. memory interleaving c. cache memory
d. virtual memory

22. To be effective, cache operations must be completely controlled by software.
a. True b. False

23. A hardware _____ checks the tags to determine of the memory location of the request is presently stored within the cache.
a. LRU controller b. cache controller c. write controller d. virtual controller
e. disk controller

24. Cache memory is like virtual memory and it does not exist physically.
a. True b. False

25. During the _____ operation writes to memory are made only when a cache line is actually replaced.
a. rewrite b. write through c. write back d. write out

26. In a master-slave processing system, a slave controls all resources and scheduling.
a. True b. False

27. In symmetrical multiprocessing, each CPU has equal access to resources.
a. True b. False

28. _____ translate data and signals to the form acceptable (understandable) to a peripheral device and control the peripheral device.
a. I/O modules or interfaces b. interrupts
c. interrupt handling routines d. buffers

29. Interrupts originate in the computer _____.
a. hardware or software b. hardware only c. software only

30. Which architecture is <u>not</u> suitable for fast data transfer between memory and peripheral devices?
a. channel architecture b. programmed I/O architecture
c. DMA architecture d. bus architecture

31. Fault-tolerant systems
a. have the ability to recover gracefully from hardware or software failures and still maintain a reasonable service.
b. guarantee correct and completely error-free operation
c. distribute loads between CPUs evenly

32. A channel
a. establishes communication with a peripheral device and assumes the responsibility for I/O transfer
b. releases the main processor to do other tasks
c. sends an interrupt to the main processor to tell it that the I/O transfer is finished
d. all of the above

33. On the IBM/z Series computers, interrupts are divided into _____ classes.
a. 4 b. 5 c. 6 d. 7 e. 8

34. Which interrupt originates in the computer hardware?
a. I/O request generated by the computer program
b. SVC call
c. program interrupt (generated by an illegal instruction)
d. external interrupt from the timer (when the program exceeds the slice of the CPU time allocated to it.

35. An image has a resolution of 800x1200 pixels. On the true color system this image would use _____ bytes of storage.
a. 960,000 b. 1,920,000 c. 2,880,000 d. 3,840,000

36. A shortcut R.A.I.D. stands for _____.
a. remote array of inexpensive disks b. redundant array of independent/inexpensive disks
c. remote access to independent drive d. redundant access input devices

37. Hard disks generally store data in a _____ format.
a. constant linear velocity (CLV) b. constant angular velocity (CAV)
c. variable linear velocity (VLV) d. variable angular velocity (VAV)

38. In a 4-disk mirrored array access time could be reduced _____ times as disks use independent controllers.
a. 2 b. 4 c. 3 d. 5

39. In a striped disk array, one disk is usually used for _____,
a. data checking b. parity checking c. system checking d. sector checking

40. The computer screen is a rectangle of the sides of 11 and 16 inches. What is the approximate size (in inches) of the diagonal?
a. 17.2 b. 24.0 c. 18.6 d. 19.42
e. None of the above

41. On disk, data are recorded on concentric circles called
a. blocks b. sectors c. tracks d. clusters

42. If the size of the logical record is 50 bytes and the blocking factor is 100, the size of the physical record is _____ bytes.
a. 2 b. 0.5 c. 500 d. 5000

43. On IBM computers, each _____ has the unique address.
a. double-word b. word c. byte d. bit

44. The most common size of RAM in contemporary PC computers available on the market now is close to
a. 16KB b. 1MB c. 64TB d. 2GB.

45. Flags are _____ registers used to keep track of special conditions such as overflow.
a. status b. general-purpose c. memory data d. memory address

46. The following sequence of steps in the instruction cycle:

PC $\rightarrow$ MAR
MDR $\rightarrow$ IR
IR [address] $\rightarrow$ MAR
A $\rightarrow$ MDR
PC+1 $\rightarrow$ PC

represents the _____ instruction.
a. ADD b. SUB c. STO d. LDA e. BR

47. If the instruction's operation code is 5 bits long, how many unique instructions can it represent?
a. 4 b. 32. c. 16 d. 8 e. 5

48. A typical capacity of a hard disk in a modern personal computer is about _____.
a. 200 MB b. 200 KB c. 200 GB d. 200 Bytes e. 200 TB

49. In the interest of increasing the execution speed of instructions, the order in which the CPU finds data and instructions is as follows:
a. registers, cache, RAM, disk, tape b. RAM, cache, registers, tape, disk
c. disk, registers, cache, tape, RAM d. registers, tape, RAM, cache, disk

50. Which of the following display technologies has become the prevalent means of displaying images?
a. cathode ray tube (CRT) b. organic light-emitting diode (ORED)
c. liquid crystal display (LCD) d. laser e. impact

51. The concept known as _____ means that individual components of the computer are designed to work together in such a way that overall performance is enhanced beyond the performance of each component.
a. fit b. synergy c. scalability d. flexibility e. accessibility

52. The abbreviation "VLSI circuits" stands for _____.
a. very-large-scale integrated circuits b. very-low-scale integrated circuits
c. very large system integration circuits d. very low system integration circuits

53. The system bus, which is the primary interface with the CPU, is sometimes referred to as _____.
a. PCI-Express b. PCI bus c. external CPU bus d. front side bus

54. Which of the following is <u>not</u> a very fast interface bus suitable for high-speed data transfers?
a. ISO b. SCSI c. USB d. SATA e. FireWire

55. Multiprocessing systems are commonly known as tightly-coupled systems.
a. True b. False

56. Commodity-off-the-shelf components are inexpensive computers connected together to form a _____ cluster.
a. blade b. grid c. Beowulf d. super

II. <u>Fill out the blanks with the most appropriate word(s)</u>

1. DRAM stands for _____.

2. Eight bytes contains _____ bits (How many)?

3. One byte can store _____ unique patterns (How many)?

4. A shortcut MIPS stands for _____

5. Checking each peripheral device for input in rotation at frequent intervals is called _____.

6. Interrupts originate in the computer _____ or _____ but are processed by the computer _____.

7. Multiple interrupts can be handled by assigning _____ to each interrupt.

8. Computers provide interrupt capability by providing special control lines to the CPU known as _____. They are usually labeled as _____.

9. In an instruction STO 50, an implicit source is an _____.

10. Assume that the content of the accumulator is 25. If you perform the right arithmetic shift of the accumulator by 1 bit, the new contents of the accumulator will be _____.

11. Assume that the content of the accumulator is 20. If you perform the left arithmetic shift of the accumulator by 2 bits, the new contents of the accumulator will be _____.

12. The first phase in the instruction (machine) cycle is called the _____ phase, and the second phase is called the _____ phase.

13. The _____ holds a data value that is being written to or read from the memory location currently addressed by the MAR.

14. A _____ is a set of parallel or serial wires, or optical conductors that can carry bits.

15. Two different processing methods are used for determining which device initiated an interrupt. These methods are _____ and _____.

16. In _____, one can start the fetch cycle for the current instruction during the execute cycle for the previous instruction. In other words, instructions can overlap.

17. Two methods of implementing a disk array are: a _____ array and a _____ array.

18. The method, by which each display is produced by scanning and displaying each pixel, one row at a time, from left to right is called _____.

19. Cache memory works due to a principle known as _____, which means that at any given time most memory references will be confined to one or a few small regions in memory.

20. When cache memory is full, some blocks in cache memory must be selected for replacement using the LRU method. The LRU stands for _____.

21. The main function of an/the _____ is to translate data and signals to the form acceptable and understood by the peripheral device, and to control the peripheral device.

22. In disk arrays data redundancy is _____, whereas in a well designed database data redundancy is _____.

23. SCSI stands for _____

24. The two primary models used for clustering (or fault-tolerant systems) are _____ and _____.

III. Suppose that the following instruction and data is found at memory locations 05 and 75, respectively.

Address	Instruction (mnemonic)	Numeric code
…..	……..	
05	LDA 75	575
….		
75	40	

Show the contents of the PC, the MAR, the MDR, the IR, and the Accumulator (A) as each step of the fetch-execute cycle is performed for instruction **LDA 75** residing at address 05. If the contents of the register is unknown, write the "?" in the space provided.

	PC	MAR	MDR	IR	A
PC $\rightarrow$ MAR	____	____	____	____	____
MDR $\rightarrow$ IR	____	____	____	____	____
IR [address] $\rightarrow$ MAR	____	____	____	____	____
MDR $\rightarrow$ A	____	____	____	____	____
PC+1 $\rightarrow$ PC	____	____	____	____	____

IV. Short calculations/answers

1. If the rotational speed of the disk is 100 revolutions per second, the average latency time is _____ milliseconds.

2. If the rotational speed of the disk is 8400 revolutions per minute, the average latency time is _____ milliseconds.

3. A disk pack contains 13 platters. The data can be recorded on both surfaces of each platter except the top and the bottom platter. The top and the bottom platter can store data on their inner surfaces only. Each surface has 500 tracks. One track can hold 50,000 bytes of information. What is the capacity (expressed in KB and MB) of one cylinder? What is the capacity (expressed in MB and GB) of the entire disk pack? Show your computations.

4. Assuming that the rotational speed of the disk is 12,000 revolutions per minute, each track has 200 sectors, and seek time is 9 ms, calculate the total disk access time for 120 sectors. Note that this time will be the sum of seek time, latency time, and transfer time of 120 sectors.

V. Short essay questions - These are examples of the short essay questions. There will be only between 3 and 5 short essay questions on Test 2.

1. What factors determine the speed of the computer?

2. Why are buses used in the computer? What can they carry? What is the difference between multipoint bus and point-to-point bus? Explain the term *throughput* and *data width* of the bus.

3. What are registers? Where are they located? Why are they needed? Are they temporary or permanent memory?

4. Describe common features and differences between serial and parallel interface.

5. What is the disk interface and what does it do?

6. Explain the Programmed I/O.

7. Discuss vectored interrupt and polling.

8. Give the examples of interrupts that originate in software and hardware

9. What is pipelining?

10. Describe the write-through and write-back operations in cache memory.

11. How are multiple interrupts handled?

12. Discuss the concepts of mirrored and striped disk arrays.

13. List techniques that improve the disk performance in terms of access time.

14. Discuss the methods of displaying pixels on the computer screen

15. Explain what is meant by *synergy*.

16. What is a loosely coupled system? How does it differ from a tightly coupled system?

17. Discuss the advantages of clustering.

18. What is grid computing?

19. Explain the operation of the SCSI.

20. Explain the basic USB topology.

Answers

I.

1. A
2. C
3. E
4. D
5. A
6. A
7. C
8. C
9. E
10. B
11. D
12. A
13. B
14. C
15. D
16. A
17. D
18. B
19. B
20. A
21. B
22. B
23. B
24. B
25. C
26. B
27. A
28. A
29. A
30. B
31. A
32. D
35. C
36. B
37. B
38. B
39. B
40. D
41. C
42. D
43. C
44. D
45. A
46. C
47. B
48. C
49. A
50. C
51. B
52. A

33. C
34. D

53. D
54. A
55. A
56. C

II.

1. dynamic random access memory
2. 64
3. 256
4. millions of instructions per second
5. polling
6. hardware, software, software
7. priority
8. interrupt lines, IRQ or INT
9. accumulator
10. 12 (integer division)
11. 80
12. fetch, execute
13. memory data register (MDR)
14. bus
15. vectored interrupt, polling
16. pipelining
17. mirrored, striped
18. raster scanning
19. locality of reference
20. least recently used (LRU)
21. I/O module or interface
22. desired, not desired
23. Small Computer System Interface
24. shared-nothing, shared disk

III.

	PC	MAR	MDR	IR	A
PC $\rightarrow$ MAR	05	05	575	?	?
MDR $\rightarrow$ IR	05	05	575	575	?
IR [address] $\rightarrow$ MAR	05	75	40	575	?
MDR $\rightarrow$ A	05	75	40	575	40
PC+1 $\rightarrow$ PC	06	75	40	575	40

575 may be replaced with LDA 75.

IV.

1.

$\frac{1}{2}\frac{1}{100} = \frac{1}{200}$ seconds = 5 milliseconds

2.

1 minute has 60 seconds

8400 revolutions /minute = 8400/60 = 140 revolutions/second

$\frac{1}{2}\frac{1}{140} = \frac{1}{280}$ seconds = 3.57 milliseconds

3.

(a) The number of recording surfaces is 11*2+1+1=24
(b) The capacity of the cylinder = 24 * 50,000 bytes = 1,200,000 bytes = 1,171.875 KB = 1.144 MB
(c) The capacity of the entire disk pack = 1.144 MB * 500 tracks = 572.0 MB = 0.559 GB

4.

The number of revolutions/second is 12,000/60=200

Latency time = $\frac{1}{2}\frac{1}{200} = \frac{1}{400}$ seconds = 2.5 ms

Transfer time = $\frac{120}{200 \times 200} = \frac{120}{40000}$ seconds = 3.0 ms

Seek time = 9 ms

The total disk access time is the sum of the three times = 9 ms + 2.5 ms + 3.0 ms = 14.5 ms

V.

The answers to the essay questions are in the textbook, lecture notes, or homework solutions posted on BB.