CprE 381: Computer Organization and Assembly Level Programming

381 Design Cycle

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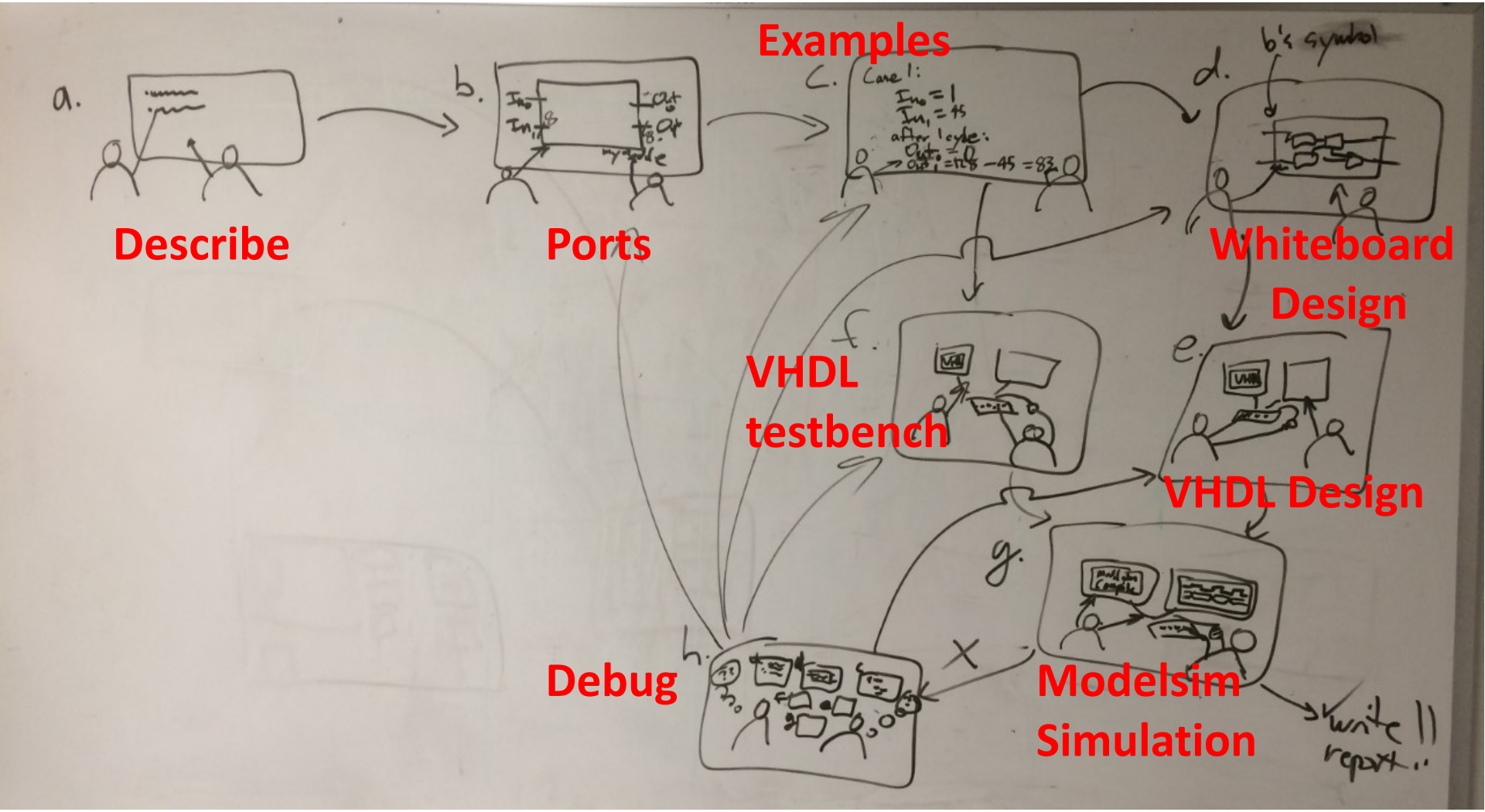
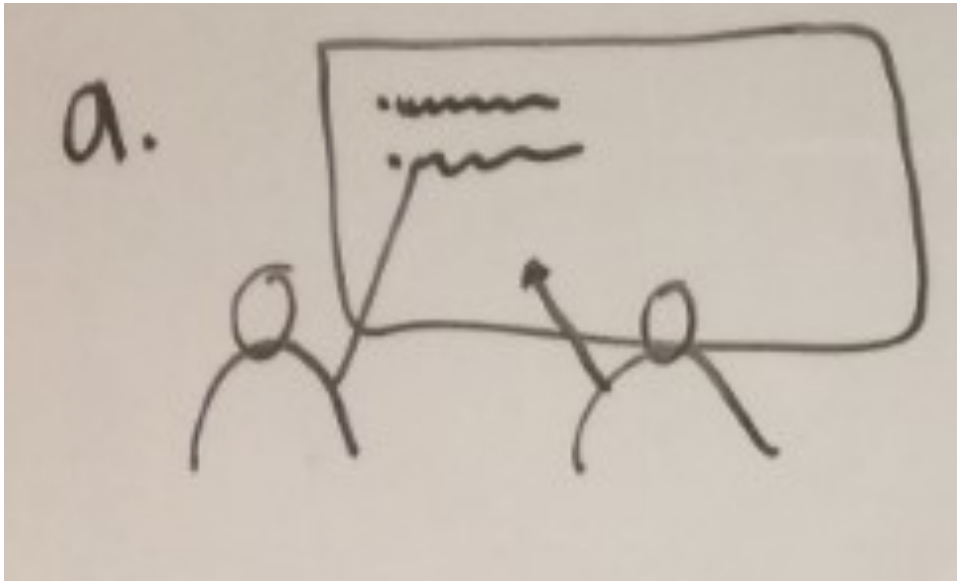
Design Cycle

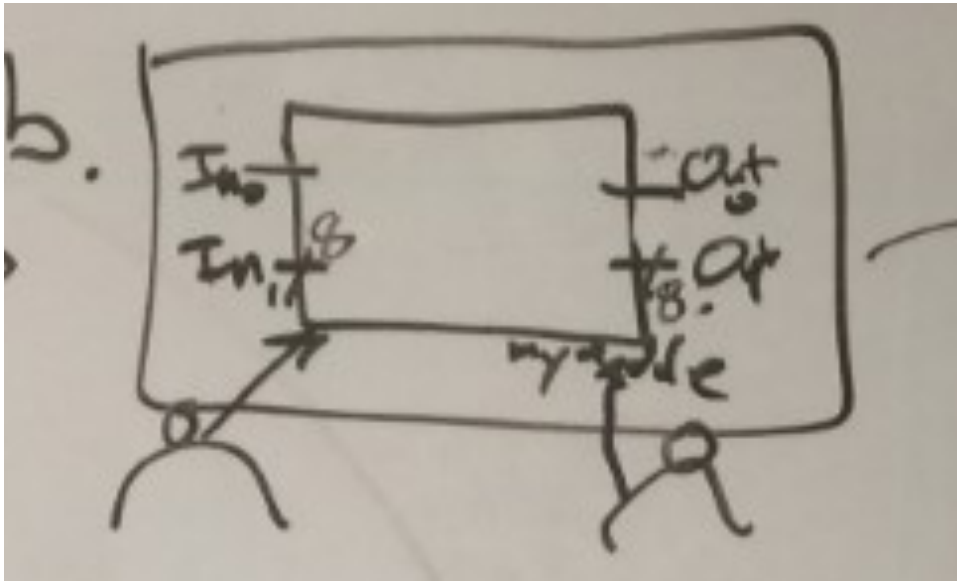


Describe



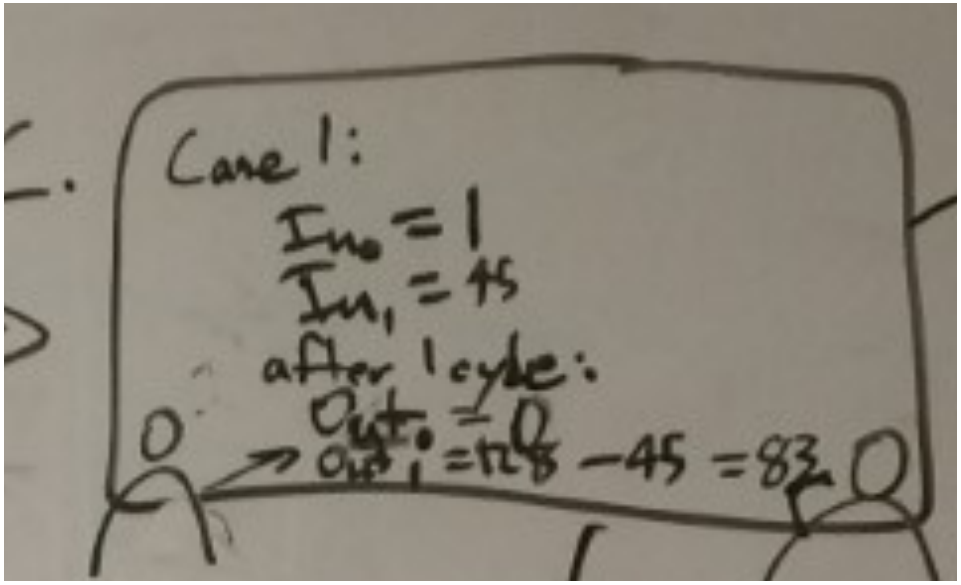
- Write a simple English description of the module
- Use a whiteboard, paper, or even text editor
- This can eventually become your module's description comment

Ports



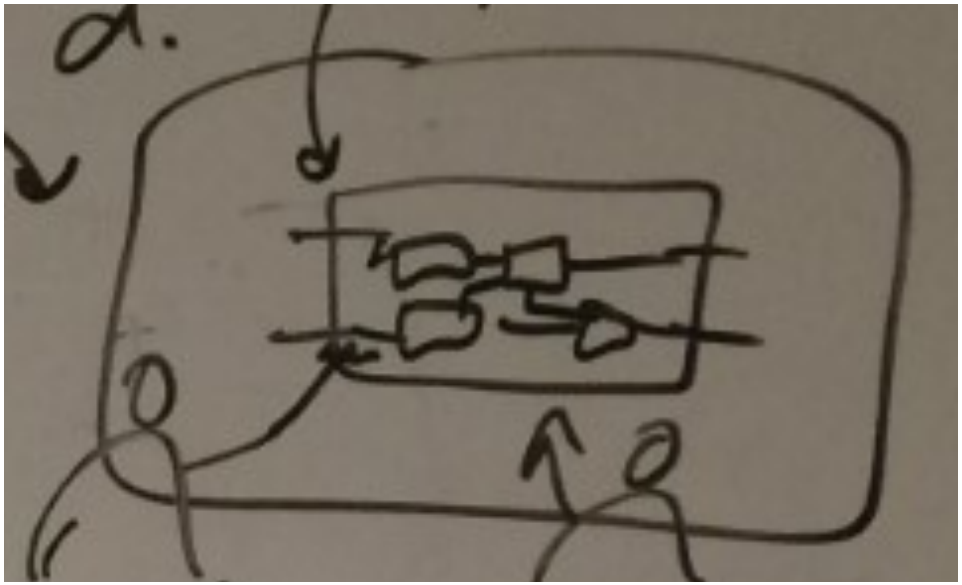
- Draw symbol/define inputs and outputs, including number of bits
- Use a whiteboard, paper, or even text editor
- This will eventually be your VHDL entity's port list

Examples



- List several specific inputs with their expected outputs
- Use a whiteboard, paper, or even text editor
- This will eventually become the start of your test cases

Draw Design



- Draw/define implementation
  - Often this is a structural datapath design as shown in the figure at the end of the lab manual
  - Also be a table of control signals or a truth table or ASM chart
  - May need to break problem down into more modules or blocks
- Use a whiteboard, paper, or even text editor
- This will eventually become the heart of your VHDL code.

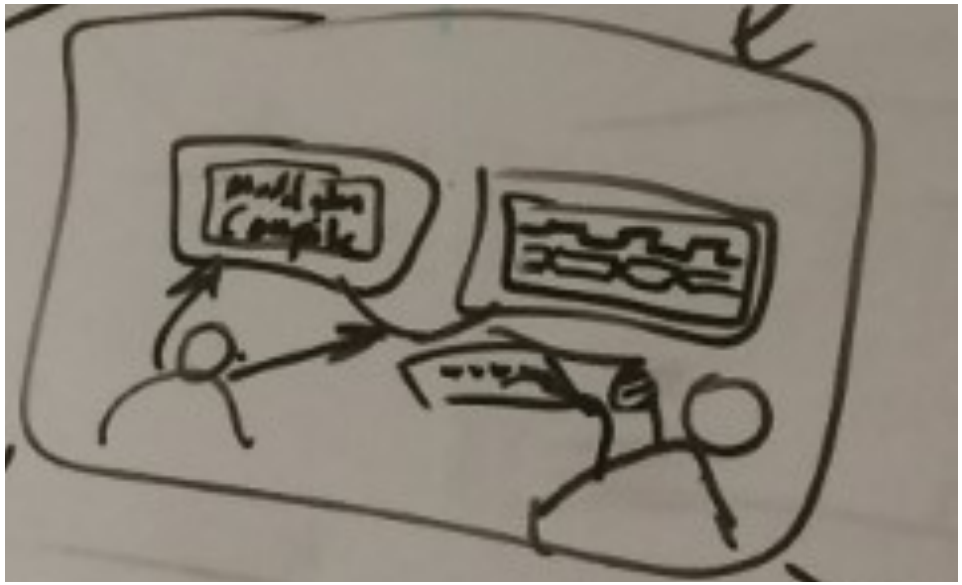
VHDL Design

- Translate design into a VHDL description.
- Use Modelsim or Notepad++ or preferred text editor
- Have VHDL references and internet handy

VHDL Testbench

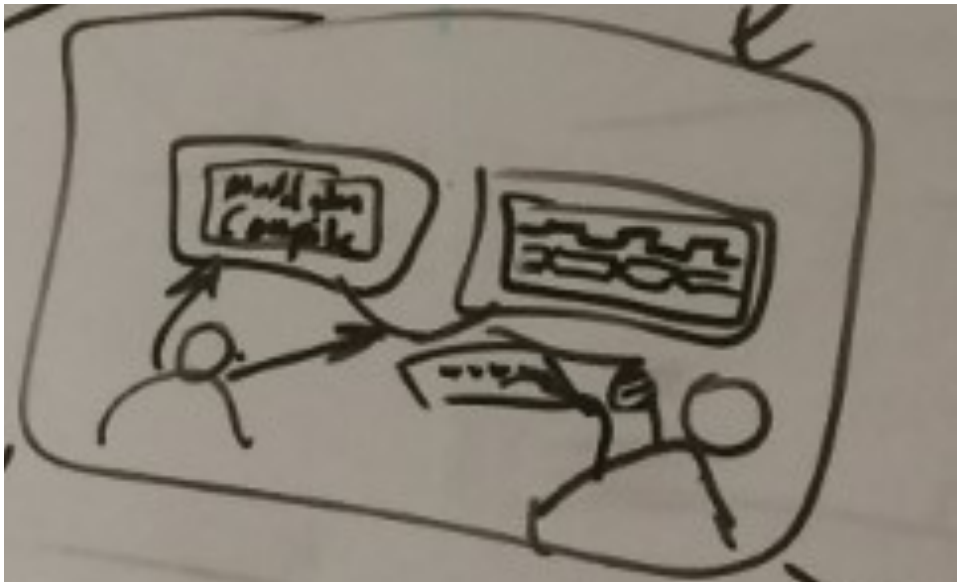
- Translate examples into a VHDL testbench and add additional tests needed
- Use Modelsim or Notepad++ or preferred text editor
- Have VHDL references and internet handy
- Revisit the test cases as you revisit your design

Modelsim Simulation



- Simulate testbench and check results against your expectations
- Use a .do file to automatically add signals to waveforms and to format radices and labels

Debug



- Debug as needed, starting from wherever the error may be.
- Tips:
  - Fix all errors AND warnings
  - No red X's in waveform that aren't intended
  - Work backwards from first observed error
  - Compare to your design drawing
  - Your understanding or expectation may be wrong