VHDL Programming in CprE 381

Henry Duwe

Spring 2020

CprE 381

Iowa State University

Model Truth Table Part II

Use when … else statement (FreeRange VHDL 13.10 for more information)

```
with D_IN select
   F_OUT <= “00000001” when “000”,
            “00000010” when “001”,
            “00000100” when “010”,
            “00001000” when “011”,
            “00010000” when “100”,
            “00100000” when “101”,
            “01000000” when “110”,
            “10000000” when “111”,
            “00000000” when others;
```