VHDL Programming in CprE 381

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Submission

- See “Demo and Submission” on final pages of lab manual
  - There is no demo
  - Turn zip file and pdf in to “Lab 1: Orientation” assignment
    - You can resubmit multiple times – we will grade your last submission before the due date (if after the due date you must send your TA an e-mail)
  - Turn individual eval/feedback in to “Lab 1: Individual Feedback (Required)”
    - Ungraded, but your lab grade will not be assigned until you do this.
  - Submit pre-lab and new team contract to the next lab’s assignment page (e.g., “Lab 2: My First MIPS Datapath”)

Model Truth Table

Use when … else statement (FreeRange VHDL Listing 4.11 for full file)

```
entity my_4t1_mux is
   port (D3,D2,D1,D0 : in std_logic;
         SEL : in std_logic_vector(1 downto 0);
         MX_OUT : out std_logic);
end my_4t1_mux;
architecture mux4t1 of my_4t1_mux is
begin
   MX_OUT <= D3 when (SEL = “11”) else
             D2 when (SEL = “10”) else
             D1 when (SEL = “01”) else
             D0 when (SEL = “00”) else
             ‘0’;
end mux4t1;
```

Generic Constant

- *Generic constant* is used to parameterize an entity

```
entity mux2t1_N is
  generic(N : integer := 16);
  port(i_S    : in std_logic;
       i_D0   : in std_logic_vector(N-1 downto 0);
       i_D1   : in std_logic_vector(N-1 downto 0);
       o_O    : out std_logic_vector(N-1 downto 0));
end mux2t1_N;
```

- Can be added to entity
- Takes a default value

Generic Constant

```
architecture behavior of tb_mux2t1_N is
component mux2t1_N
  generic(N : integer := 32);
  port(i_S        : in std_logic;
       i_D0       : in std_logic_vector(N-1 downto 0);
       i_D1       : in std_logic_vector(N-1 downto 0);
       o_O        : out std_logic_vector(N-1 downto 0));
end component;…
begin
  …
```

- The default value can be changed in a component statement

Generic Constant

```
DUT: mux2t1_N
   generic map( N => 32)
   port map(…
```

- The generic constant value can also be decided in a component instantiation statement

Generate Statement

- A for…generate statement may used in an architecture to instantiate **an array of component instances**

```
 G_NBit_MUX: for i in 0 to N-1 generate
    MUXI: mux2t1 port map(
       -- All instances share the same select input.
             i_S      => i_S,
       -- ith instance's data 0 input hooked up to
ith data 0 input.
             i_D0     => i_D0(i),
i_D1     => i_D1(i),
             o_O      => o_O(i));
  end generate G_NBit_MUX;
```