**Tasks**

1. Breakdown resources and tasks
   1. Download PMOD documentation from Digilent, schematic of PMOD, and SSD1331 OLED controller reference manual
   2. Determine I/O of PMOD
   3. Determine how to startup, turn off, and reset controller
   4. Determine different available commands
2. FPGA MOSI SPI interface
   1. Drive FPGA as master to control chip select, MOSI, and slave clock
   2. Should send 1 byte of data, or 2 hex values at a time
   3. Should drive D/C (data/command control) bit at start of every byte sent
3. MOSI Byte Buffer
   1. Take in X bytes to transmit concurrently, with individual D/C bits for each
4. Shape Wrapper
   1. Startup
   2. Draw a line
   3. Draw a rectangle
   4. Clear window
   5. Reset
5. Wrapper for SPI interface to change color of drawn shapes
6. Write text, update over certain amount of time
   1. Create table for ASCII values

**Nbit\_MOSI\_SPI**

Function

* Load 1 byte of data and serial transmit from MSB to LSB over o\_MOSI
* Drive o\_CS and o\_DC on neg edge so will be stable for slave to read

Parameter

* WIDTH: default 8, N bits to transmit in one set

Input

* I\_RST: asynchronous reset
* I\_SCK: clock for slave interface, has to transmit on it
* I\_DATA: byte to transmit to OLED interface slave (can either be command or data)
* I\_START: begin transmitting byte in i\_DATA
* I\_DC: D/C control to be updated on negedge at same time as data on MOSI line

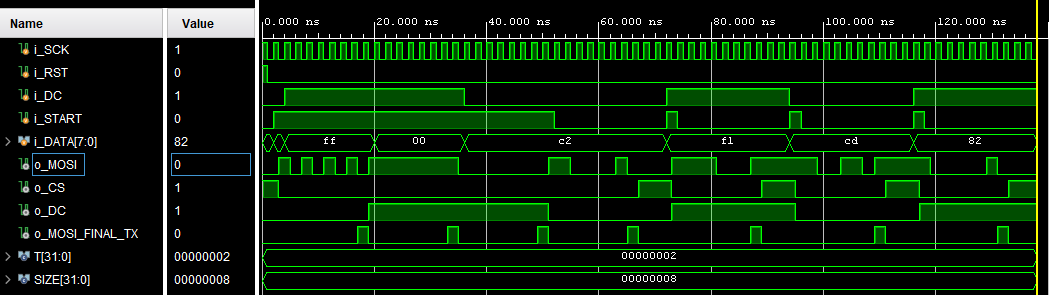
Output

* O\_MOSI: Output 1 bit at a time of i\_DATA, starting with MSB
* O\_CS: chip select, active low
* O\_DC: D/C to control data vs. command for the OLED controller
* O\_MOSI\_FINAL\_TX: asserted when last bit transmitted

States

* Idle: waiting for i\_START to be asserted once to transmit byte
* Transmit: transmit byte, stay in state if i\_START asserted by end, otherwise back to idle

**Nbit\_MOSI\_SPI\_tb**



**Nbyte\_MOSI\_SPI\_buffer**

Take in X inputs parallel, serially load them and drive start of master SPI MOSI

Paramters

* WIDTH: number of bits to transmit in one set
* N: max # of sets that can be parallel loaded

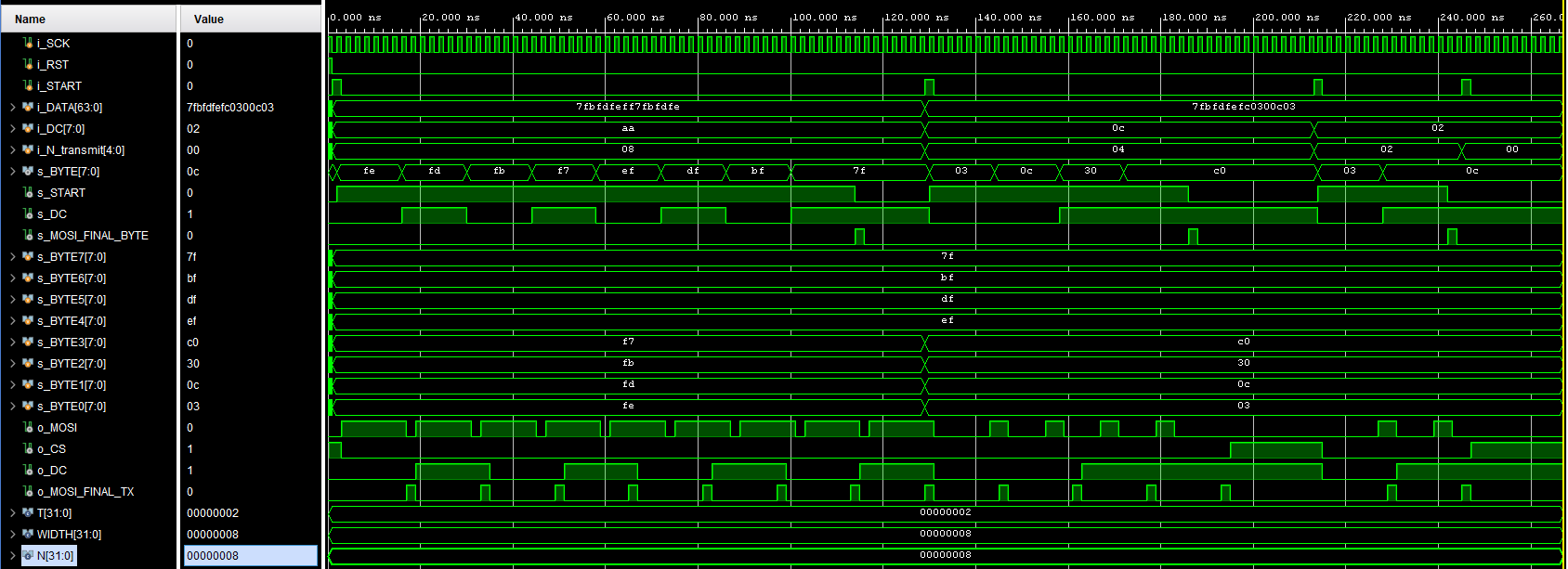
Inputs

* I\_SCK: SPI clock
* I\_RST: asynch reset
* [WIDTH\*N-1:0] i\_DATA: 2D bit array holding N sets to transmit over MOSI
* [N-1:0] i\_DC: D/C command for each byte
* I\_START: start from driver control, initiate parallel load of bytes
* [4:0] i\_N\_transmit: # of N bytes to transmit on load, will be counted

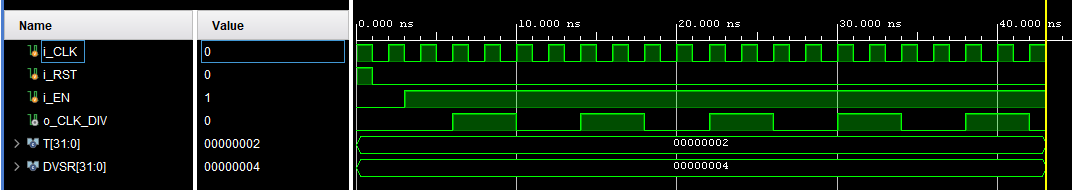
Outputs

* [WIDTH-1:0] o\_DATA: byte to feed to master SPI shift module
* O\_START: start bit to transmit another byte over MOSI, keep on to keep going
* O\_DC: D/C read from input DC for each respective byte
* O\_MOSI\_FINAL\_BYTE: final byte to transmit

**Nbyte\_MOSI\_SPI\_buffer\_tb**



**Clock Divider**



**OLED\_Interface**

Paramters

* WIDTH: number of bits to transmit in one set
* N: max # of sets that can be parallel loaded
* SCLK\_DIVIDER: minimum period for SCK
* WAIT\_3\_US: # of count to wait 3 us on 100MHz clock
* WAIT\_100\_MS: # of count to wait 100 ms on 100MHz clock
* NUM\_COL: # of pixel columns in OLED array
* NUM\_ROW: # of pixel rows in OLED array
* ASCII\_COL\_SIZE: # of x bits of ASCII char
* ASCII\_ROW\_SIZE: # of y bits of ASCII char
* N\_COLOR\_BITS: # of color bits in pixel transmission. Either 16 or 8 bits

Input

* I\_CLK: FPGA clock
* I\_RST: asynch reset
* [1:0] I\_MODE: display mode select, will determine state machine load
* I\_START: load bytes and transmit
* I\_TEXT\_COLOR: text color of ASCII
* I\_BACKGROUND\_COLOR: color for pixels not ASCII, background
* I\_ASCII: 1 byte ASCII values, filling array of ASCII\_COL\_SIZE \* ASCII\_ROW\_SIZE

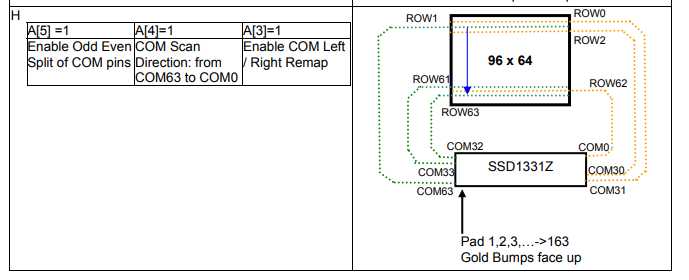
Output

* O\_CS: Active low chip select
* O\_MOSI: Master out slave in serial bit
* O\_SCK: Slave clock
* O\_D/C: Data/Command control
* O\_RES: power reset
* O\_VCCEN: VCC Enable
* O\_PMODEN: Vdd Logic Voltage control
* O\_MOSI\_FINAL\_BIT: indicator of final bit in byte transmission
* O\_MOSI\_FINAL\_BYTE: indicator of final byte transmission of SPI byte buffer

Uses the Nbit\_MOSI\_SPI to send serial bits to OLED display over MOSI. Also drives CS and D/C. This will include a clock divider to count/utilize the FPGA clock and drive O\_SCK for the byte buffer and slave OLED display.

Turn on Steps:

1. Apply power to VDD, VDDIO (3V3 supply on FPGA)
2. Set RES pin to low for atleast 3 us
3. Set RES pin to high, set VCCEN to high, set PMODEN to high, wait 3 us
4. After VCC is stable, send command 0xAF for display ON, wait 100 ms
5. Set Display Settings
   1. Send command byte 0xA0
   2. Send data byte to update to 256 color format (bit 6 to 1)
   3. Set display row/col order: A[5:3] = 3b111
   4. Other bits kept as default settings like in reset



ASCII Draw steps:

1. Load next ASCII value
2. Set start and end row based on ASCII position
   1. Set Row command, 0x75
   2. Starting row address (range from 00d to 63d) , data command
   3. Ending row address (range from 00d to 63d), data command
3. Set start and end column based on ASCII position
   1. Set Row command, 0x15
   2. Starting row address (range from 00d to 93d), data command
   3. Ending row address (range from 00d to 93d), data command
4. Transmit 8x8 bit ASCII
5. Repeat until all ASCII transmitted