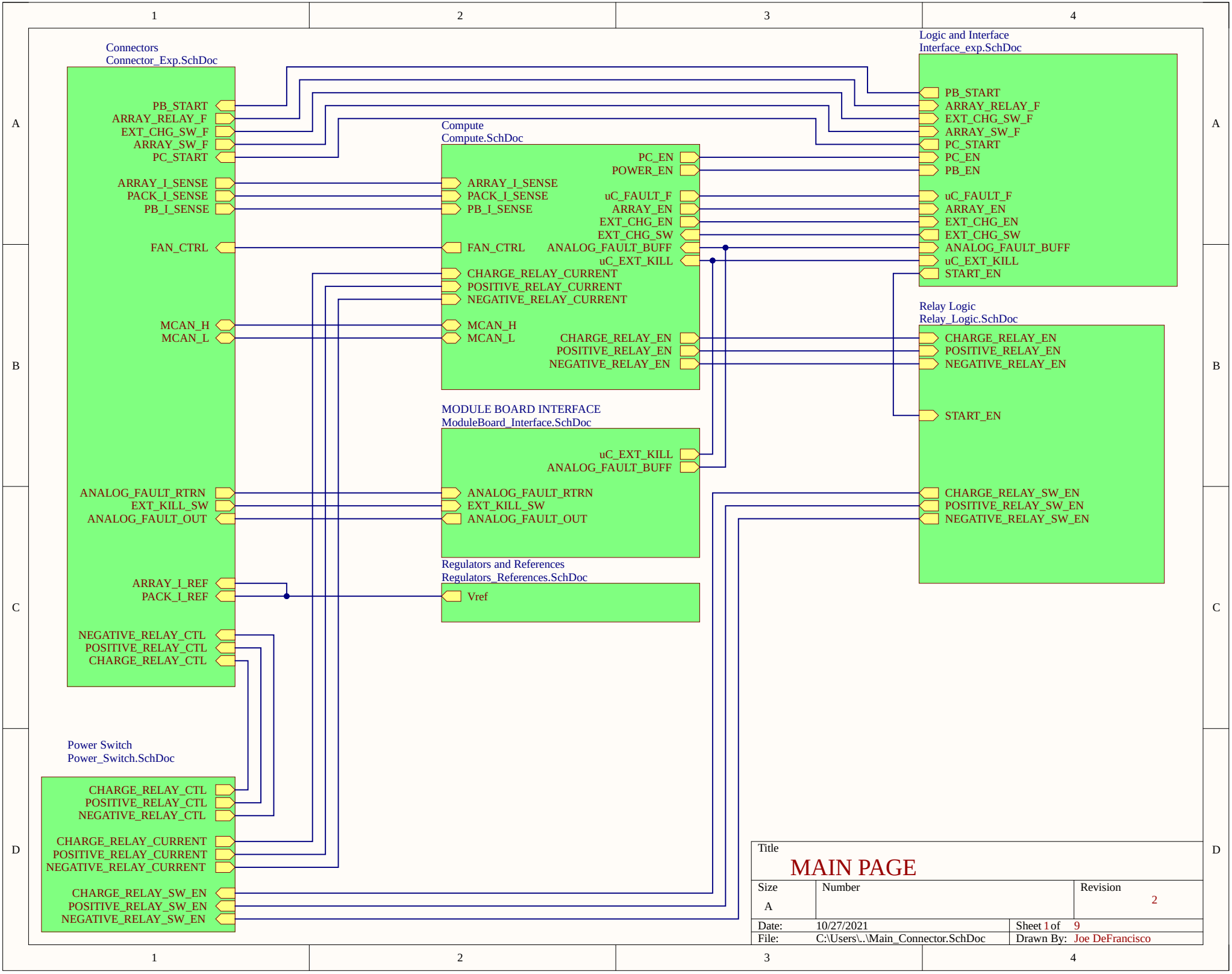
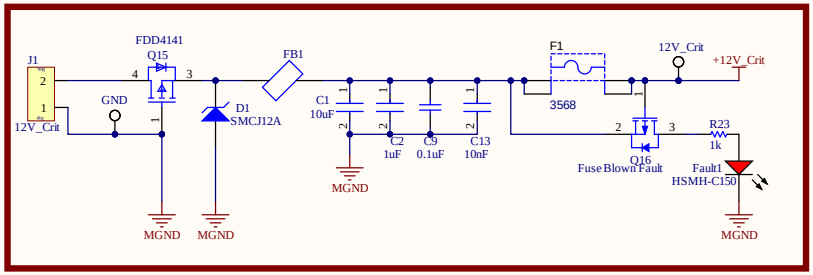
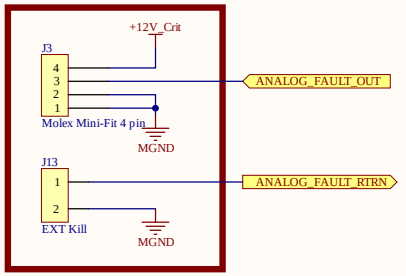

Connectors
Connector_Exp.SchDoc
PB_START
ARRAY_RELAY_F
EXT_CHG_SW_F
ARRAY_SW_F
PC_START
ARRAY_I_SENSE
PACK_I_SENSE
PB_I_SENSE
FAN_CTRL
MCAN_H
MCAN_L
ANALOG_FAULT_RTRN
EXT_KILL_SW
ANALOG_FAULT_OUT
ARRAY_I_REF
PACK_I_REF
NEGATIVE_RELAY_CTL
POSITIVE_RELAY_CTL
CHARGE_RELAY_CTL
Compute
Compute.SchDoc
PC_EN
POWER_EN
ARRAY_I_SENSE
PACK_I_SENSE
PB_I_SENSE
uC_FAULT_F
ARRAY_EN
EXT_CHG_EN
EXT_CHG_SW
FAN_CTRL
ANALOG_FAULT_BUFF
uC_EXT_KILL
CHARGE_RELAY_CURRENT
POSITIVE_RELAY_CURRENT
NEGATIVE_RELAY_CURRENT
MCAN_H
MCAN_L
CHARGE_RELAY_EN
POSITIVE_RELAY_EN
NEGATIVE_RELAY_EN
MODULE BOARD INTERFACE
ModuleBoard_Interface.SchDoc
uC_EXT_KILL
ANALOG_FAULT_BUFF
ANALOG_FAULT_RTRN
EXT_KILL_SW
ANALOG_FAULT_OUT
Regulators and References
Regulators_References.SchDoc
Vref
Logic and Interface
Interface_exp.SchDoc
PB_START
ARRAY_RELAY_F
EXT_CHG_SW_F
ARRAY_SW_F
PC_START
PC_EN
PB_EN
uC_FAULT_F
ARRAY_EN
EXT_CHG_EN
EXT_CHG_SW
ANALOG_FAULT_BUFF
uC_EXT_KILL
START_EN
Relay Logic
Relay_Logic.SchDoc
CHARGE_RELAY_EN
POSITIVE_RELAY_EN
NEGATIVE_RELAY_EN
START_EN
CHARGE_RELAY_SW_EN
POSITIVE_RELAY_SW_EN
NEGATIVE_RELAY_SW_EN
Power Switch
Power_Switch.SchDoc
CHARGE_RELAY_CTL
POSITIVE_RELAY_CTL
NEGATIVE_RELAY_CTL
CHARGE_RELAY_CURRENT
POSITIVE_RELAY_CURRENT
NEGATIVE_RELAY_CURRENT
CHARGE_RELAY_SW_EN
POSITIVE_RELAY_SW_EN
NEGATIVE_RELAY_SW_EN
Title
MAIN PAGE
Size
A
Number
Revision
2
Date: 10/27/2021
Sheet 1 of 9
File: C:\Users\..\Main_Connector.SchDoc
Drawn By: Joe DeFrancisco

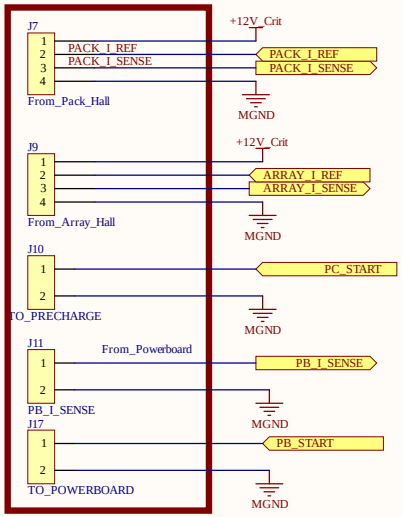
12V Critical



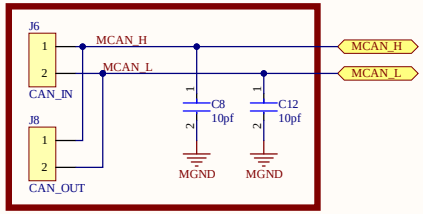
Module Board Interface



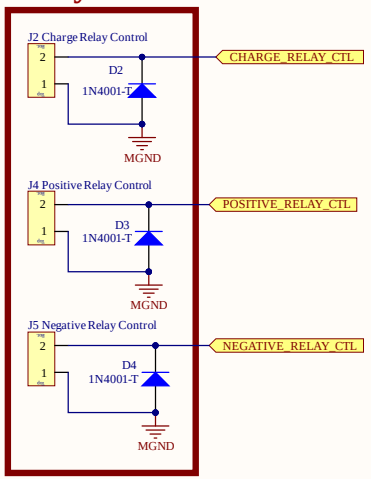
PB and PC Interface



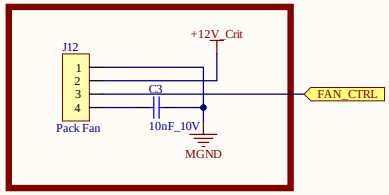
Main CAN



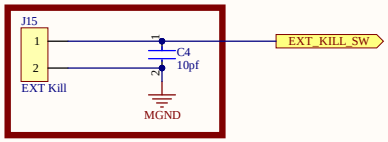
Relays



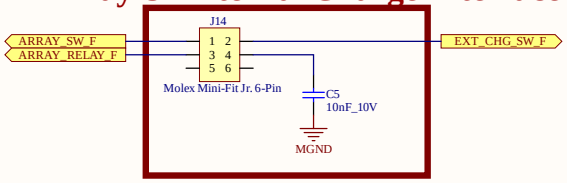
Pack Fans



EXTERNAL KILL



Array & External Charge Interface



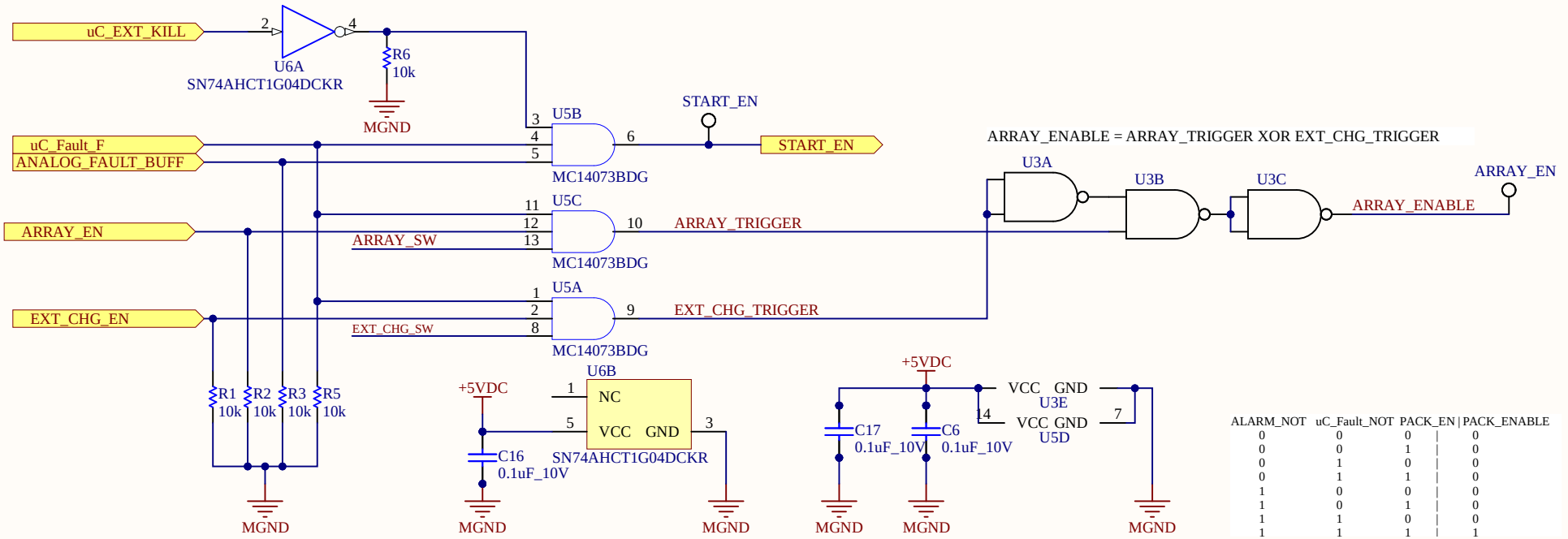
Notes

- J17 and J10 are buffered on precharge and powerboard

Title	Connectors		PRISUM
Size: A3	Number: *	Revision: 2	
Date: 10/27/2021	Time: 5:21:55 PM	Sheet 3 of 9	
File: C:\Users\Jake\OneDrive\Documents\College\Clubs\Solar Car\BPS\Headnode\Altium Project\Connector_Exp.SchDoc			

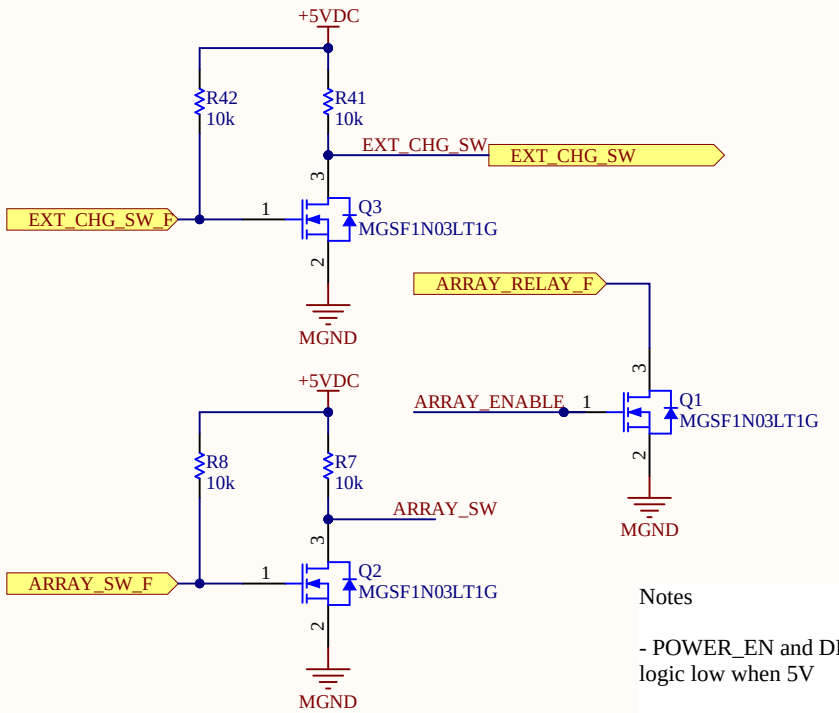
Altium

Array & External Charge Enable Logic

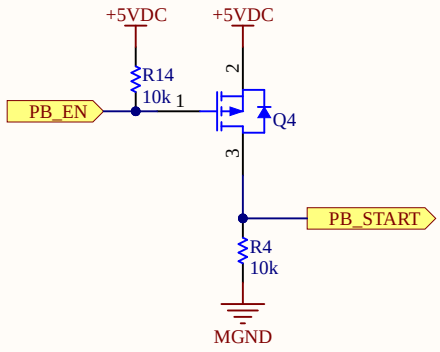


ALARM_NOT	uC_Fault_NOT	PACK_EN	PACK_ENABLE
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

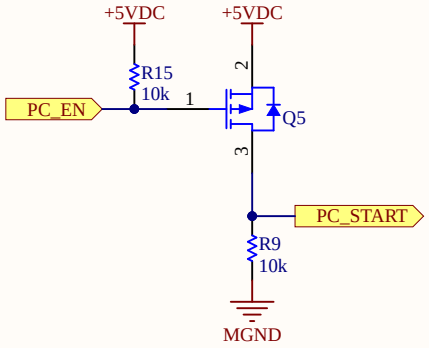
Array & External Charger Interface



To Powerboard



To Precharge



Notes

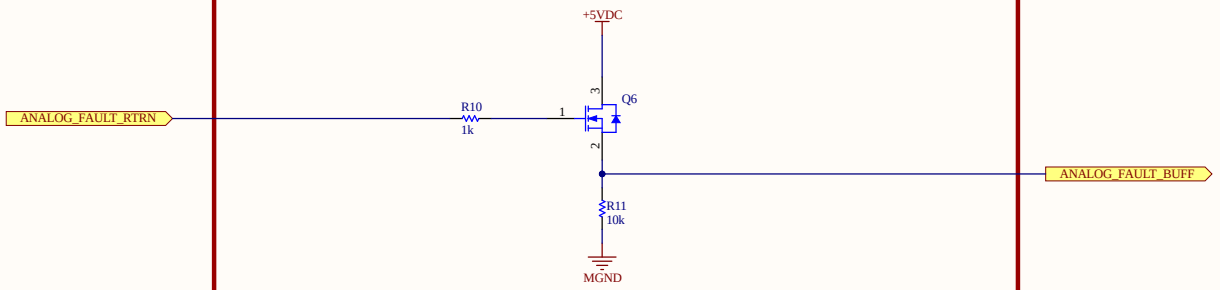
- POWER_EN and DRIVE_EN is logic high when 0V, logic low when 5V

Title: Interface		
Size: A	Number:	Revision: Rev5
Date: 10/27/2021		Sheet 2of 9
File: C:\Users\..\Interface_exp.SchDoc		Drawn By: Joe DeFrancisco

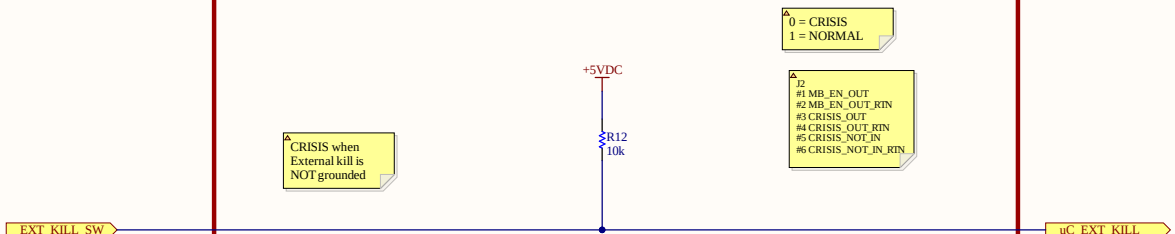
INPUT

FAULT LINE RECIEVER

OUTPUT



EXTERNAL KILL



FAULT LINE DRIVER

NOTES:

Fault Line Driver is a voltage source for the Analog Fault line that runs through the battery pack.
The wiring for the module board will need to be a single string. Current requirement should be small becuase on loop back to HN, it drives an NMOS gate.

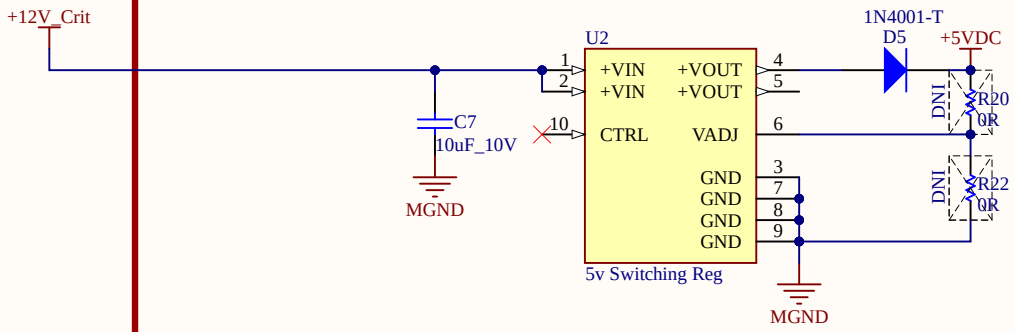
Title	***Module Board Interface***		
Size: B	Number:*	Revision:*	
Date: 10/27/2021	Time: 5:21:55 PM	Sheet 4 of 8	
File: C:\Users\Jake\OneDrive\Documents\College\Clubs\Solar Car\BPS\Headnode\Altium Project\ModuleBoard_Interface.SchDoc			

Altium

INPUT

5V REGULATOR

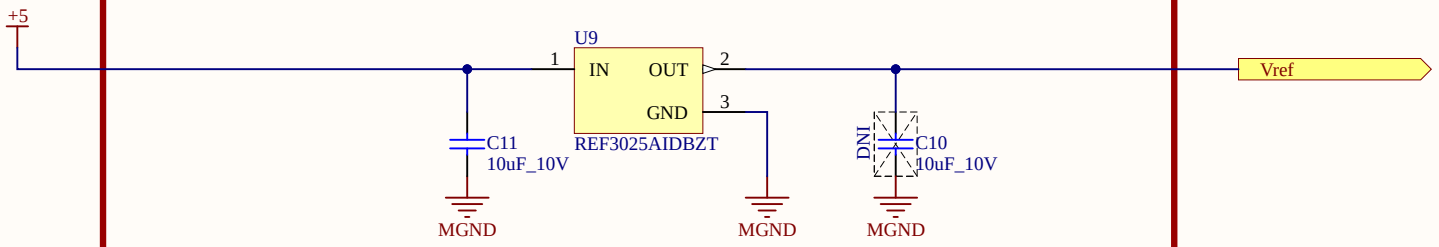
OUTPUT



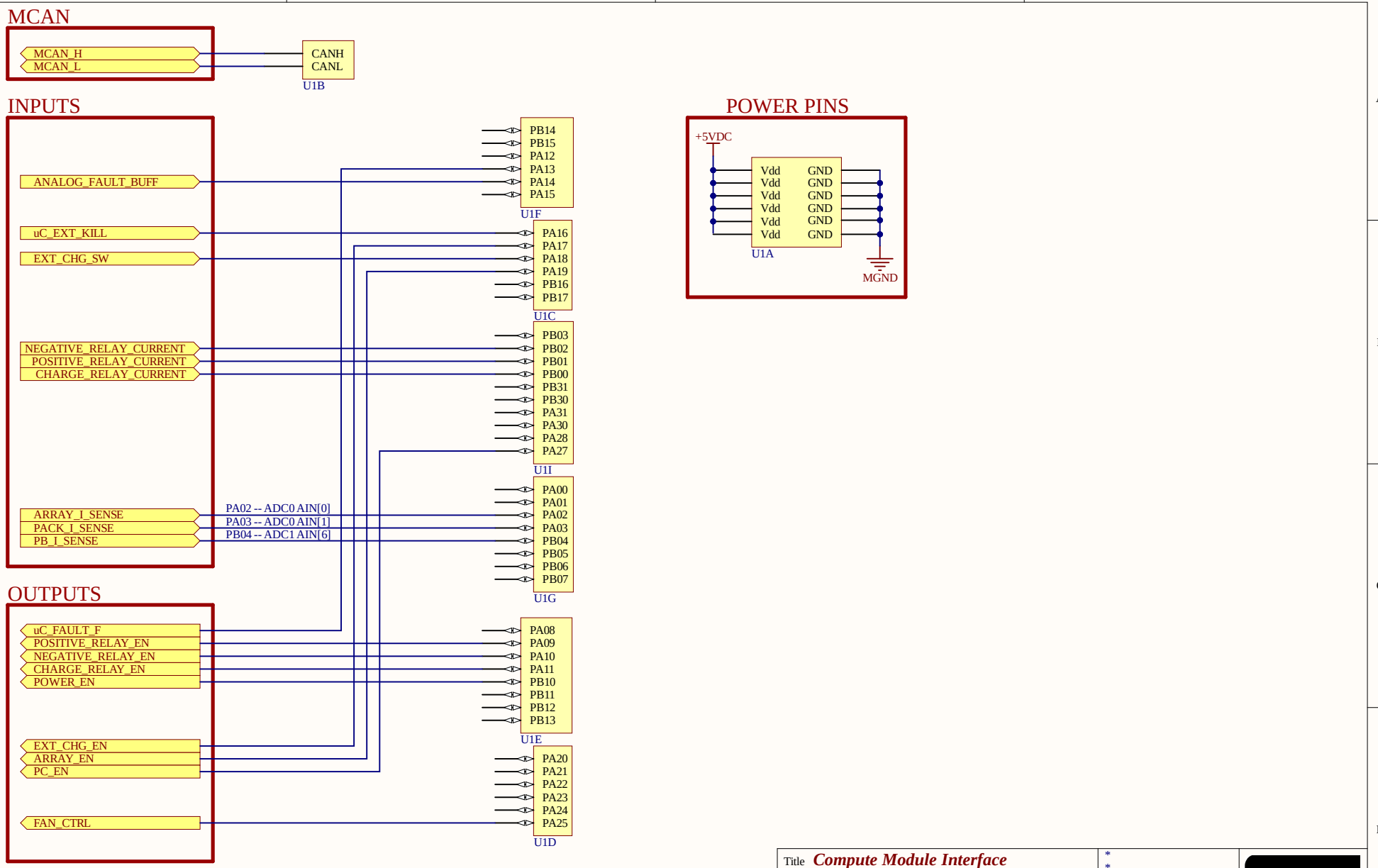
Notes

- R22 will be needed as a trim up resistor due to the voltage drop across D5. This can vary board to board so measure the output voltage without R20 or R22 soldered to see what voltage needs to be calculated to pull it up.

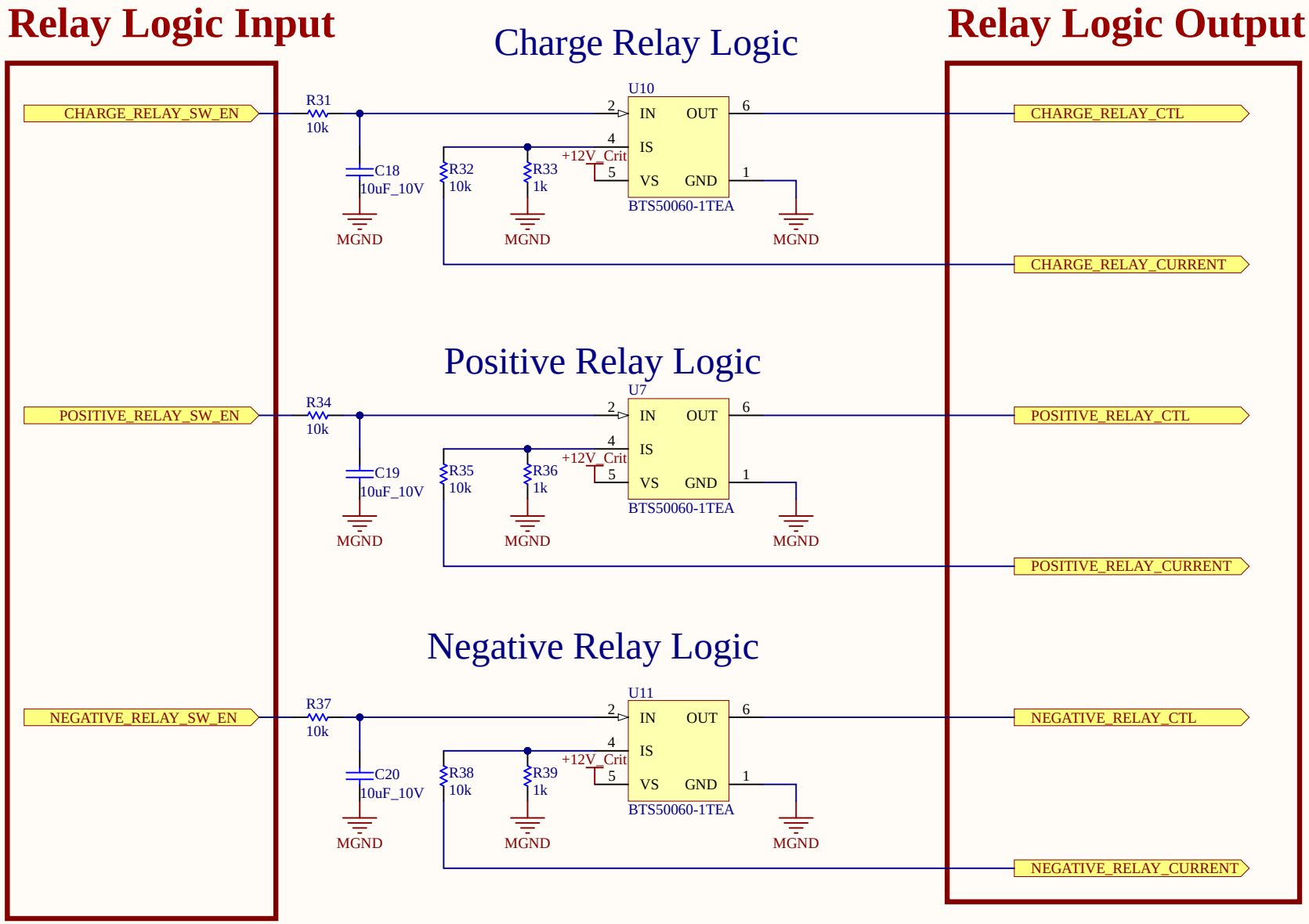
2.5V REFERENCE



Title	Voltage Regulators and ADC References	
Size: A	Number:	Revision:
Date: 10/27/2021	Sheet 6 of 9	
File: C:\Users\..\Regulators_References.SchDoc	Drawn By: Joe DeFrancisco	



Title	***Compute Module Interface***		
Size: A4	Number:*	Revision:*	
Date: 10/27/2021	Time: 5:21:56 PM	Sheet 6 of 8	
File: C:\Users\Jake\OneDrive\Documents\College\Clubs\Solar Car\BPS\Headnode\Altium Project\Compute.SchDoc			

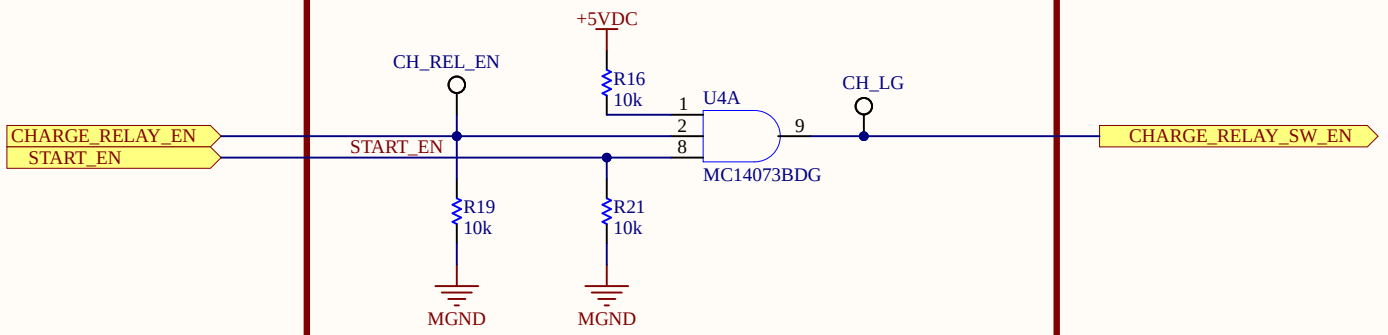


Title: Switch Relays		
Size: A	Number:	Revision:
Date: 10/27/2021		Sheet 8 of 9
File: C:\Users\..\Power_Switch.SchDoc		Drawn By: Jake Hafele

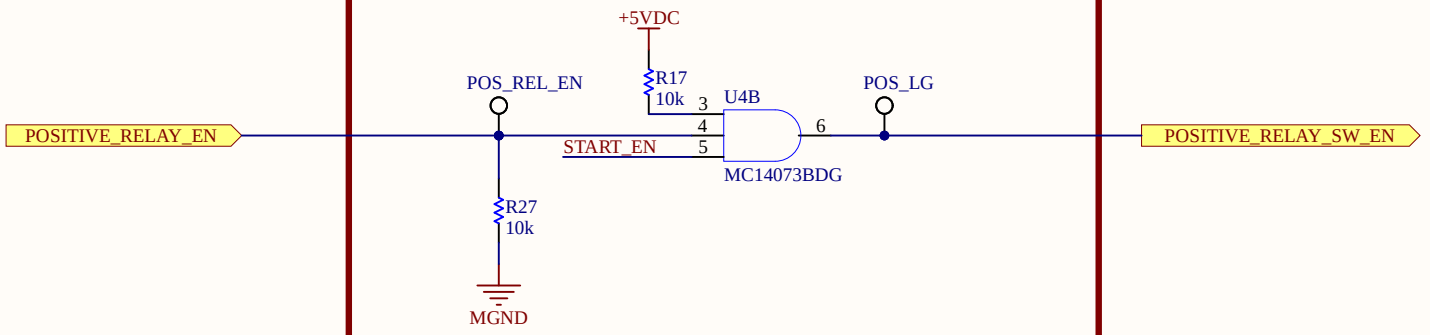
Relay Logic Input

Relay Logic Output

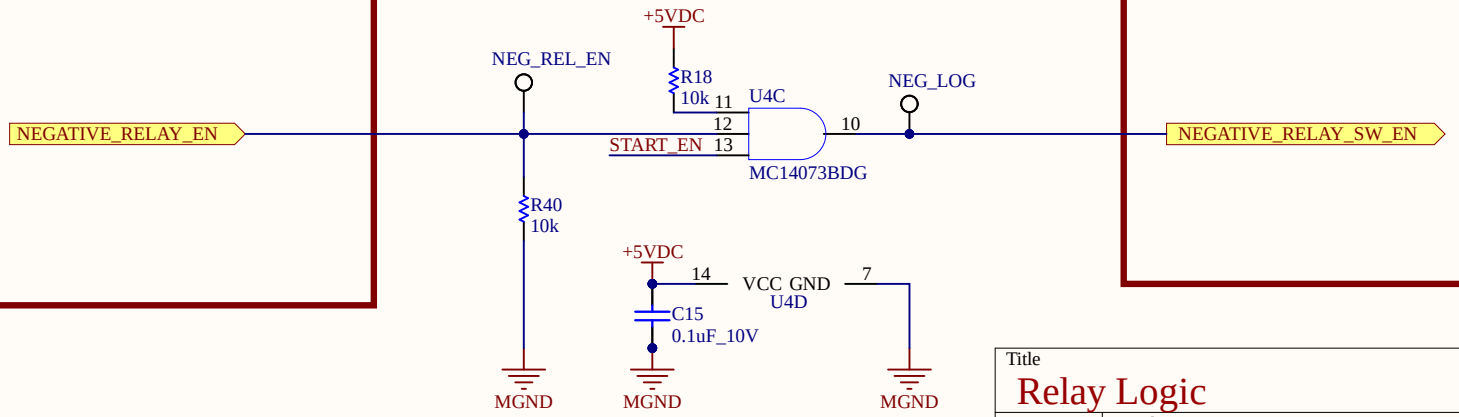
Charge Relay Logic



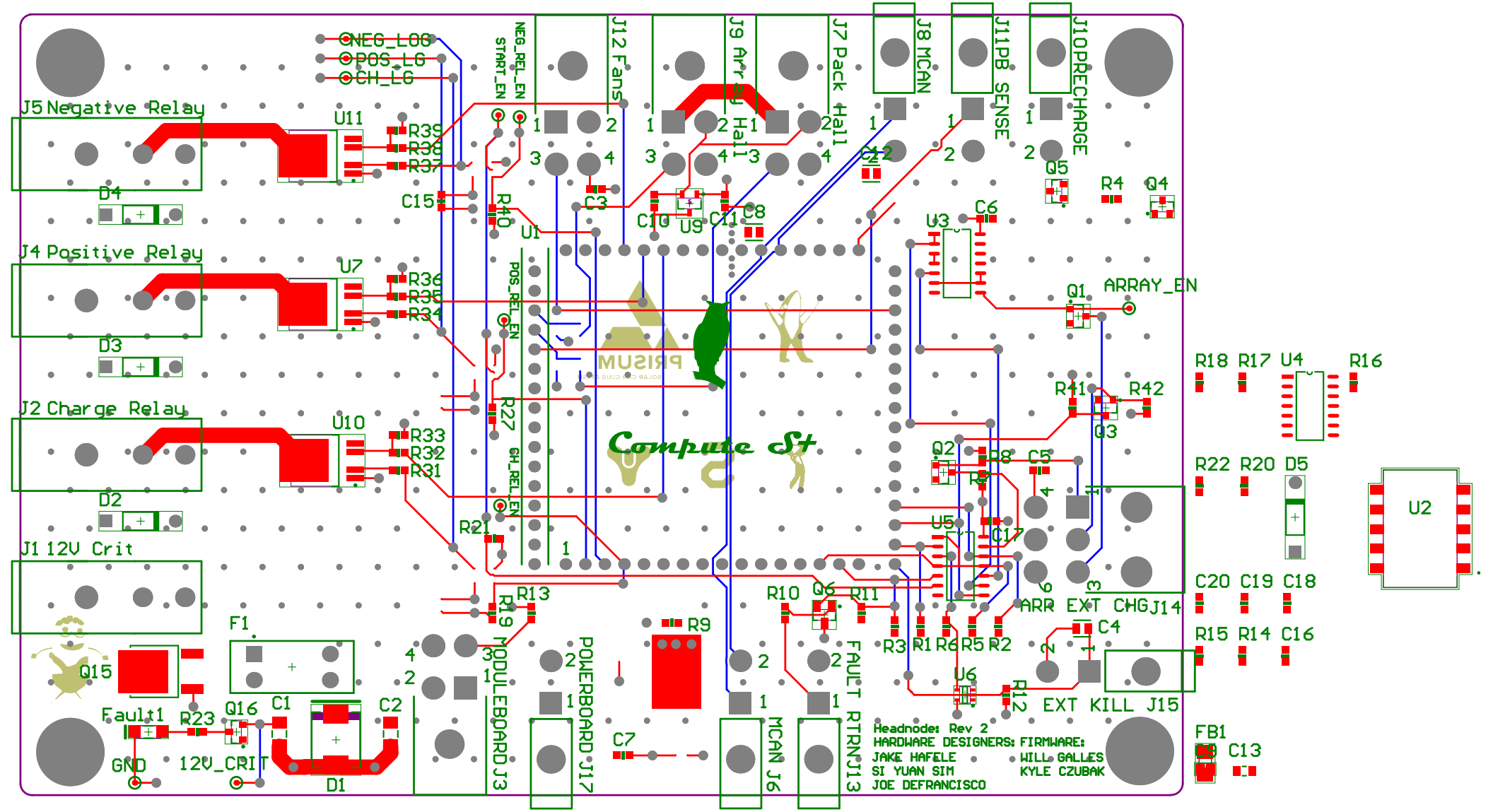
Positive Relay Logic



Negative Relay Logic



Title: Relay Logic		
Size: A	Number:	Revision:
Date: 10/27/2021		Sheet 9 of 9
File: C:\Users\..\Relay_Logic.SchDoc		Drawn By: Jake Hafele


NEG_LOG
POS_LG
CH_LG
J5 Negative Relay
J4 Positive Relay
J2 Charge Relay
J1 12V Crit
D4
D3
D2
U11
U7
U10
R39
R38
R37
R36
R35
R34
R33
R32
R31
C15
R40
U1
NEG_REL_EN
START_EN
POS_REL_EN
CH_REL_EN
R27
R21
J12 Fans
J9 Array Hall
J7 Pack Hall
C3
C10
U9
C11
C8
J8 MCAN
J11PB SENSE
J10PRECHARGE
C12
Q5
R4
Q4
U3
C6
Q1
ARRAY_EN
R41
R42
Q3
Q2
R8
C5
U5
C17
R18 R17 U4 R16
R22 R20 D5
U2
C20 C19 C18
R15 R14 C16
ARR EXT CHG J14
EXT KILL J15
C4
U6
R12
FB1
C13
R13
R19
R10
Q6
R11
R9
R3 R1 R6 R5 R2
F1
Q15
Fault1
R23
Q16
C1
C2
D1
GND
12V_CRIT
MODULEBOARD J3
POWERBOARD J17
MCAN J6
FAULT RTRN J13
C7
Headnode: Rev 2
HARDWARE DESIGNERS:
JAKE HAFELE
SI YUAN SIM
JOE DEFRANCISCO
FIRMWARE:
WILL GALLES
KYLE CZUBAK