

Jake Hafele

309-696-0228 | jakehafele1@gmail.com | www.linkedin.com/in/jake-hafele/ | <https://www.jakehafele.com>

OBJECTIVE

Seeking a full-time entry level position in FPGA design and/or verification starting May 2024.

EDUCATION

Iowa State University, College of Engineering

Bachelor of Science in Electrical Engineering

December 2023

GPA: 4.0/4.0

Master of Science in Computer Engineering

December 2024

University of Limerick Study Abroad Program

Spring 2022

EMPLOYMENT

Garmin, Design Engineer Intern - Olathe, KS

May 2023 – Present

- Designed a prototype power supply design using Cadence Allegro for GTS TCAS unit
- Determined load shed ratings to satisfy DO-160 Section 16 Power Input Requirements
- Modeled lightning suppression, surge suppression, voltage regulators, and comparator circuits in LTSpice

Iowa State University, Teaching Assistant - Ames IA

January 2021 – May 2023

- Taught labs for courses on Digital Logic, Embedded Systems 1, Heat Transfer, and Fluids
- Demonstrated best coding practices in Verilog and C to integrate designs for FPGAs and Microcontrollers
- Analyzed waveforms in ModelSim and real time embedded applications in Code Composer Studio

Collins Aerospace, Systems Engineer Intern - Cedar Rapids, IA

May 2022 – December 2022

- Updated documentation for the CH-47F Chinook platform that satisfied customer needs and requirements
- Verified software and hardware updates through a suite of system wide tests
- Inspected current and new subsystem designs that are integrated into the Chinook system
- Performed system verifications before software releases that ensured system integration met standards

SKILLS

Skills	FPGA Synthesis, Waveform Validation, Timing Analysis, Agile Workflow
Tools	Vivado, Quartus Prime, ModelSim, GTKWave, Git, Subversion, Code Composer Studio
Coding	Verilog, VHDL, C, MATLAB, Python, TCL

PROJECTS

Open-Source Digital ASIC Fabrication

- Designed a silicon proven open-source digital ASIC, with submission and fabrication through eFabless
- Utilized open-source tools such as GTKWave and OpenROAD to verify and layout Verilog designs
- Designed an SPI interface to improve risk mitigation against the provided Wishbone communication bus

Synthesized 5-Stage MIPS Processor

- Used ModelSim to design and validate a 5-stage MIPS processor in VHDL
- Performed timing analysis based on instruction count, maximum clock frequency, and cycles per instruction
- Synthesized MIPS processor and I/O using Quartus Prime for an Altera DE2-115 FPGA development board

Solar Car

- Lead the hardware battery protection project, which monitors the voltage, current, and temperature of 1,100+ lithium-ion batteries
- Mentored team members on PCB projects that interfaced with driver applications and safety critical controls
- Organized a standardized parts library with over 500 components that could be shared between 10+ PCBs

ACTIVITIES AND LEADERSHIP

- PrISum Solar Car Club – Electrical Team Manager
- Critical Tinkers – Leadership Cabinet
- The Engineering Ambassador and Mentor Program

HONORS

- Top 2% of Engineers in Class Award 2020 – 2023
- College of Engineering Dean's List 2019 – 2023