Reference Docs

Coding Standard for ELC 2137

Updated: February 7, 2020. Version: SystemVerilog 2017

This is the coding standard for programming Verilog code in ELC 2173 Digital Logic Lab. In addition to correctness of your code, you will also be graded based on this code standard. Not following these instructions will result in points being deducted.

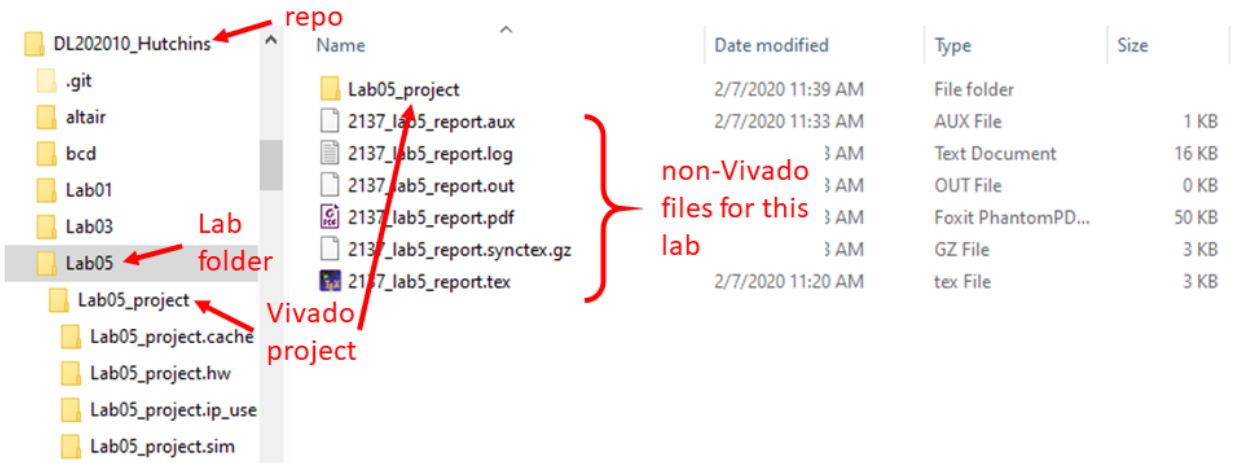
File Structure

Lab Folder

Your files should be organized in the following manner:

- Your repo will have a name like "DL202010_SomeName". I set this name when I create the repo on GitHub.
- Within this repo, you should have a folder for each lab. Name these folders as "LabXX" where XX is the lab number (e.g. Lab04 or Lab11).
- Within each lab folder, put your LaTeX report file and the assignment files I give you (except Verilog files, see below).
- When you create your Vivado project, have it create a folder under the lab folder and name it "LabXX_project".

You can see this structure in the following image:

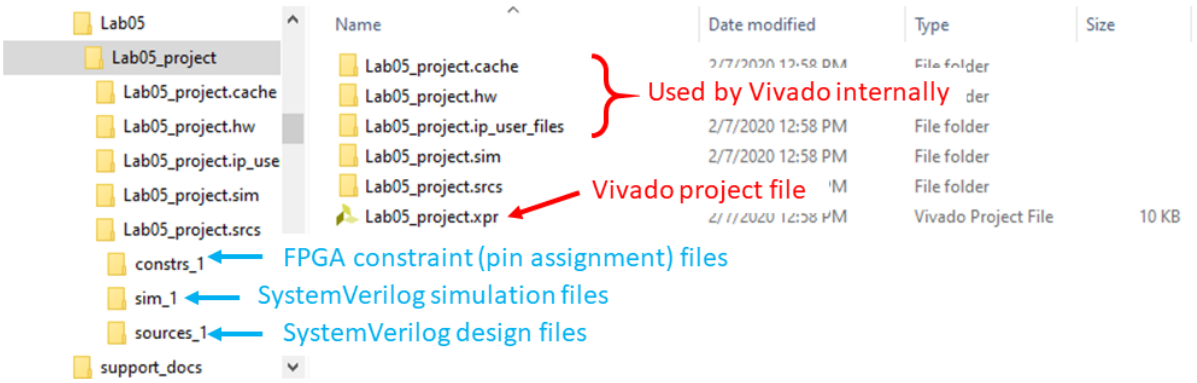


Vivado Project

Inside your Vivado project folder, you should have the following:

- All SystemVerilog design files (*.sv) shall be stored in a "sources_X" subfolder of the "LabXX_project.srcs" folder. All SystemVerilog simulation files (*.sv) dhall be stored in a "sim_X" subfolder of the "LabXX_project.srcs" folder.
- All simulation waveform configuration files (*.wcfg) shall be stored in the "LabXX_project.sim" folder. Screenshots of simulation waveforms can also be stored here.
- All constraint files shall be stored in a "constrs_X" subfolder of the "LabXX_project.srcs" folder.
- There should only be one .xpr file for each lab.
- The .xpr file shall be stored in the Vivado project's base directory.

Here is the proper structure of the Vivado project files:



Code Structure

Naming Conventions

Files

- Each assignment's project name should be "LabXX.xpr" where XX is the lab number (e.g. Lab04 or Lab11).
- Every file name should be the same as the module name.
  - For example, the module `fulladder` should be in a file named "fulladder.sv".
- File/module names should **not contain spaces**.

Simulations

- Create a new simulation set for each test you want to run. Give the set the same name as your testing file (see next).
- Within each simulation set, you should have only one Verilog test bench named as "<module to be tested>_test.sv".
  - For example, the test bench for `fulladder` should be named "fulladder_test.sv".
- There should be **no spaces** in any simulation set or test bench's name.

Code

- For `wire`, `reg`, `input`, `output` objects:
  - Use all lower case: `ain, bout`
  - Use underscore '_' if you want: `a_in, b_out`
- For `parameter`, `localparam` objects:
  - Use all upper case: `BITWIDTH, DATAREADY`
  - Use underscore '_' if you want: `BIT_WIDTH, DATA_READY`

Indentation

Indent code using one *tab* for each code block.

This is a bad indentation:

```
1  `timescale lns/lps
2
3  module fulladder_test;
4
5  reg a_in, b_in, cin;
6  wire cout, sum;
7
8  fulladder FA(.a(a_in), .b(b_in), .cin(cin), .cout(cout), .sum(sum));
9
10 initial
11 begin
12 {a_in, b_in, cin} = 3'b000; #5;
13 {a_in, b_in, cin} = 3'b001; #5;
14 {a_in, b_in, cin} = 3'b010; #5;
15 {a_in, b_in, cin} = 3'b011; #5;
16 {a_in, b_in, cin} = 3'b100; #5;
17 {a_in, b_in, cin} = 3'b101; #5;
18 {a_in, b_in, cin} = 3'b110; #5;
19 {a_in, b_in, cin} = 3'b111; #5;
20 $finish;
21 end
22
23 endmodule // fulladder_test
24
```

This is a good indentation:

```
1  `timescale 1ns/1ps
2
3  module fulladder_test;
4
5     reg a_in, b_in, cin;
6     wire cout, sum;
7
8     fulladder FA(.a(a_in), .b(b_in), .cin(cin), .cout(cout), .sum(sum));
9
10    initial
11      begin
12         {a_in, b_in, cin} = 3'b000; #5;
13         {a_in, b_in, cin} = 3'b001; #5;
14         {a_in, b_in, cin} = 3'b010; #5;
15         {a_in, b_in, cin} = 3'b011; #5;
16         {a_in, b_in, cin} = 3'b100; #5;
17         {a_in, b_in, cin} = 3'b101; #5;
18         {a_in, b_in, cin} = 3'b110; #5;
19         {a_in, b_in, cin} = 3'b111; #5;
20        $finish;
21      end
22
23 endmodule // fulladder_test
24
```