ELC 2137 Lab 3: Adder

Jake Simmons and Haonan Jin

February 4, 2020

Summary

In this lab, we first built a half adder and with it drew a schematic and wiring diagram. Then we tested it to see if its behaviour matched the half adder truth diagram. Next we built a full adder and with it drew a schemtaic and wiring diagram. Then we tested this one as well to see if its behaviour matched the full adder truth diagram. Lastly, we created a two bit adder. We did this by combining two full adders then checked to see if its behaviour matched the two bit adder truth table.

Q&A

1. Which gates could we use for combining the carry bits?
   (a) The gates we could use for combining the carry bits are XOR, AND Gates.
2. Which one should we use and why?
   (a) We should use the XOR Gate, because in binary when you add two ones together, the output will give you a zero with an one carried over. A XOR Gate, when inputted with two ones the output is zero which is same when you add two ones in binary. Also in a XOR Gate if one and zero is inputted a one is outputted which is the same when you add a one and zero in binary. If we were to use the AND Gate to add two binary numbers, one plus one would output one which in binary is not correct.

Results

Table1: Proof carry outputs of the first and second stage HAs cannot be high at the same time

Cin	A	B	C1	S1	C2	Cout	S
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	1	0	0	1
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	1	1	1	0
1	1	1	1	0	0	1	1

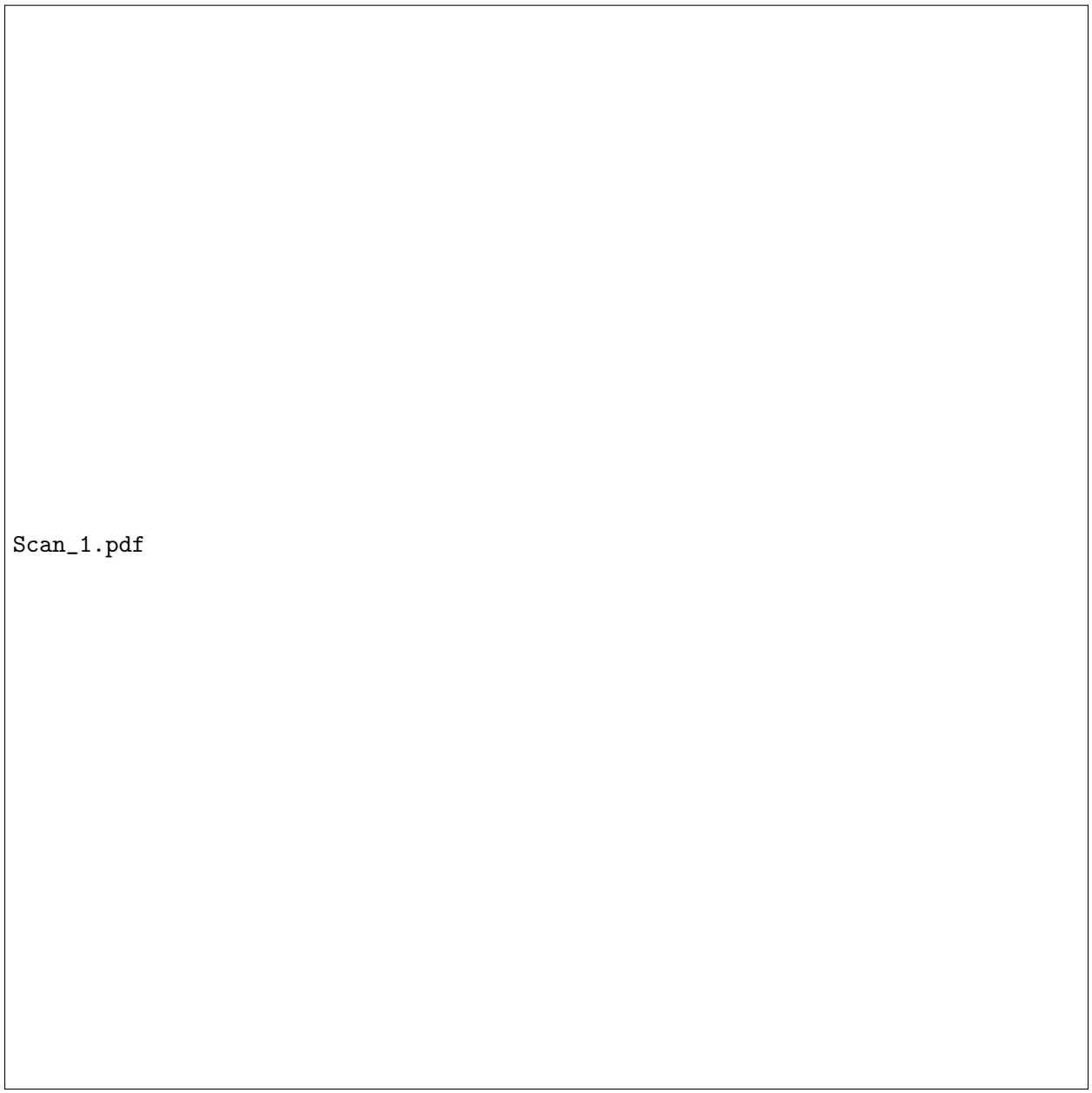

Figure 1: Schematics and Wiring Diagram of the Half and Full Adder

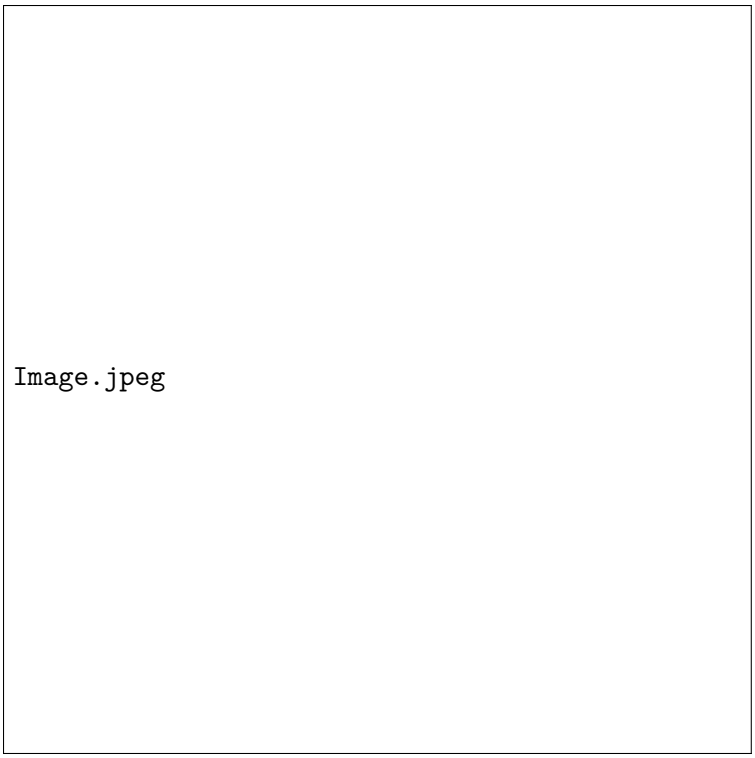

Figure 2: Picture of the Half Adder

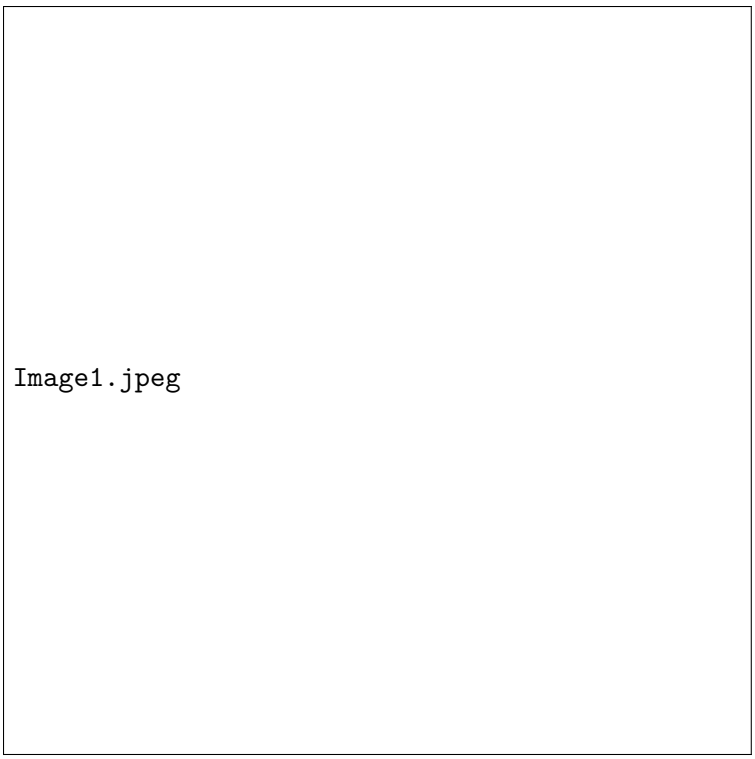

Figure 3: Picture of the Full Adder

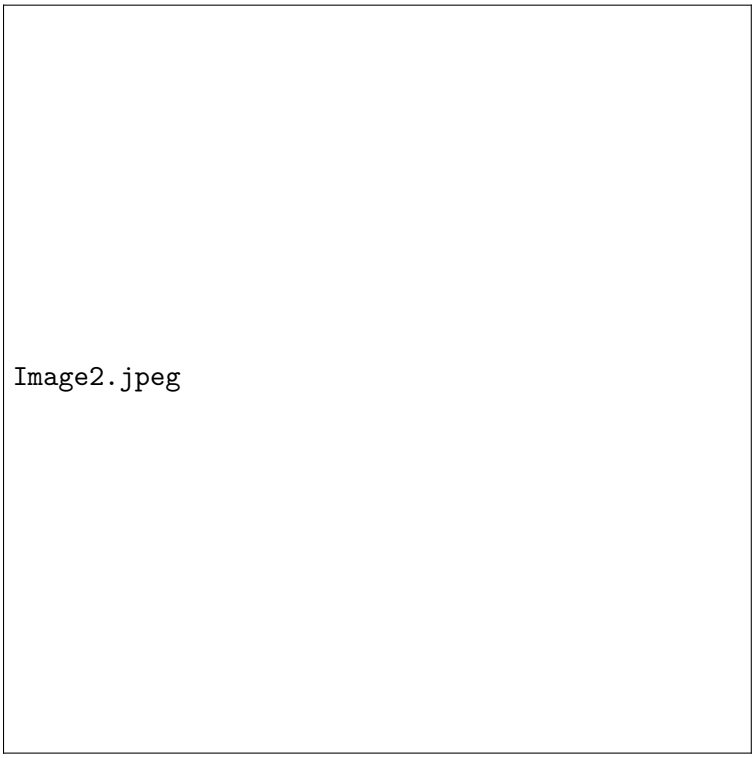

Figure 4: Picture of the 2-Bit Adder

Code