ELC 2137 Lab 4: Subtractor

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Summary

In this experiment we made a subtractor from a adder. First we made an adder by combining two full adders which is a two-bit adder. Then we added three XOR Gates, this was becasue we needed to invert two of our inputs to generate the 2's complement. The third XOR Gate inverted the carry out bit because Figure 3 shows that the carry out bit in our expected results was the opposite of what it should have been mathematically.

Q&A

1. Why did we use two full adders instead of a half adder and a full adder?

   We used two full adders instead of a half adder and a full adder becasue if we used a half adder and full adder we would not get all three outputs. We would lose the S2 and Cout outputs.

2. How many input combinations would it take to exhaustively test the adder/subtractor?

   It would take 16 combinations to exhaustively test the adder/subtractor.

3. Why were the combinations given in the truth table chosen?

   The combinations given in the truth table were chosen to show that using the 2's complement in binary to subtract numbers does not always work.

4. Do the results from your adder/subtractor match what you would expect from theory? Explain any discrepancies.

   The results from our adder/subtractor do not match what was expected from theory. This is becasue the actual adder/subtractor has 5 inputs while based on theory there are only four inputs. The 5th input is a carry in bit which when missing causes the carry out bit to be opposite in theory compared to the actual results.

Results

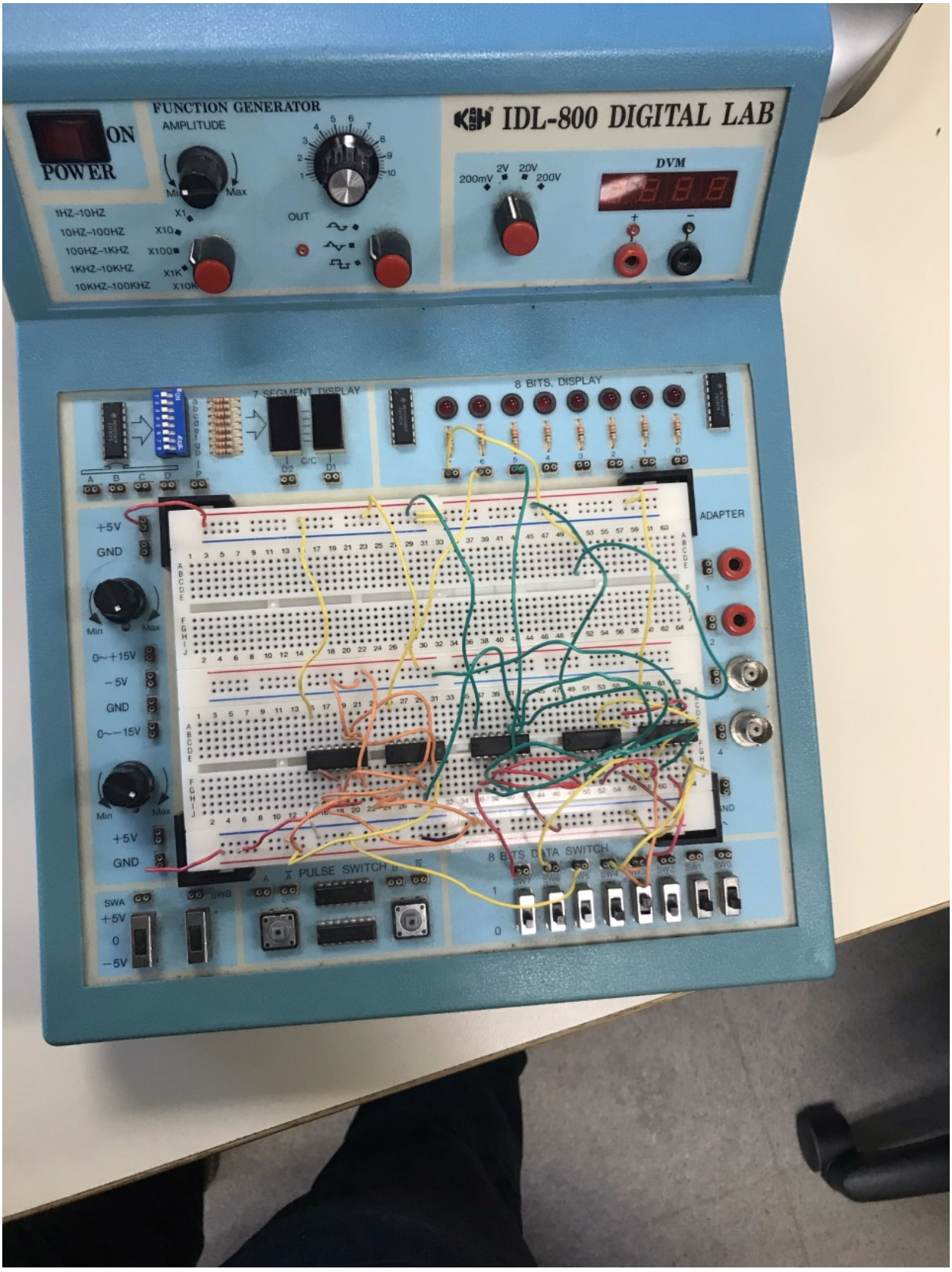

Figure 1: Picture of Assembled Circuit

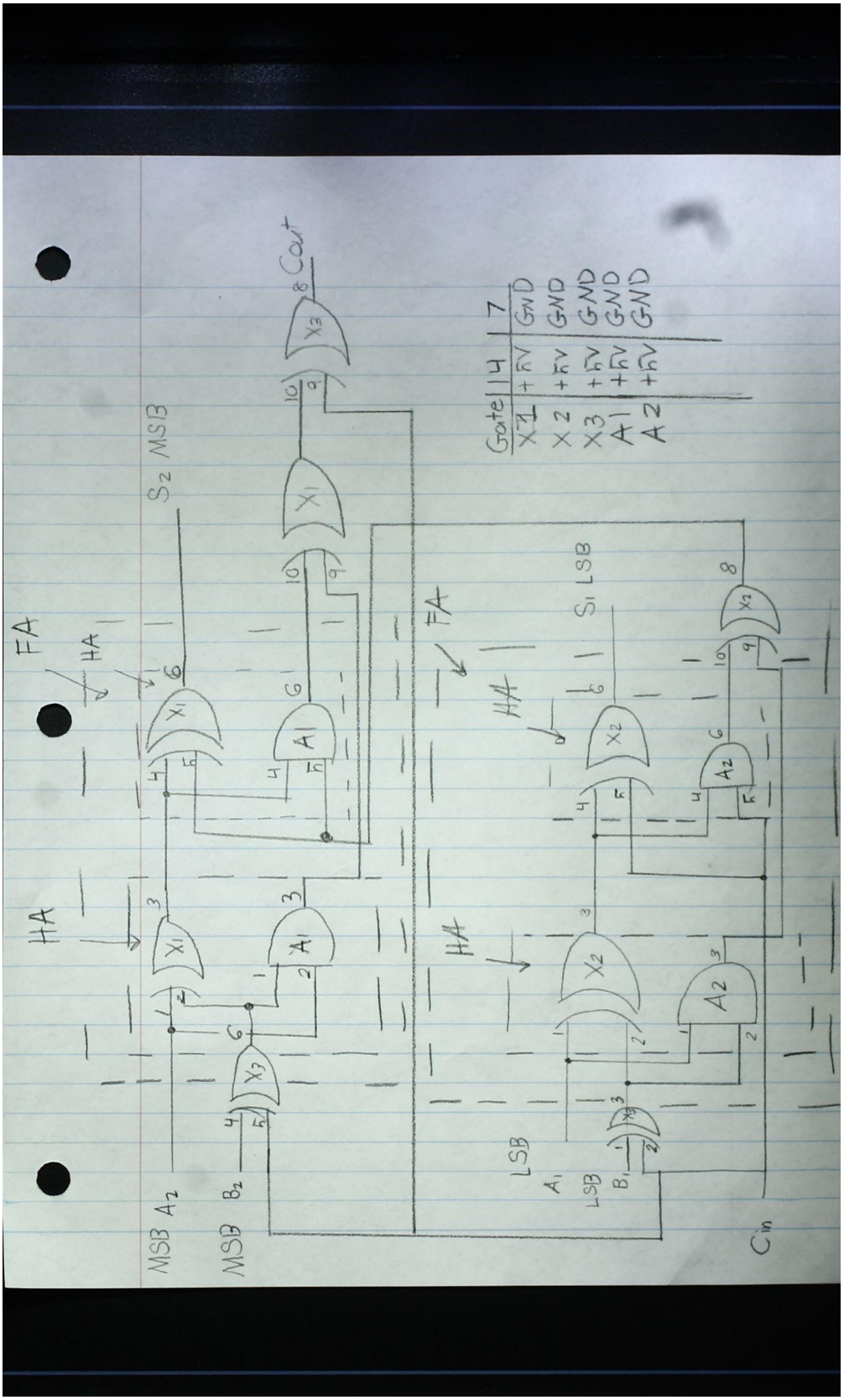

Figure 2: Two-Bit Adder/Subtractor Schematic

Circuit Demonstration Page

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Instructor Signatures

Separate Full Adders

Two-Bit Adder

Adder/Subtractor

Inputs		Expected Results			Actual Results
A	B	B 2's comp	Sub	Dec	Sub
00	01	11	011	3	111
00	10	10	010	2	110
00	11	01	001	1	101
01	01	11	100	-4	000
10	01	11	101	-3	001
10	00	00	110	-2	010

Figure 3: Circuit Demonstration Page

Code