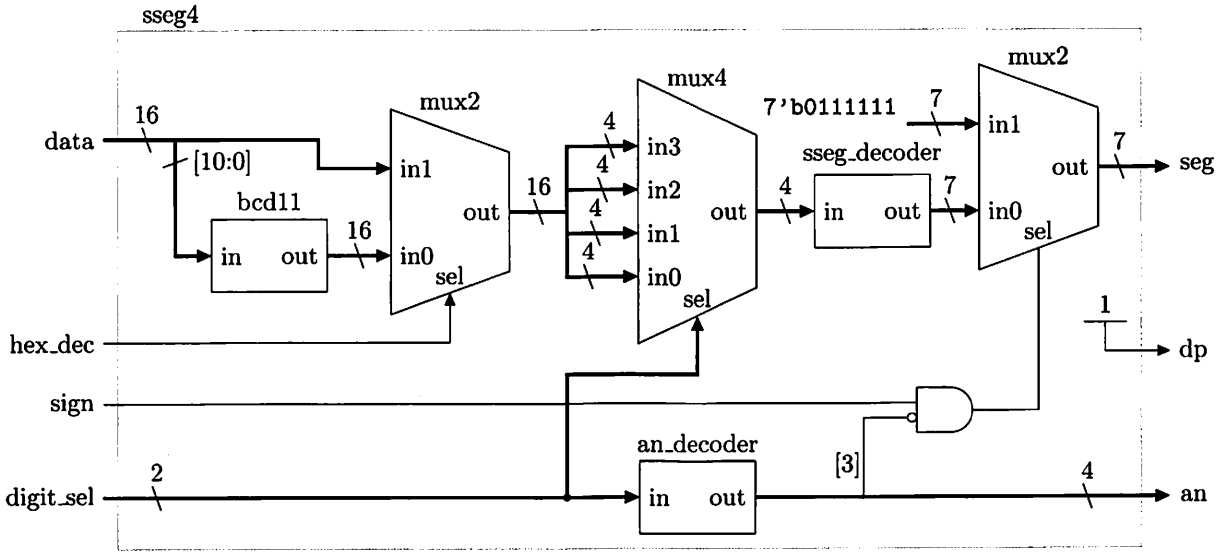

Figure 10.2: 4-digit 7-seg driver (**sseg4**) schematic repeated from Lab 8

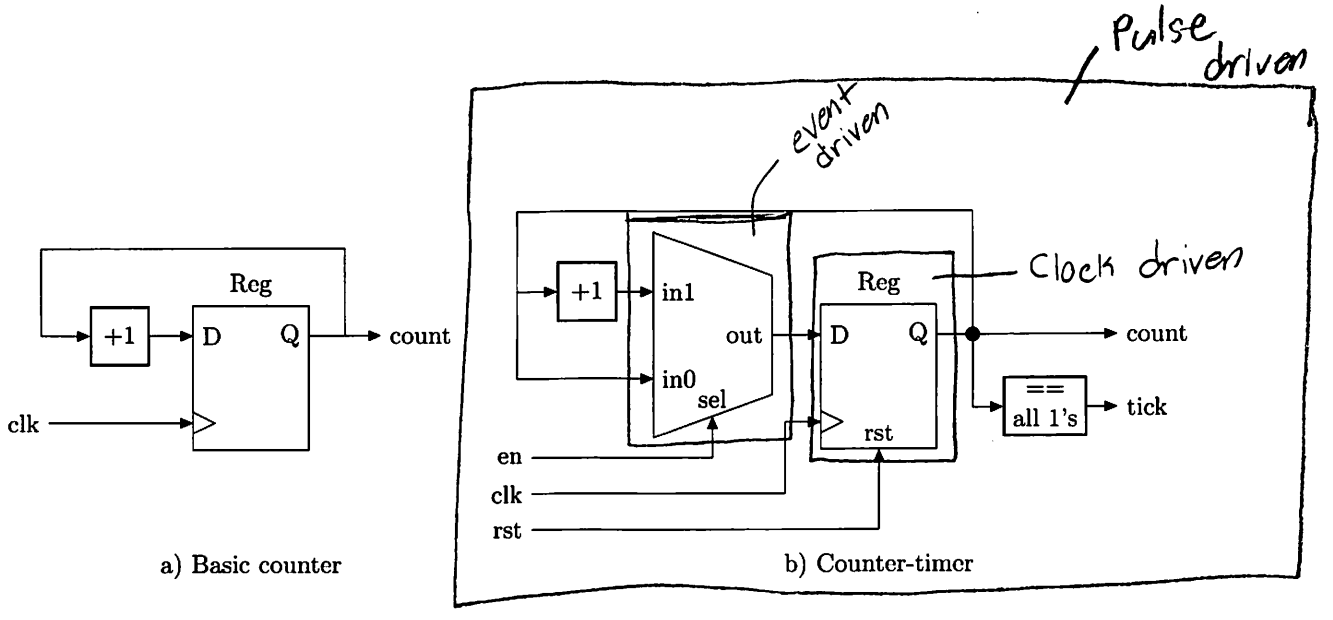

Figure 10.3: RTL schematics for a basic counter and our counter-timer