Discussion 13: I/O, ECC/Parity, RAID

I/O

1. Fill this table of polling and interrupts.

Operation	Definition	Pro / Good for…	Con / Bad for…
Polling	Checking a location at regular intervals for new input.	infrequent (i.e. slow input devices) data input devices with continual input that need sampling deterministic easy to write	frequent data input devices with high transfer rates but are rarely ready
Interrupts	A hardware location that interjects into the process to give new input	frequent data input	something that gives continual and needs to be sampled input since it would clog the processor has some overhead, so polling can be faster for slow, often ready devices. non deterministic requires additional hardware

2. Memory Mapped I/O
   Certain memory addresses correspond to registers in I/O devices and not normal memory.
   0xFFFF0000 – Receiver Control:
   Lowest two bits are interrupt enable bit and ready bit.
   0xFFFF0004 – Receiver Data:
   Received data stored at lowest byte.
   0xFFFF0008 – Transmitter Control
   Lowest two bits are interrupt enable bit and ready bit.
   0xFFFF000C – Transmitter Data
   Transmitted data stored at lowest byte.

   Write MIPS code to read a byte from the receiver and immediately send it to the transmitter.

```
lui t3 0xFFFF)
IO0:
lw t0 0(t3)
andi t1 t0 0x00000011
addi t2 0 0x00000011
bne t1 t2 IO0
lw t4 4(t3)

IO1:

lw t0 8(t3)
andi t1 t0 0x00000011
addi t2 0 0x00000011

bne t1 t2 IO1
sw t4 12(t3)
```

Hamming ECC

Recall the basic structure of a Hamming code. Given bits 1, . . . , m, the bit at position 2^n is parity for all the bits with a 1 in position n. For example, the first bit is chosen such that the sum of all odd-numbered bits is even.

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Data	P1	P2	D1	P4	D2	D3	D4	P8	D5	D6	D7	D8	D9	D10	D11
P1	X		X		X		X		X		X		X		X
P2		X	X			X	X			X	X			X	X
P4				X	X	X	X					X	X	X	X
P8								X	X	X	X	X	X	X	X

1. How many bits do we need to add to 0011_2 to allow single error correction?
   3
2. Which locations in 0011_2 would parity bits be included?
   1,2,
3. Which bits does each parity bit cover in 0011_2?
   1: 1,2,4 3: 2,3,42: 1,3
4. Write the completed coded representation for 0011_2 to enable single error correction.
   1000011_2
5. How can we enable an additional double error detection on top of this?
   If double error happens, the pairities won't add up.
   Wrong: add an additional parity bit over entire sequence
6. Find the original bits given the following SEC Hamming Code: 0110111_2
   0110011_2 -> 1011_2
7. Find the original bits given the following SEC Hamming Code: 1001000_2
   1001100_2 ->0100_2
8. Find the original bits given the following SEC Hamming Code: 010011010000110_2
   010011010100110
   -> 01100100110_2

RAID

Fill out the following table:

	Configuration	Pro / Good for…	Con / Bad for…
RAID 0	Splits data in stripes with no fault tolerance	Permormance No over head	reliability
RAID 1	Data is duplicated	when reliability is better that performance or storage efficiency fast read write, fast recovery	no fault tolerance wrong: high over head
RAID 2	Stripe data at the bit level and check with hamming code	high (theortical) data rate and reliability small overhead	performance redundant disk checks
RAID 3	Stripe data at the byte level and checked with parity	good for high data rates of long data chains small check information overhead	performance on randomly accessed memory
RAID 4	Striped data at the block level with parity disk	can support simultaneous reads from multiple disks	multiple reads from same disk writes can't be done synchonously since all parity in on one disk
RAID 5	Striped data at the block level with parity distributed between disks	Long lifetime since the parity stress is distributed	Performance not as good as Raid 0