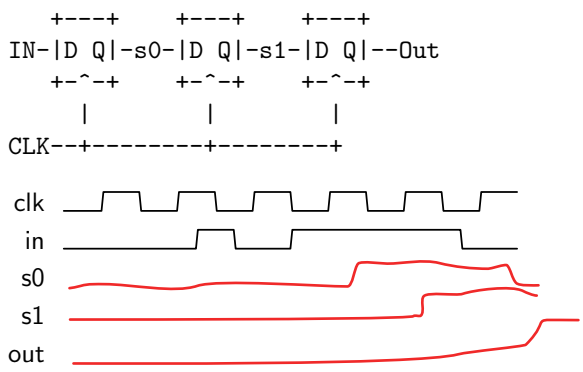
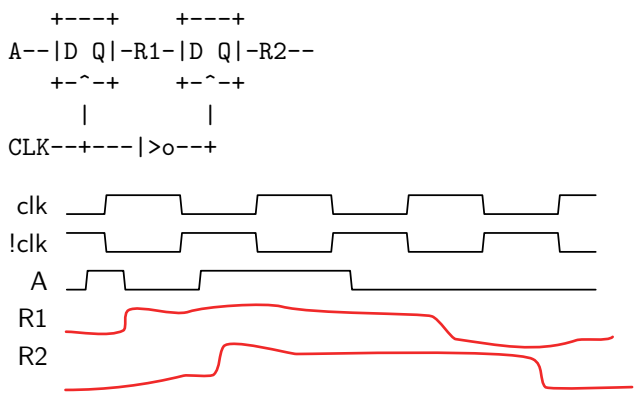
State

1. Fill out the timing diagram for the circuit below:

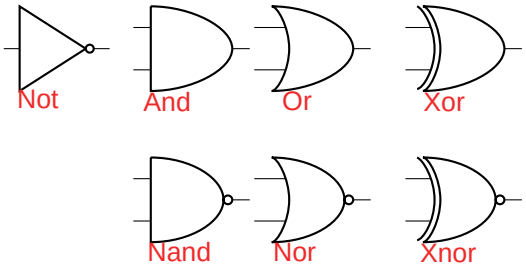


2. Fill out the timing diagram for the circuit below:



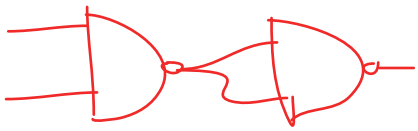
Logic Gates

1. Label the following logic gates:



2. Convert the following to boolean expressions:
   (a) NAND — A* + AB*
   (b) XOR — AB* + A*B
   (c) XNOR — AB + A*B*

3. Create an AND gate using only NAND gates.



4. How many different two-input logic gates can there be? How many n-input logic gates?

2(n+1) ... or 2^2^n depending on your definition of different

Boolean Logic

$1 + A = 1$	$A + \bar{A} = 1$	$A + AB = A$	$(A + B)(A + C) = A + BC$
$0B = 0$	$B\bar{B} = 0$	$A + \bar{A}B = A + B$	
DeMorgan's Law:	$\overline{AB} = \bar{A} + \bar{B}$	$\overline{A + B} = \bar{A}\bar{B}$	

1. Minimize the following boolean expressions:

   (a) Standard: $(A + B)(A + \bar{B})C$

   (A + BB*)C
   (A + 0)C
   AC

   (b) Grouping & Extra Terms: $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C} + ABC + A\bar{B}C$

   (A* + A)B*C* + (A* + A)BC*) + A(BC + B*C)
   B*C* + BC* + ACC* + AC
   C* + A

   (c) DeMorgan's: $\overline{A(\bar{B}\bar{C} + BC)}$

   A* + (B*C* + BC)*
   A* + (B*C*)*(BC)*
   A* + (B** + C**)(B* + C*)
   A* + (B + C)(B* + C*)A* + B(B* + C*) + C(B* + C*)
   A* + BC* + B*C