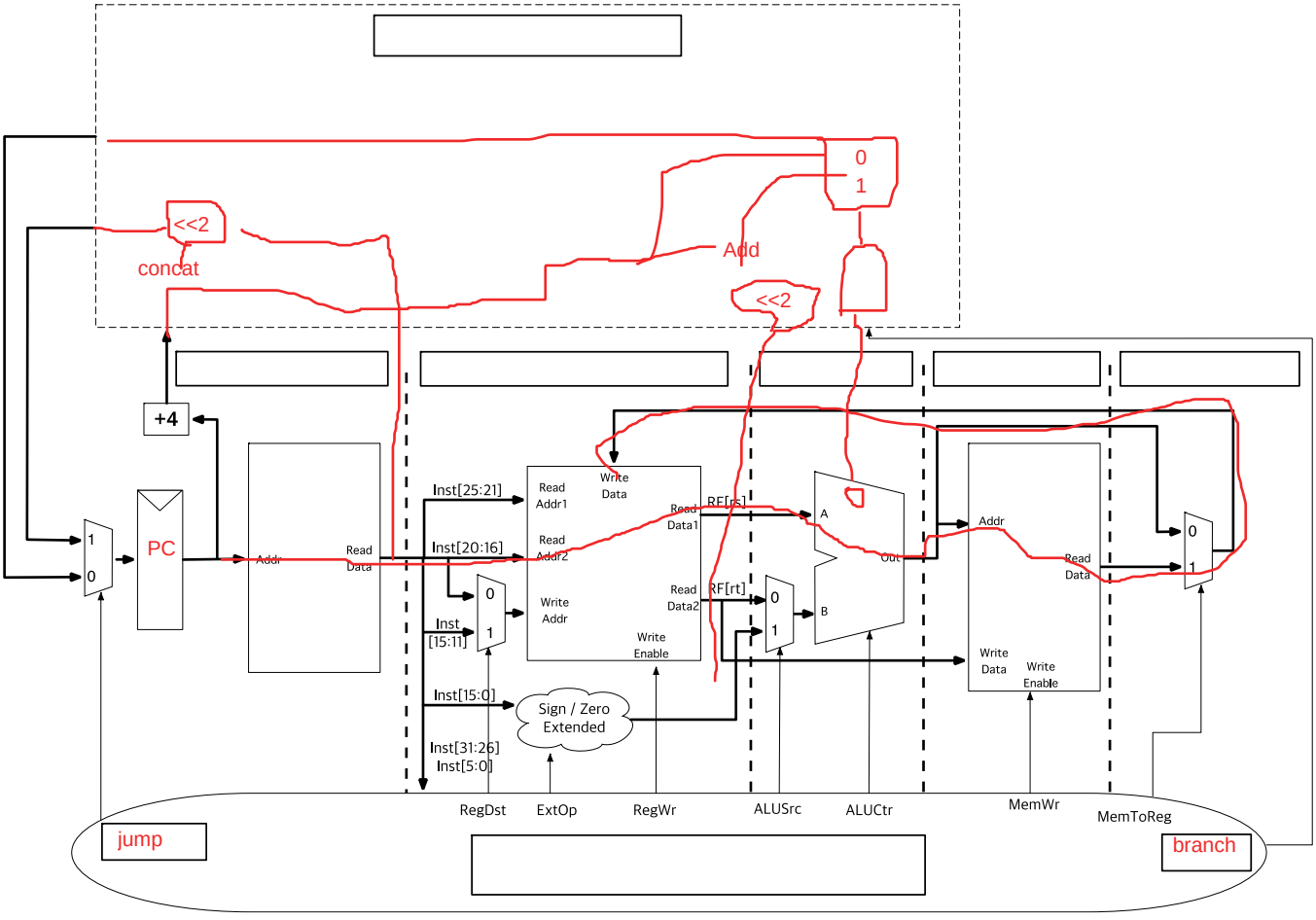
Single Cycle CPU Design

Here we have a single cycle CPU diagram. Answer the following questions:

1. Name each component.
2. Name each datapath stage and explain its functionality.

Stage	Functionality
Load instruction [S] Instruction fetch	Takes in machine code from memory, generates control signals, increments pc [S] Send address to instruction memory, read instruction
load registers [S] Decode, register read	loads in registers, immediate [S]generate control signals from opscode and funct, populate registers with rs/rt sign extend immediates
alu [S] execute	perform arithmatic [s] perform arithmatic and logic functions
writes to register	store output into registers [s] read from and write to memory
write to memory [s] write register	writes information in registers to memory [s] writes back the alu result and load memory to register

3. Provide data inputs and control signals to the next PC logic.
4. Implement the next PC logic.



Single Cycle CPU Control Logic

Fill out the values for the control signals from the previous CPU diagram.

Instrs.	Control Signals								
	jump	branch	RegDst	ExtOp	ALUSrc	ALUCtr	MemWr	MemtoReg	RegWr
add	0	0	1	-	0	0010	0	0	0
ori	0	0	0	0	1	0001	0	0	1
lw	0	0	-	1	1	0010	0	1	1
sw	0	0	-	1	1	0010	1	-	0
beq	0	1	-	1	0	0110	0	-	0
j	1	-	-	-	-	-	0	-	0

This table shows the ALUCtr values for each operation of the ALU:

Operation	AND	OR	ADD	SUB	SLT	NOR
ALUCtr	0000	0001	0010	0110	0111	1100

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- $t_{clk} \geq t_{clk\text{-}to\text{-}q} + t_{CL} + t_{setup}$, where t_{CL} is the critical path in the combinational logic.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

Element	Register clk-to-q	Register Setup	MUX	ALU	Mem Read	Mem Write	RegFile Read	RegFile Setup
Parameter	$t_{clk\text{-}to\text{-}q}$	t_{setup}	t_{mux}	t_{ALU}	$t_{MEMread}$	$t_{MEMwrite}$	t_{RFread}	$T_{RFsetup}$
Delay(ps)	30	20	25	200	250	200	150	20

1. What instruction exercises the critical path?

lw

2. What is the critical path in the single cycle CPU?

mem read

3. What are the minimum clock cycle, t_{clk}, and the maximum clock frequency, f_{clk}?

300ps or 3.33Ghz

4. Why is a single cycle CPU inefficient?

Because use are using each part of the process individually

5. How can you improve its performance?

By splitting each process up into a separate clk cycles