Assignment-1

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A) CMOS Inverter using IC 4007

Aim

a) To build a NOT gate using CMOS IC 4007 chip.

b) Plot the readings of V_{out} and V_{in} to obtain high and low noise margin of gate.

Apparatus

1. Breadboard
2. IC Chip 4007
3. Potentiometer
4. Oscilloscope
5. Wire
6. Wire cutter
7. Tweezer

Theory

The IC 4007 contains complementary pairs of PMOS and NMOS transistors. When you connect pins 1–5 (output), pin 3 (input), pin 2 (V_{dd}), and pin 4 (ground), you create a **CMOS inverter**:

- PMOS transistor connects between V_{dd} and output.
- NMOS transistor connects between output and ground.
- Both transistor gates connect to the input.

1. **Input LOW (0V):** PMOS turns ON, NMOS turns OFF → Output connects to V_{dd} = HIGH.
2. **Input HIGH (V_{dd}):** PMOS turns OFF, NMOS turns ON → Output connects to ground = LOW.

This perfect complementary switching creates a NOT gate with zero static power consumption and full voltage swing between 0V and V_{dd}.

Noise margin is the **maximum allowable noise voltage** that won't cause incorrect output. There are two types:

- High Noise Margin (NM_H): For HIGH input levels.
- Low Noise Margin (NM_L): For LOW input levels.

0.1 Steps to find noise margin

0.1.1 Step 1: Plot Voltage Transfer Characteristic (VTC)

- X-axis: V_{in} (0V to V_{dd})
- Y-axis: V_{out}
- Slowly vary V_{in} from 0V to V_{dd} while measuring V_{out}.

0.1.2 Step 2: Identify Critical Points from VTC Graph

1. V_{OH}: Output HIGH voltage (when V_{in} is LOW).
2. V_{OL}: Output LOW voltage (when V_{in} is HIGH).
3. V_{IH}: Minimum input voltage recognized as HIGH.
4. V_{IL}: Maximum input voltage recognized as LOW.

0.1.3 Step 3: Calculate Noise Margins

$$NM_H = V_{OH} - V_{IH} \quad \text{(High noise margin)}$$
$$NM_L = V_{IL} - V_{OL} \quad \text{(Low noise margin)}$$

- V_{IH}: Where slope $\left(\frac{dV_{\text{out}}}{dV_{\text{in}}}\right) = -1$ in HIGH-to-LOW transition region.
- V_{IL}: Where slope $\left(\frac{dV_{\text{out}}}{dV_{\text{in}}}\right) = -1$ in LOW-to-HIGH transition region.

Procedure

1. Insert IC 4007 into breadboard straddling the center gap.
2. Pin 2 (V_{dd}) $\rightarrow$ +5V supply (red wire).
3. Pin 4 (Ground) $\rightarrow$ 0V/GND supply (black wire).
4. **Input Signal:** Pin 3 $\rightarrow$ Input signal source.
5. **Output signal:** Short pins 1 and 5 together with a jumper wire.
6. Connect measurement device to pins 1–5.
7. Use potentiometer supply for V_{in}.
8. Measure V_{out} with oscilloscope.
9. Plot V_{out} vs V_{in} to get VTC curve.
10. Draw tangent lines with slope $= -1$ to find V_{IH} and V_{IL}.
11. Read V_{OH} (V_{out} at $V_{\text{in}} = 0V$) and V_{OL} (V_{out} at $V_{\text{in}} = V_{dd}$).
12. Calculate using formulas above.

Circuit Diagram

Observations

V_{in}	V_{out}
0	5
0.5	5
1	5
1.5	5
2	5
2.285	4.78
2.5	4.58
2.675	4.18
2.985	0.62
3.125	0.34
3.5	0.145
3.625	0.075
4	0
4.5	0
5	0

Table 1: Measured Data

From the graph plotted , we obtain values of $V_{IL} \approx 2.6V$ and $V_{IH} \approx 3.2V$

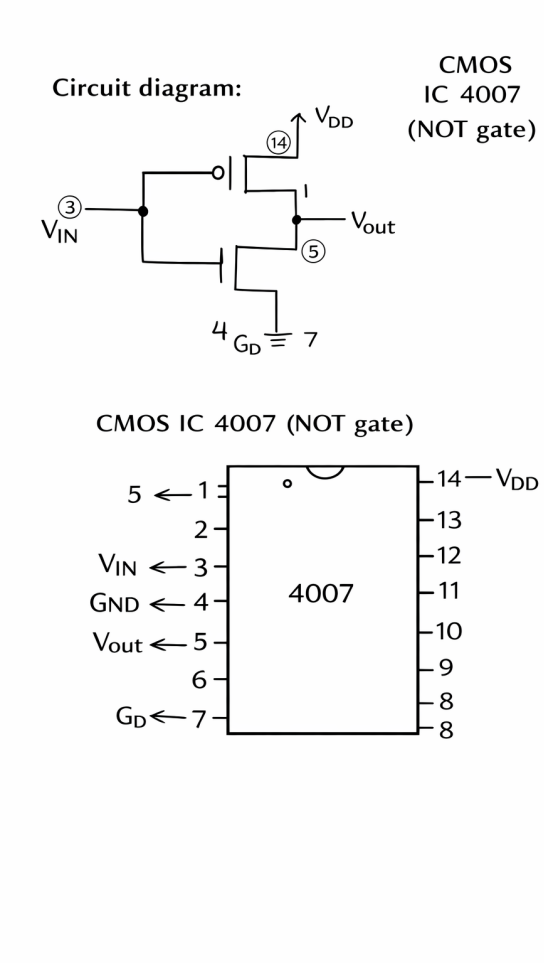

Figure 1: CMOS IC 4007 configured as a NOT gate

0.2 High noise margin

$$N_{MH} = V_{OH} - V_{IH}$$
$$N_{MH} = V_{DD} - V_{IH}$$
$$N_{MH} = 5 - 3.2$$
$$N_{MH} = 1.8V$$

0.3 Low noise margin

$$N_{ML} = V_{IL} - V_{OL}$$
$$N_{ML} = 2.6 - 0$$

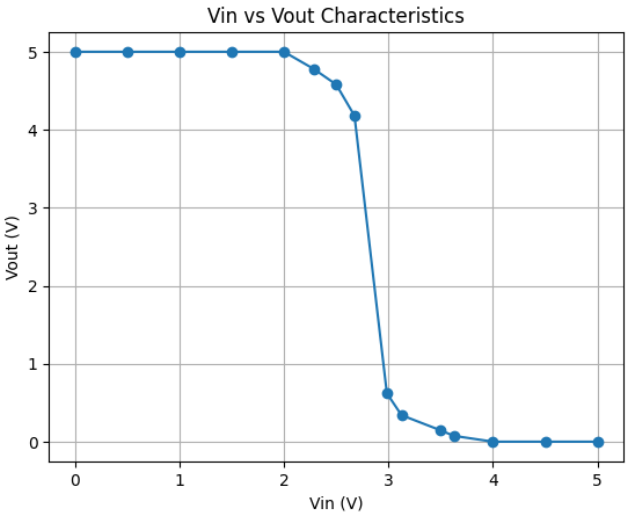

Figure 2: VTC graph

$$N_{ML} = 2.6V$$

Result

We were able to realize a CMOS inverter using the IC 4007. The high noise marin is 1.8 V and the low noise margin is 2.6 V , this indicates a good noise immunity.

Precautions

- The IC must straddle the center gap of the breadboard.
- No two pins on the same side of the IC should share a breadboard row.
- Bridge the rails explicitly with jumpers at splits.
- Make sure wires are placed correctly into breadboard.

B) CMOS NAND and NOR Gates using IC 4007

Aim

To realize a 3-input CMOS NAND gate and a 3-input CMOS NOR gate using the IC 4007 and to verify their truth tables.

Apparatus Required

- IC 4007 (CMOS transistor array)
- Breadboard
- DC power supply (5 V)
- Jumper wires
- input wires

Theory

In CMOS logic, digital gates are implemented using complementary pMOS and nMOS transistors. The pMOS transistors form the pull-up network connected to VDD, while the nMOS transistors form the pull-down network connected to ground.

CMOS NAND Gate

A CMOS NAND gate is realized by connecting the nMOS transistors in series and the pMOS transistors in parallel. The output becomes LOW only when all the inputs are HIGH.

$$Y_{\text{NAND}} = (A \cdot B \cdot C)'$$

CMOS NOR Gate

A CMOS NOR gate is realized by connecting the nMOS transistors in parallel and the pMOS transistors in series. The output becomes HIGH only when all the inputs are LOW.

$$Y_{\text{NOR}} = (A + B + C)'$$

Pin Connections Using IC 4007

3-Input CMOS NOR Gate

Supply Connections:

- Pin 14 connected to VDD (+5 V)
- Pin 7 connected to Ground (VSS)

pMOS Series Connections (Pull-Up Network):

- Pin 11 connected to Pin 1
- Pin 13 connected to Pin 2

nMOS Parallel Connections (Pull-Down Network):

- Pin 7 connected to Pin 9
- Pin 9 connected to Pin 4
- Pin 8 connected to Pin 12
- Pin 12 connected to Pin 5

Input Connections:

- Pin 6 connected to Input A
- Pin 10 connected to Input B
- Pin 3 connected to Input C

Output:

- Pin 12 taken as NOR output

Circuit Diagram

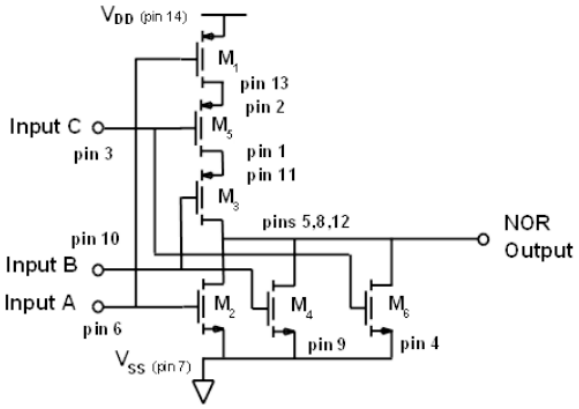

Figure 3: VTC graph

3-Input CMOS NAND Gate

Supply Connections:

- Pin 14 connected to VDD (+5 V)
- Pin 7 connected to Ground (VSS)

pMOS Parallel Connections (Pull-Up Network):

- Pin 14 connected to Pin 2
- Pin 2 connected to Pin 11
- Pin 13 connected to Pin 1
- Pin 1 connected to Pin 12

nMOS Series Connections (Pull-Down Network):

- Pin 5 connected to Pin 9
- Pin 8 connected to Pin 4

Input Connections:

- Pin 6 connected to Input A
- Pin 10 connected to Input B
- Pin 3 connected to Input C

Output:

- Pin 12 taken as NAND output

Circuit Diagram

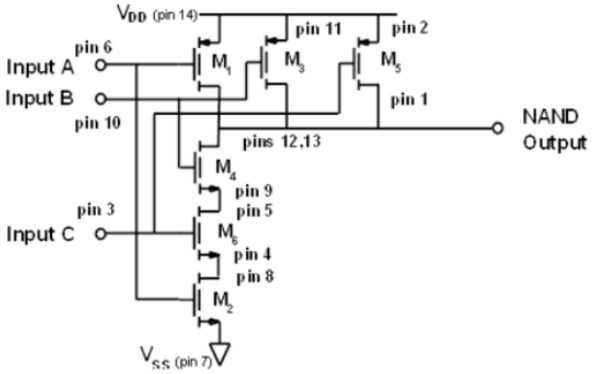

Figure 4: VTC graph

Procedure

The IC 4007 is placed across the central gap of the breadboard. The VDD pin is connected to +5 V and the VSS pin is connected to ground. Internal pin connections are made as specified to form the pull-up and pull-down networks. Inputs are applied to the gates, and the output is observed for all possible input combinations.

Observation

For the 3-input CMOS NAND gate, the output was observed to be logic HIGH for all input combinations except when all three inputs were at logic HIGH, in which case the output became logic LOW.

For the 3-input CMOS NOR gate, the output was observed to be logic HIGH only when all the inputs were at logic LOW. For all other input combinations, the output was logic LOW.

The observed outputs matched the theoretical truth tables.

Truth Table: 3-Input NAND Gate

A	B	C	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table: 3-Input NOR Gate

A	B	C	Output
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Precautions

- Ensure correct orientation of the IC before applying power.
- Do not leave CMOS inputs floating.
- Verify power supply connections before switching ON.
- Avoid short circuits between VDD and ground.
- Switch OFF power before modifying connections.

Result

The 3-input CMOS NAND gate and 3-input CMOS NOR gate were successfully implemented using IC 4007, and the observed outputs matched the theoretical truth tables.

C) Ring Oscillator using NOT Gates

Aim

To design a ring oscillator using an odd number of NOT gates and to estimate the propagation delay of a single NOT gate by measuring the oscillation frequency. The experiment is performed using TTL IC 7404 and CMOS IC 4009 for $N = 3$ and $N = 5$.

Apparatus

- IC 7404 (TTL Hex NOT gate)
- IC 4009 (CMOS Hex NOT gate)
- Breadboard
- DC power supply (5 V)
- Digital Storage Oscilloscope (DSO)
- Connecting wires

Theory

A ring oscillator consists of an odd number of inverters connected in series with the output of the last inverter fed back to the input of the first inverter. Due to the odd number of inversions, the circuit oscillates.

If T is the propagation delay of one inverter and N is the number of inverters, the frequency of oscillation f is given by:

$$f = \frac{1}{2NT}$$

Hence, the propagation delay of a single inverter is:

$$T = \frac{1}{2Nf}$$

Circuit Diagram

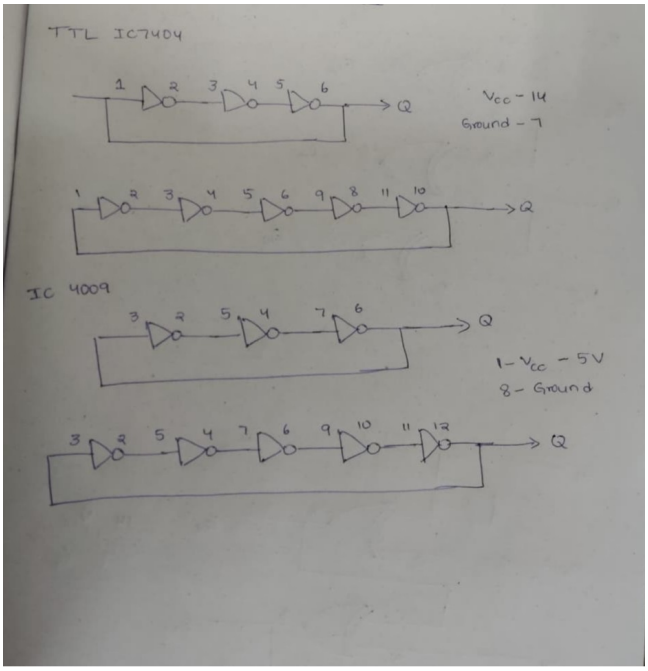

Figure 5: Ring Oscillator

Procedure

1. NOT gates from IC 7404 were connected in a ring configuration with $N = 3$ and $N = 5$.
2. The output of the last NOT gate was fed back to the input of the first gate.
3. The oscillation frequency was measured using a Digital Storage Oscilloscope.

4. The experiment was repeated using CMOS IC 4009.

5. The propagation delay of a single NOT gate was calculated using the measured frequency.

Calculations

The propagation delay of a single NOT gate was calculated using:

$$T = \frac{1}{2Nf}$$

The calculations were performed separately for:

- IC 4009 for $N = 3$

$$f = 4.54MHz$$
$$T = \frac{1}{2 * 3 * 4.54 * 10^6}$$
$$T = 36nS$$

- IC 4009 for $N = 5$

$$f = 3.1MHz$$
$$T = \frac{1}{2 * 5 * 3.1 * 10^6}$$
$$T = 32nS$$
$$T_{avg} = \frac{36 + 32}{2}$$
$$T_{avg} = 34nS$$

- IC 7404 for $N = 3$

$$f = 30.8MHz$$
$$T = \frac{1}{2 * 3 * 30.8 * 10^6}$$
$$T = 5.4nS$$

- IC 7404 for $N = 5$

$$f = 18.6MHz$$
$$T = \frac{1}{2 * 5 * 18.6 * 10^6}$$
$$T = 5.3nS$$
$$T_{avg} = \frac{5.4 + 5.3}{2}$$
$$T_{avg} = 5.35nS$$

Result

A ring oscillator was successfully designed using TTL IC 7404 and CMOS IC 4009 for $N = 3$ and $N = 5$. The oscillation frequency was measured and the propagation delay of a single NOT gate was estimated. The experimental results were found to be consistent with theoretical expectations.

D) Binary to Gray Code and Gray Code to Binary converters

Aim

To implement a 4-bit (i) binary to Gray code converter and (ii) Gray code to binary converter using the TTL exclusive-OR IC 7486, apply the inputs using on-board switches, observe the outputs on on-board LEDs, and verify the truth table.

Apparatus Required

- IC 7486 (TTL Exclusive-OR gate)
- Breadboard
- DC power supply (5 V)
- Connecting wires
- On-board switches
- LEDs with current-limiting resistors

Theory

Gray code is a binary numeral system in which successive values differ by only one bit. This property reduces errors during transitions and is widely used in digital systems such as encoders and communication circuits.

Binary to Gray Code Conversion

For a 4-bit binary number ($B_3B_2B_1B_0$), the corresponding Gray code ($G_3G_2G_1G_0$) is given by:

$$G_3 = B_3$$
$$G_2 = B_3 \oplus B_2$$
$$G_1 = B_2 \oplus B_1$$
$$G_0 = B_1 \oplus B_0$$

Gray to Binary Code Conversion

For a 4-bit Gray code ($G_3G_2G_1G_0$), the corresponding binary number ($B_3B_2B_1B_0$) is given by:

$$B_3 = G_3$$
$$B_2 = B_3 \oplus G_2$$
$$B_1 = B_2 \oplus G_1$$
$$B_0 = B_1 \oplus G_0$$

IC 7486 Pin Details

IC 7486 consists of four 2-input XOR gates.

- Pin 14: VCC (+5 V)
- Pin 7: Ground

Gate pin configuration:

- Gate 1: Inputs (Pins 1, 2), Output (Pin 3)
- Gate 2: Inputs (Pins 4, 5), Output (Pin 6)
- Gate 3: Inputs (Pins 9, 10), Output (Pin 8)
- Gate 4: Inputs (Pins 12, 13), Output (Pin 11)

Circuit Connections

(i) 4-Bit Binary to Gray Code Converter

Power Connections:

- Pin 14 connected to +5 V
- Pin 7 connected to Ground

Logic Connections:

- G_3 taken directly from B_3
- B_3 and B_2 connected to pins 1 and 2; output G_2 taken from pin 3
- B_2 and B_1 connected to pins 4 and 5; output G_1 taken from pin 6
- B_1 and B_0 connected to pins 9 and 10; output G_0 taken from pin 8

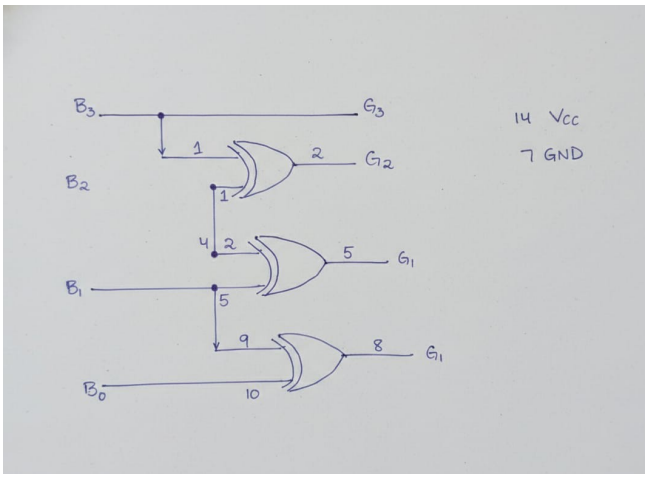

Figure 6: Binary to Gray Code converter

(ii) 4-Bit Gray to Binary Code Converter

Power Connections:

- Pin 14 connected to +5 V
- Pin 7 connected to Ground

Logic Connections:

- B_3 taken directly from G_3
- B_3 and G_2 connected to pins 1 and 2; output B_2 taken from pin 3
- B_2 and G_1 connected to pins 4 and 5; output B_1 taken from pin 6
- B_1 and G_0 connected to pins 9 and 10; output B_0 taken from pin 8

Procedure

The IC 7486 is placed on the breadboard and powered using a +5 V supply. Inputs are applied using on-board switches. XOR gate connections are made as per the conversion equations. The outputs are observed using LEDs. All possible input combinations are applied and the outputs are recorded.

Observation

For the binary to Gray code converter, successive input values resulted in Gray codes differing by only one bit. For the Gray to binary code converter, the

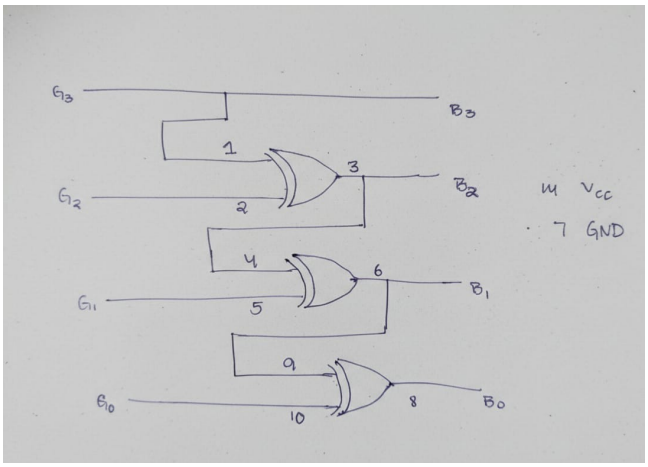

Figure 7: Gray Code to Binary converter

original binary values were correctly reconstructed from the Gray code inputs. The observed outputs matched the theoretical truth tables.

Truth Table (Binary to Gray)

Binary	Gray
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111
1011	1110
1100	1010
1101	1011
1110	1001
1111	1000

Precautions

- Ensure correct orientation of IC before applying power.

- Use current-limiting resistors with LEDs.
- Do not leave inputs floating.
- Verify power connections before switching ON.

Result

A 4-bit binary to Gray code converter and a 4-bit Gray to binary code converter were successfully implemented using IC 7486, and the observed outputs matched the theoretical truth tables.