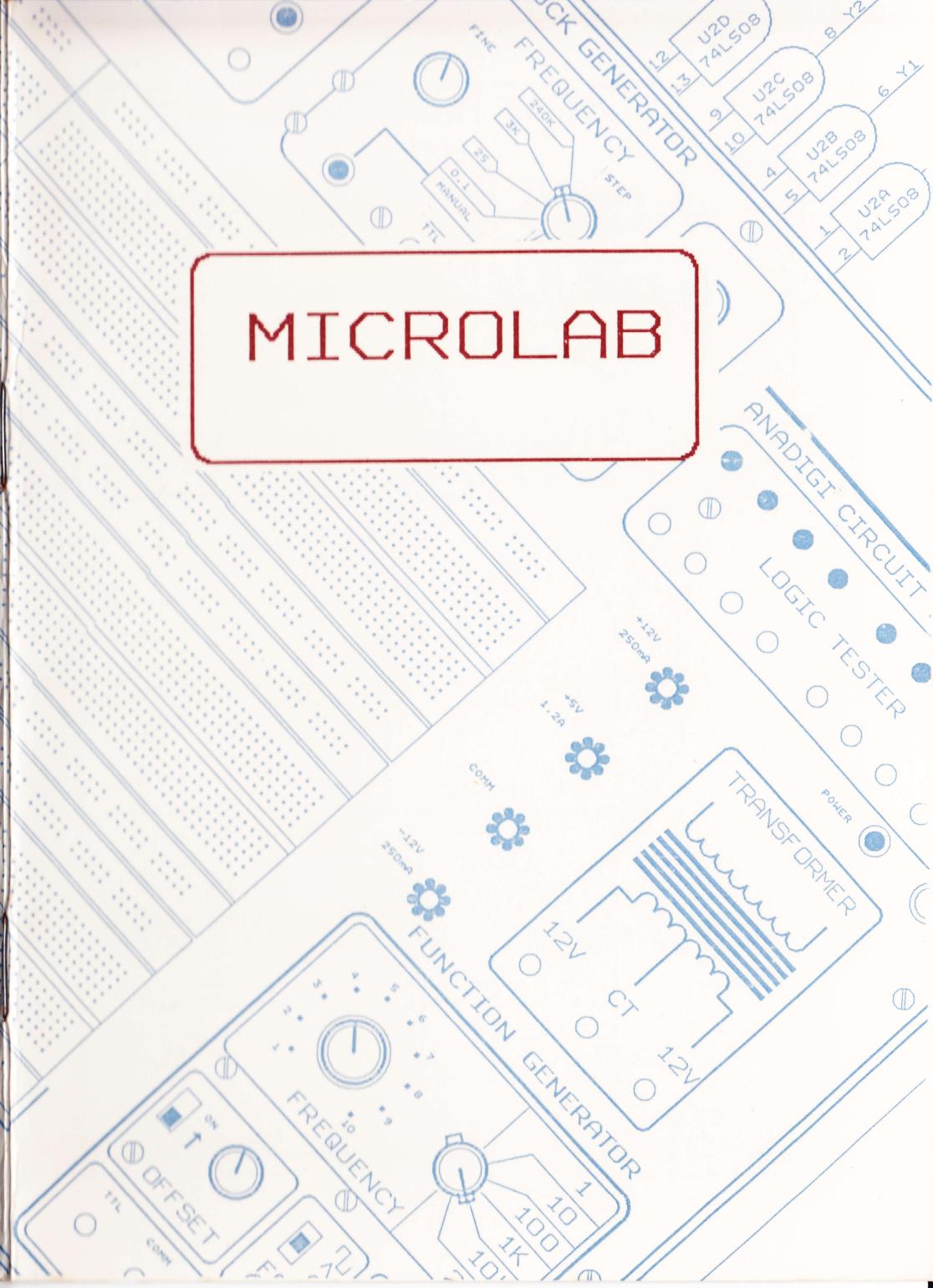
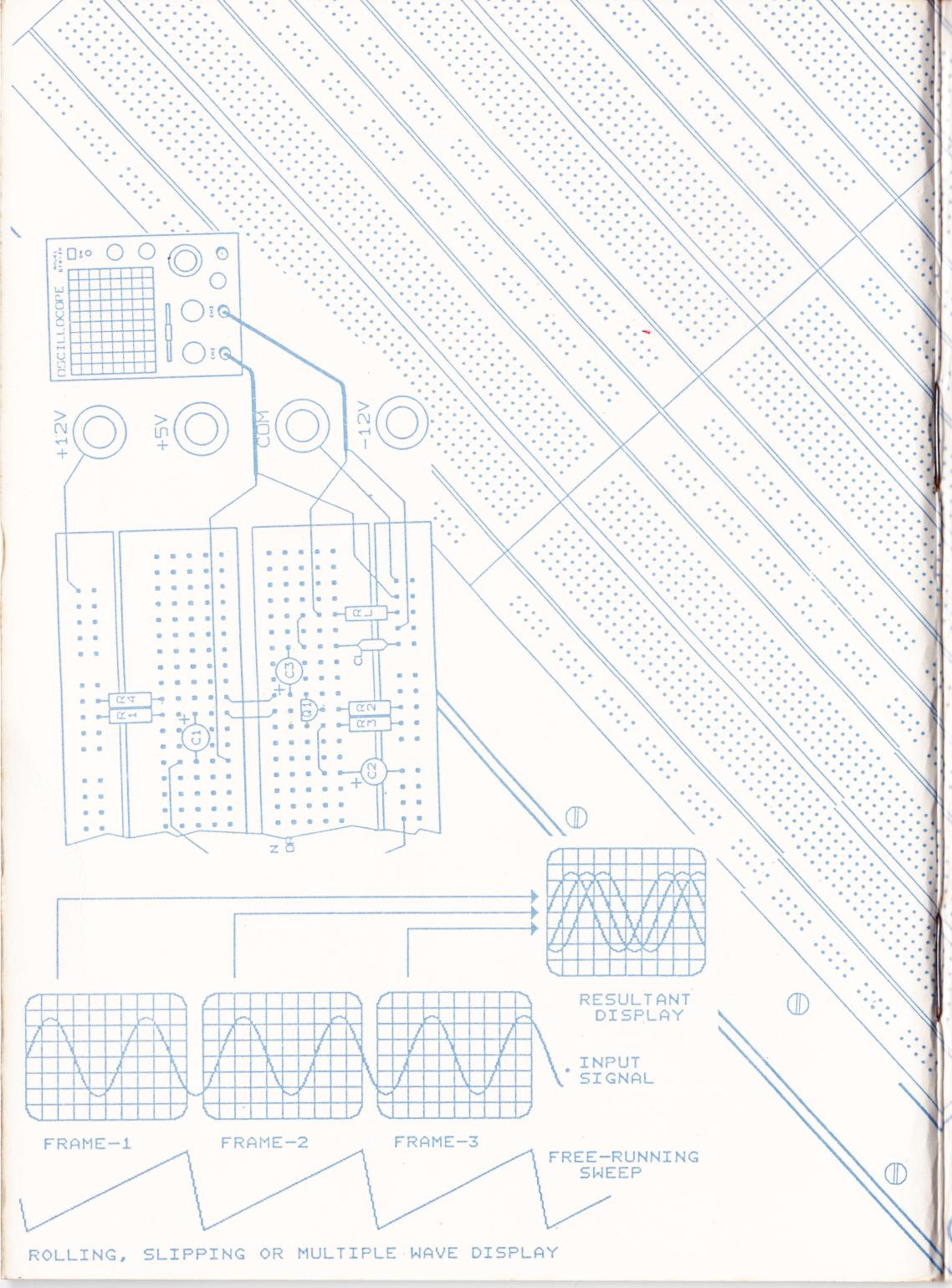
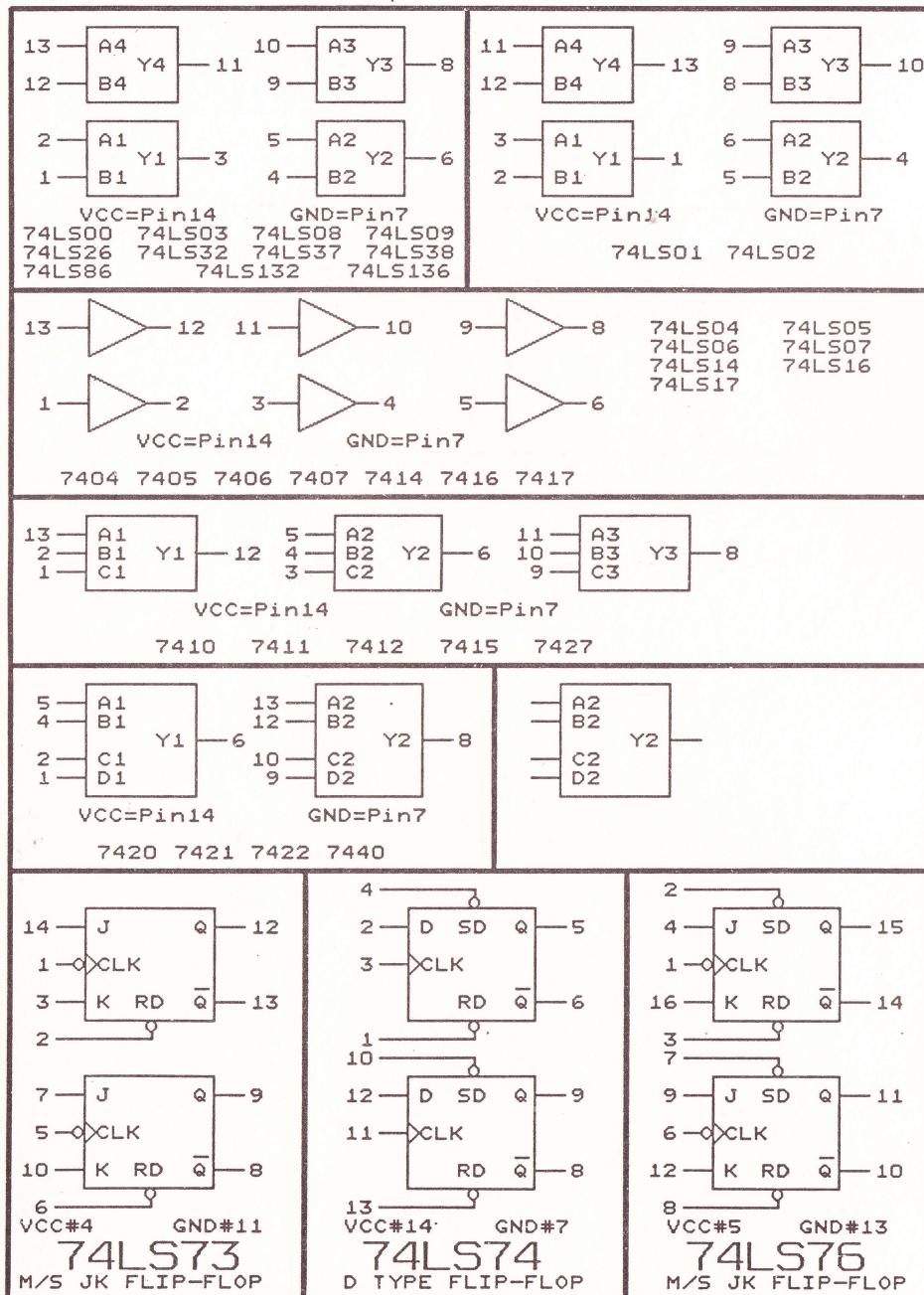


# MICROLAB



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**MICROLAB** is an assembly of instruments required in Analog and Digital electronic experiments. This is equivalent to a complete laboratory set-up except an Oscilloscope. In fact it is by far better than ever, because existence of all instruments in one frame makes interconnections short, firm and noise free.

**MICROLAB** introduces the concept "make your own circuit". The merits of MICROLAB over the conventional so called SET-UP trainer kits are :-

- Suitable for students, trainee, in science college, polytechnic, engineering college, technical and industrial institute and R & D centres.
- Same experiments may be allotted simultaneously to all students with wider choice.
- A one time lecturer or technical advice on an experiment will benefit all the student, since they all are doing the same experiment.
- A good pace is maintained between theory and practice. *i.e.* black board to bread board.
- Students come closer to the electronic events and can interact in component level, thereby gaining more confidence, which is most desirable to the would be employer. This is not possible with set-up experiments.
- Since students set up their experiments at components level, defects can be traced into components level and may be rectified by replacing the bad components. So no experiment is held up for set-up failure.

- Short circuit protection has been given for any point to any point on board.
- Only a circuit diagram provides the necessary guidance to the students.
- List of experiments may be dynamically modified without the need for purchasing new set-ups.

## CONSTRUCTION

The instrument is sturdy built, both electrically and mechanically. It is perfectly student-proof. Students can not do any electrical harm to it deliberately or out of ignorance. Inside, all sections are modular and fitted with plug-in terminals.

## SUBSYSTEM – DETAILS

### Power Supply

MICROLAB consists of 5 Nos. of Power Supplies *i.e.* (i) +5 Volt, (ii) +12 Volt, (iii) -12 Volt, (iv) 0 to 30 Volt variable and (v) AC 12V - CT - 12V. Followings are the details of the various Power Supplies. See figure 1.

(i) The regulated +5 Volt DC Power Supply is specially made for digital experiments though it can also used for other experiments. The maximum current is 1.2 Amp, which is sufficient for bread-board full of ICs. The output is available at BTI-15 red ( $\pm 5V$ ) terminal referred to BTI-15 black (COM) terminal. This has a unique feature called "Trip and delay reset" overload protection. If an overload occurs the Power Supply trips OFF until the mains AC power is put to OFF at-least 30 seconds. This feature protects the experimental circuit and the Power Supply itself. It has been experienced that if the Vcc (+5 Volt) even gets connected to an "output LOW" pin of an IC or IC's Vcc-GND pin connections reversed (which is often done by the students by putting the ICs

reversed on the bread-board), the IC remains undamaged. The reset delay period of 30 seconds is chosen, keeping in mind the common psychology of students, otherwise the students try to get reset (repeatedly) the Power Supply without rectifying the faults.

(ii) The regulated +12 Volt DC supply is made around the well-known IC 7812. The current limit is 250 mA, with a constant current overload protection. The output is available at PT-10 yellow (+12V) terminal referred to BTI-15 black (COM) terminal.

(iii) The regulated -12 Volt DC supply is made around the well-known IC 7912. The current limit is 250 mA, with a constant current overload protection. The output is available at PT-10 green (-12V) terminal referred to BTI-15 black (COM) terminal.

(iv) The variable voltage regulated Power Supply can be set at any voltage between 0 Volt to 30 Volt by turning the control Knob (1 in fig.2). The current limit is 100 mA, with a constant current overload protection. The output is available at PT-10 blue (0-30V) terminal (2 in fig.2) referred to COM terminal.

+12V

+5V

COM

-12V

Figure 1

(v) An isolated AC 50 Hz 12-CT-12 Volt @ 100mA is provided for experiments like rectifier, clipping, clamping etc. The supply is derived from the main's transformer ( $\approx 20:1$  ratio) of MICROLAB and specified at 230 Volt AC input (line Voltage) only. Obviously it will vary with the line voltage variation. The output is available at

three snap-fit terminals. (fig. 3)

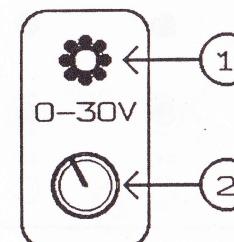


Figure 2

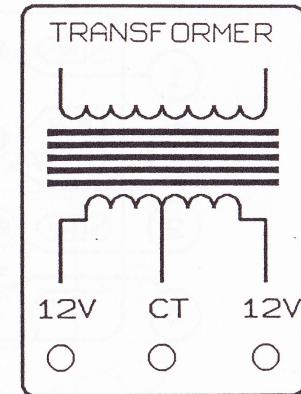


Figure 3

### Logic Source

The LOGIC SOURCE (array of 8 logic switches) deserve special reference since the invention of a technique, involved herewith, provided the impetus for the launching of MICROLAB. The technique is the use of unstrained phosphor bronze integrated leaf switches. The electronic circuit following the switch not only debounces it but is so environment friendly that it modifies itself on overload due to wrong connection. It is so sensitive that a touch by hand or a metal object to the output terminal may change its state. If user is not able to set or reset a particular bit it is a warning that there is a wrong connection at this point. Conventional switches, however costly, need at least 10% replacement after a semester of laboratory work. This has been the experience of technicians in Computer Sc. & Engg. Dept of IIT, Kharagpur. And then they used these leaf switches. Not a single switch has gone bad since 1984 after their regular experiments in the hardware laboratory. The SET buttons(1), CLeaR buttons(2), status indicators(3) and the OUTput terminals(4) are shown in fig. 4.

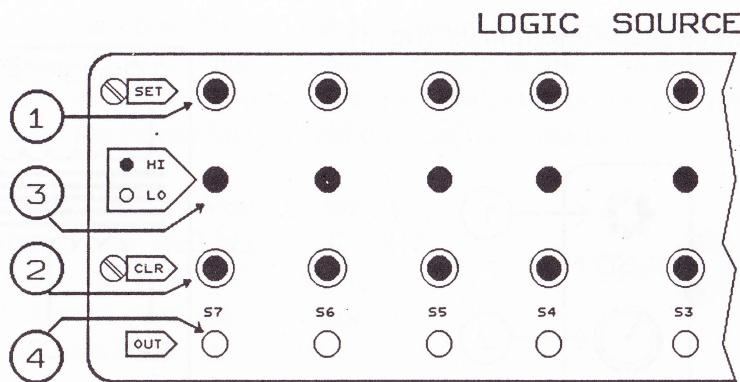


Figure 4

### Clock Generator

The CLOCK generator (TTL rectangular wave) frequency may be adjusted continuously from very low to moderately high. The very low frequency is used to trace logical events by logic probes visually. The high frequency is used in conjunction with an oscilloscope. The manual mode generates single pulse and useful for circuit debugging in single step mode. The various controls are shown in fig.5

1. **Mode/Frequency Selector Switch** selects the frequency range ( High, Medium or Low) as well as Manual Mode.
2. **MANUAL Switch** for the operation of manual clock. Clock Output High if pressed and clock Output Low if released. (Keeping the Mode selector Switch in MANUAL position).
3. **FREQUENCY Control** sets the frequency within the range Min. to Max. value
4. **Indicator** – logic state of the TTL output is displayed here

5. **TTL &  $\overline{\text{TTL}}$  Outputs** Terminals Output TTL & complimented TTL compatible desired signals.

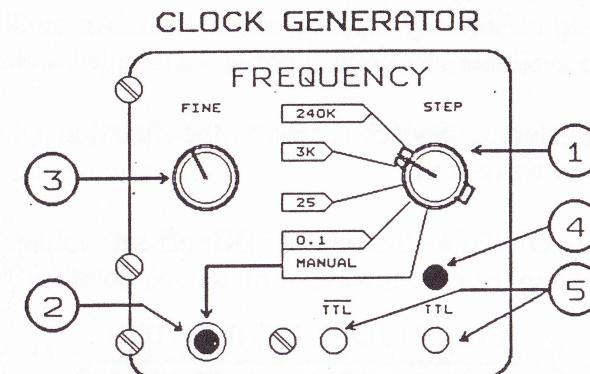


Figure 5

### Logic Tester

The eight bits LOGIC PROBES are noteworthy in that, each of them can show logic LOW, HIGH, PULSE and Hi-impedance state of a point. That is they are Four-State logic probes. The **Hi-impedance** state conforms to one of "Tri-state", "Faulty output", "Broken wire", "Insertion to a blank hole" or "Insertion of the wire sleeve into the connector". Conventional logic probes show such state as logic "Hi", while, a voltmeter shows "zero". The logic probes of MICROLAB display such condition as "Hi-Z". INPUT terminal (1) and Indicator (2) are shown in fig. 6

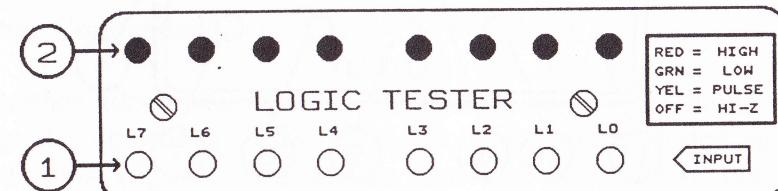


Figure 6

## Function Generator

A standard square-sine-triangle FUNCTION GENERATOR is also available on board. It produces any one of the three waveforms (square, triangle, sine) of amplitude limited within -10Volt and +10Volt. A dc offset may also be added to it. An auxiliary TTL output is also available. Various controls are detailed under (fig. 7)

1. **FORM Selector Switch** selects the function i.e. Square, Triangle or wave-form.
2. **OFFSET ON/OFF Switch.** A DC off-set voltage may be introduced on the output wave-form in ON position.

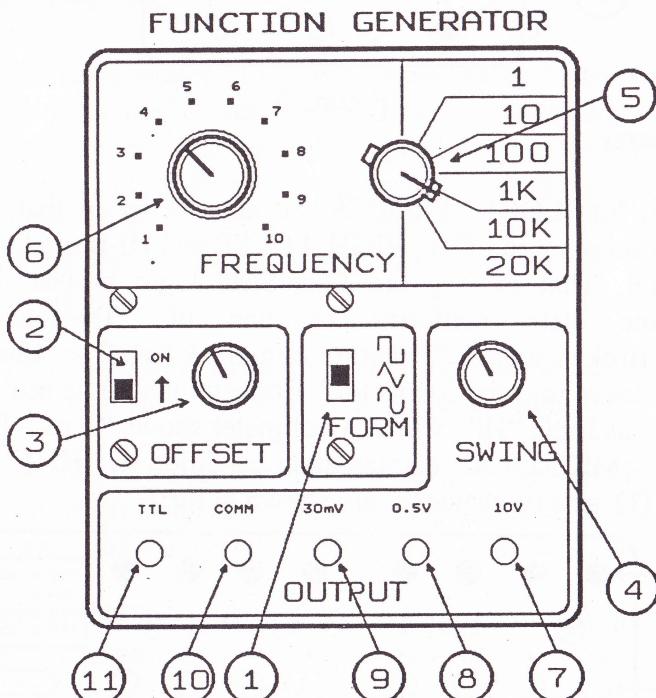


Figure 7

3. **OFFSET Control** controls the amount of Off-Set voltage to be added to the output wave-form. Clock-wise increase and anticlock-wise decrease.
4. **SWING Control** sets the amplitude of output wave-form. Clock-wise increase and anticlock-wise decrease.
5. **FREQUENCY Multiplier** multiplies the frequency set by the frequency control.
6. **FREQUENCY Control** sets the frequency in conjunction with multiplier switch.
7. **10 V Output Terminal.** Produces 0 to  $\pm 10_{PP}$  Volts Output on Min to Max rotation of SWING control.
8. **0.5V Output Terminal.** Produces 0 to  $\pm 500_{PP}$  mili Volts Output on Min. to Max. rotation of SWING Control.
9. **30 mV Output Terminal** Produces 0 to  $\pm 30_{PP}$  mili Volts Output on Min. to Max. rotation of SWING Control.
10. **COM Terminal** is Ground or 0 Volt reference.
11. **TTL Output Terminal** – a TTL output of same frequency is available at this terminal.

## Easy Connection

Another silent worker, an indigenous product, to be found in all signal connections on MICROLAB, is the spring-loaded snap fit terminals (fig. 8) This makes firm and clean interconnections possible with ordinary wires instead of patch cords. Only

Laboratory people feel the pains linked with so called patch cords!!!.

### Stack Buffers

And lastly take note of the four buffers (appearing useless?) on front panel. They are there to enable you keep one set on top of another without affecting the experiments wired on them. You can stack them upto six levels and vacate useful laboratory space for another class. (see fig. 9)



Figure 8



Figure 9

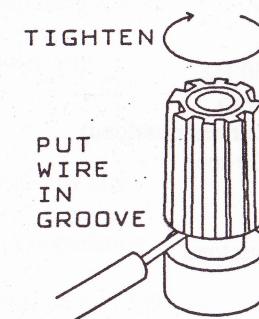
### Installation

MICROLAB may be installed in a dust-free and normal temperature laboratory environment. Use a power source that delivers 200 to 240 Volts AC, 45 to 55 Hz. Be sure about earth point of your socket and proper connections i.e. live at right and neutral at left. Avoid direct sunlight and moisture.

### Connectivity

The Power terminals are well-known BTI-15 and PT-10 Screw terminal with banana plug compatibility. They are different in colour for each power supply. All other input/output signal connectors are indigenously made spring-loaded snap-fit terminals. These unique terminals help to make firm and quick connections with ordinary wires instead of special patch cords. (*Only laboratory people feel the pains linked with so called patch cords!*). The

correct procedure of connections for both terminals are shown in fig 10.



WIRE CONNECTION TO  
PT-10 POWER TERMINAL



WIRE CONNECTION TO  
SNAP-FIT TERMINAL

Figure 10

### The Workspace

MICROLAB is installed with 6 numbers WISH-102 bread-boards. The bread-boards are pasted horizontally up-down on the base metal of the instrument. The details of bread-board are given in appendix

### Interference

The instrument is free from interference i.e. it neither creates nor receives any noise which may disturb the operation of the experimental circuits (especially digital circuits such as counters, shift-registers etc.) in a classroom where multiple MICROLAB are in use.



Auxiliary Output	: TTL (2 Fan out)
Output Reference	: Output is in reference to the Com Terminal which is connected to the Power Supply COM Terminals via a 10 Ohm resistance
Protection Connectivity	: Short circuit to any voltage on board Snap-fit Terminals

*Note 1 : Reference (GND) for all other sections is Power Supply COM Terminals*

*Note 2 : The LED indication in PULSE mode of Logic Probe is restricted up-to 50 K Hz.*

## APPENDIX

### About the BREADBOARD

Breadboard is a valuable invent that facilitates experiment with electronic circuits. Any experimental circuit can be hooked up on it very quickly and reliably. It not only saves time but also keeps components reusable. Components are not to be soldered or their leads trimmed. The limitations of the breadboard are :-

Thickness of the component leads 24 swg to 26 swg  
 Point to point isolation 100 Volt maximum  
 Maximum current at one junction 100 miliAmp  
 Maximum frequency a few MegaHertz

Breadboards are available in various sizes and various make. The best of the breadboards have been used in MICROLAB. Six units

of type 102 are installed. Figure11 shows the external view of one breadboard.

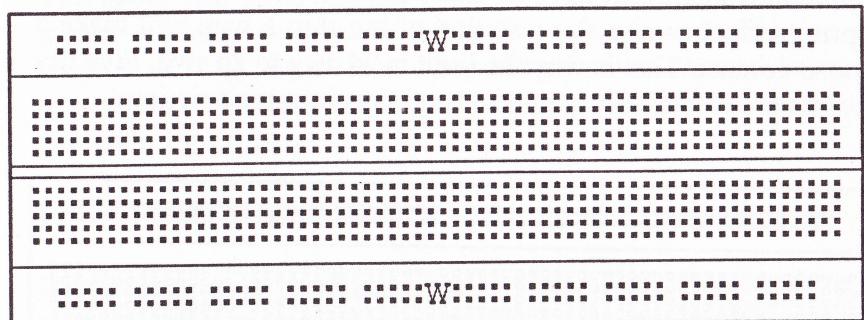


Figure 11 : BREADBOARD type 102

Component leads are inserted through the holes to make interconnection. Each hole is called a tie-point. How exactly the connections are made can be understood from the construction of the tie-points( fig 12) and their interconnections (fig 13).

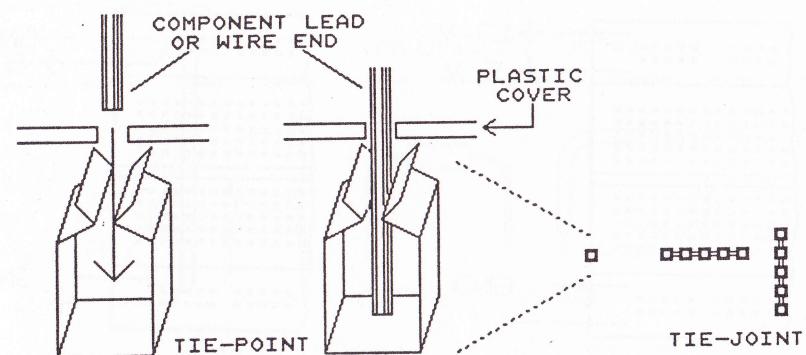


Figure 12 : Tie-point and tie-joint

A tie-point is made of silver plated phosphor bronze leaf contactor. As a component lead or a wire is inserted from the

hole in top cover the v-shaped ends of the leaf allow it with proper centering and even pressure from both sides. It can be appreciated here that insertion of too thick a wire will damage the spring effect as also the insertion of too thin a wire will make a loose contact. That is why the limit is 24 swg to 26 swg. Five tie-points are electrically connected and thus it forms a tie-joint.

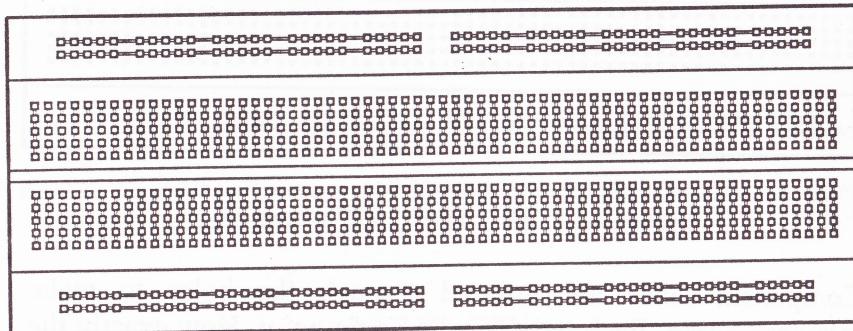


Figure 13 : Internal connections of the BREADBOARD

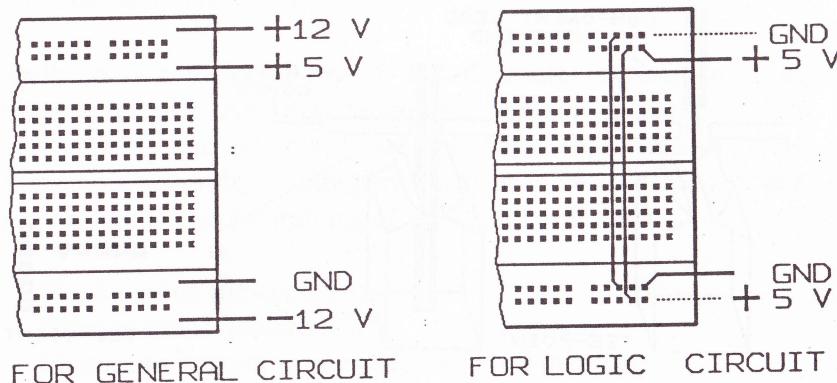


Figure 14 : Power bus convention

### Power bus convention

The upper two rows and the lower two rows of a breadboard are meant to carry the power supply for noise-free distribution to various parts of the circuit. They should never be used to carry any signal. The convention of feeding powerlines to these are shown in figure 14.

### Insertion of Components

Component leads should be inserted vertically. Do not bend leads at point of insertion as it may break here or leave the inner portion oblique. Do not bend sharply because sharp bends can not be straightened for re-use. Avoid criss-cross of components.

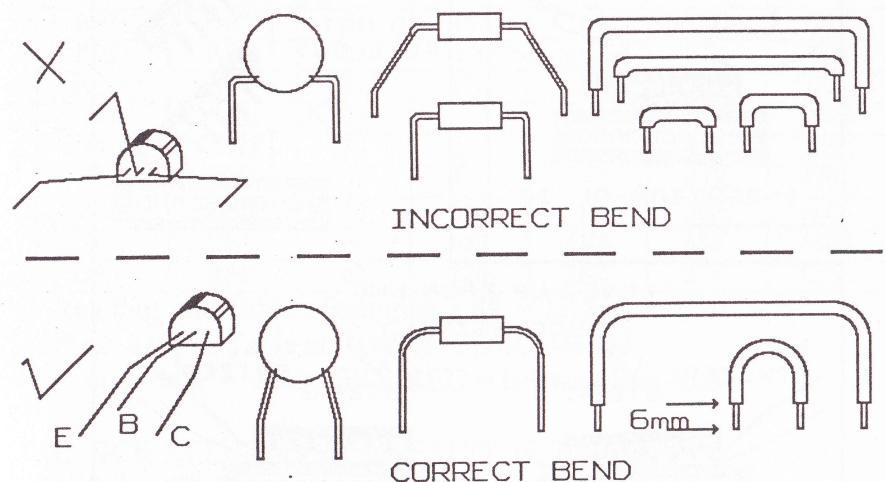


Figure 15 : Component leads and wires

Transistors are to be bent as shown in figure 15 and inserted into adjacent holes only so that the top view will be as in figure 18. Resistor Diode & Capacitor leads should **not** be pulled apart **more than 1 inch**.

## Insertion and removal of IC

Check the pins of the IC straight. Put the IC across the central channel of the breadboard with pins right on the holes. Press the IC at both ends simultaneously (fig. 16)

Removal of IC needs a greater care. Pulling out an IC will result in **bent pins**. Lever up each end alternately and successively until it becomes loose (fig. 16)

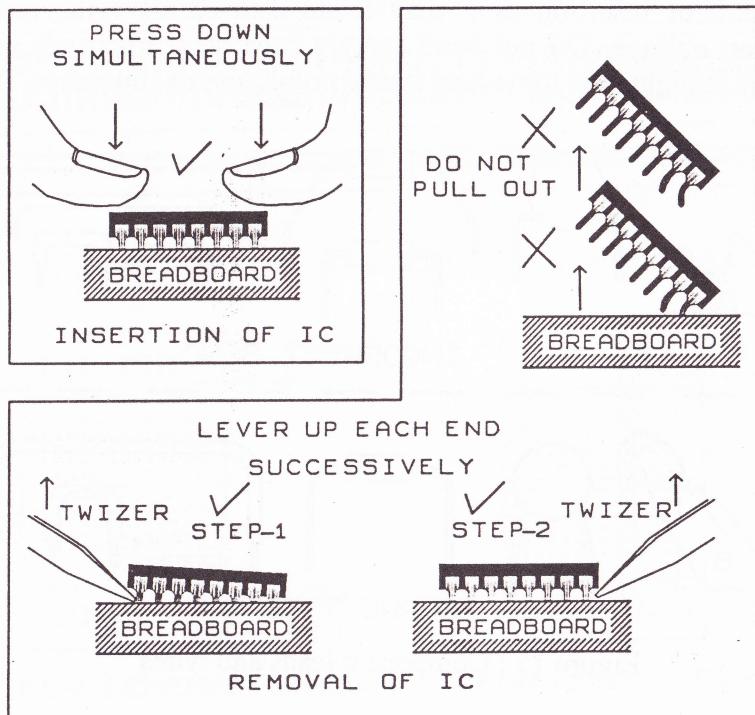
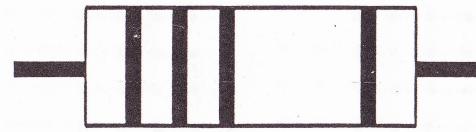


Figure 16 Insertion and removal of IC

COLOUR CODES : Black=BLK=0 Brown=BRN=1  
 Red=RED=2 Orange=ORG=3 Yellow=YEL=4 Green=GRN=5  
 Blue=BLU=6 Violet=VIO=7 Grey=GRY=8 White=WHT=9



Value of R =  $AB \times 10^C$  D = gold for 5% D = silver for 10%

Example YEL-VIO-ORG =  $47 \times 10^3 = 47$  K ohm

### QUICK REFERENCE RESISTANCE TABLE

1<sup>st</sup> Colour 2<sup>nd</sup> Colour ----- 3<sup>rd</sup> Colour -----

		BLK	BRN	RED	ORG	YEL
BRN	BLK	10	100	1K	10K	100K
BRN	RED	12	120	1K2	12K	120K
BRN	GRN	15	150	1K5	15K	150K
BRN	GRY	18	180	1K8	18K	180K
RED	RED	22	220	2K2	22K	220K
RED	VIO	27	270	2K7	27K	270K
ORG	ORG	33	330	3K3	33K	330K
ORG	WHT	39	390	3K9	39K	390K
YEL	VIO	47	470	4K7	47K	470K
GRN	BLU	56	560	5K6	56K	560K
BLU	GRY	68	680	6K8	68K	680K
GRY	RED	82	820	8K2	82K	820K

Reading the Table : Example 1.8K = 1K8

Find 1K8 in Table at ROW-4 COLOUMN-3

Colour code = BRN-GRY-RED = Brown-Grey-Red

### QUICK REFERENCE CAPACITOR TABLE

1<sup>st</sup> No. 2<sup>nd</sup> No. ----- 3<sup>rd</sup> No -----

		1	2	3	4
1	0	100 PF	1000 PF	.01 $\mu$ F	.1 $\mu$ F
1	5	150 PF	1500 PF	.015 $\mu$ F	.15 $\mu$ F
2	2	220 PF	2200 PF	.022 $\mu$ F	.22 $\mu$ F
3	3	330PF	3300 PF	.033 $\mu$ F	.33 $\mu$ F
4	7	470 PF	4700 PF	.047 $\mu$ F	.47 $\mu$ F
6	8	680 PF	6800 PF	.068 $\mu$ F	.68 $\mu$ F

LAY OUT SHEET: USE XEROX COPY OF THIS FOR LAY-OUT

19

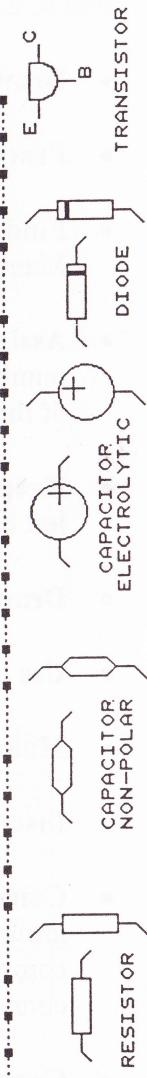
USE THESE  
SYMBOLS



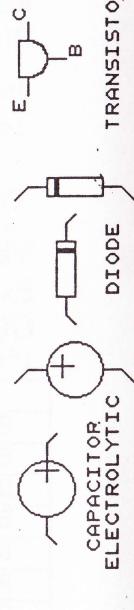
LAY OUT SHEET: USE XEROX COPY OF THIS FOR LAY-OUT

20

USE THESE  
SYMBOLS



USE THESE  
SYMBOLS



## PROCEDURE OF A COMPLETE EXPERIMENT

- Draw the circuit diagram from word description of the problem.
- Procure all components, tools, hook-up wires, multi-meter etc.
- Find the pin details of the IC, Transistor, Diode etc. (Use Data Manual)
- Assign Chip and other active components identification numbers into the circuit diagram on each logical sub-component of the Chip and other active components used.
- Keep the MICROLAB power OFF with switch provided on the left hand side.
- Draw a lay-out plan for placement of components on board
- Use only single strand 25 / 26 swg wire for interconnection.
- Make Power Bus connections as described earlier (Fig. 14)
- Insert the Chips and other active components as per lay-out
- Connect the common bus to  $V_{ss}$  (Gnd) of each Chip and grounded pins of transistors with short jumpers. Other components having one end connected to ground should be connected directly to the bus.
- Connect the  $V_{cc}$  bus to each  $V_{cc}$  input of the Chips with short jumpers.
- Make all other interconnections starting from the input side of your diagram.

- **Tik** every line on the diagram as it is done.
- **Do not** think of circuit logic while you make connections
- Put power switch on and proceed to verify result.
- Keep power off while making any change in connection.

### Example : Common Emitter Amplifier with BC547

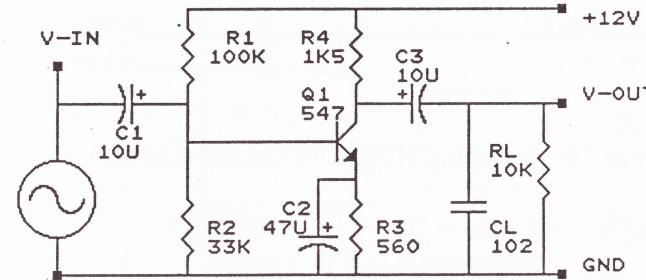


Figure 17 CE Amplifier Circuit diagram

Expected results :  $V_E = 2.2 \text{ V}$   $V_C = 7 \text{ V}$   $V\text{-Gain} = 150$

Max-input = 50 miliVolt Peak to Peak

$F_L = 200 \text{ Hz}$  Flat range = 2 KHz to 20 KHz  $F_H = 100 \text{ KHz}$

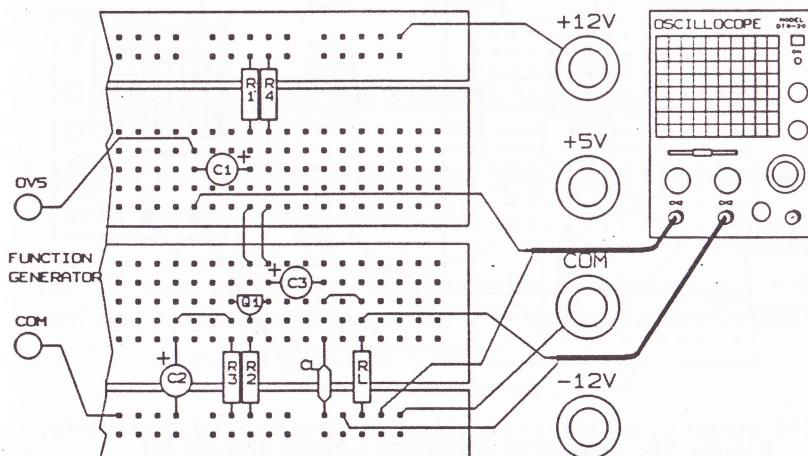


Figure 18: CE Amplifier Layout and set-up

### Example : Invertig Amplifier with Op-Amp 741

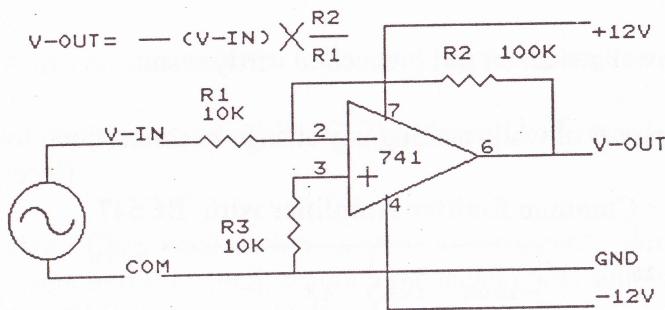


Figure 19 : Inverting Amplifier Circuit diagram

Expected result : V-gain = 10     $F_H = 100$  KHz  
 Slew-rate = 0.5 V/  $\mu$  Second

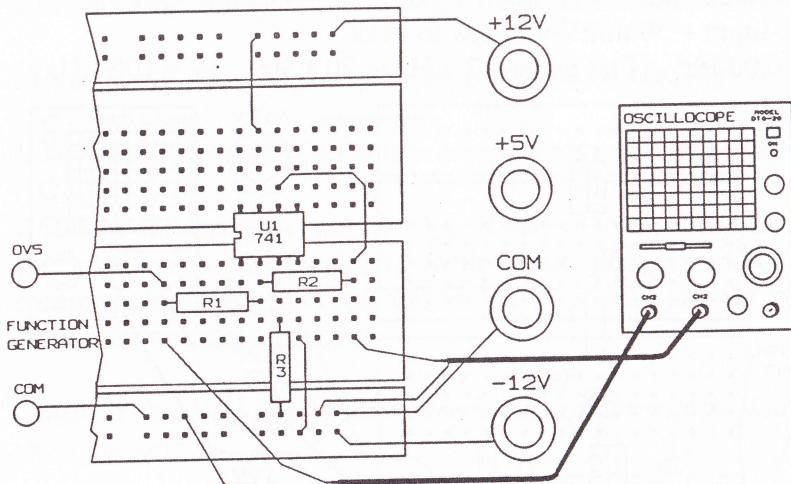


Figure 20 : Inverting Amplifier Layout and set-up

### Example : 2 to 4 Decoder

Find the boolean functions.  
 Draw the logic diagram.

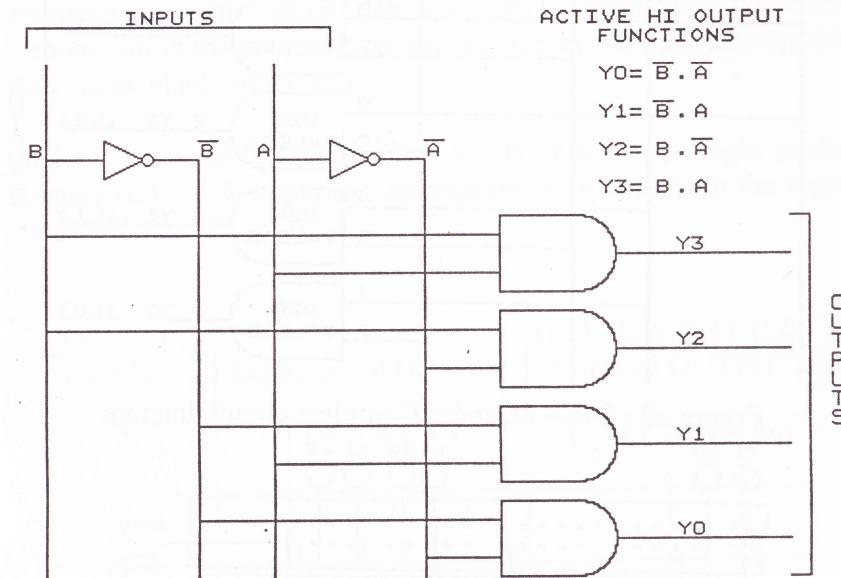


Figure 21: 2 to 4 decoder logic diagram

Put the IC type numbers , sub-block numbers, pin numbers on the diagram (figure 22 and figure 23).

Plan physical positions of the ICs on the breadboard and number them as U1, U2 etc for first row ; V1, V2 etc for the second row and W1, W2 etc for third row (figure 22)

Make power-bus connection for logic circuits (as in figure 14)

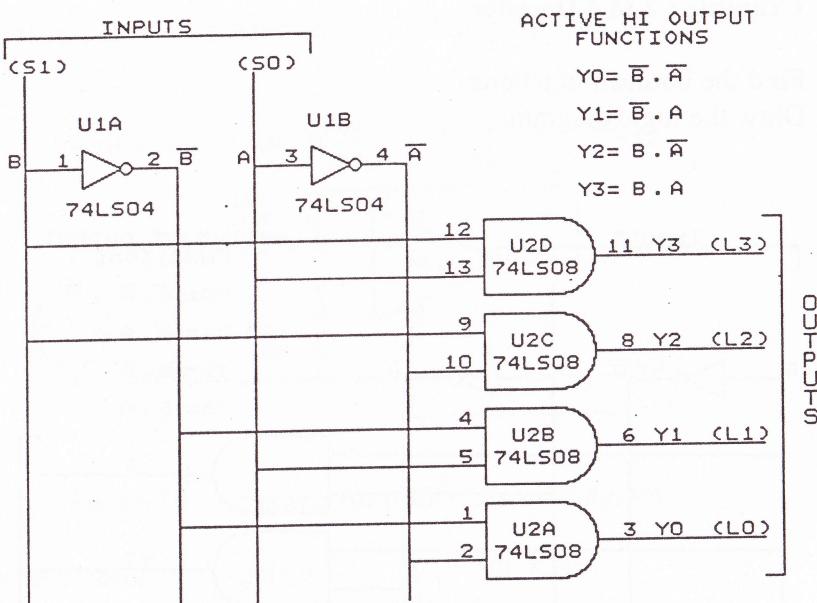


Figure 22 : 2 to 4 Decoder Complete circuit diagram

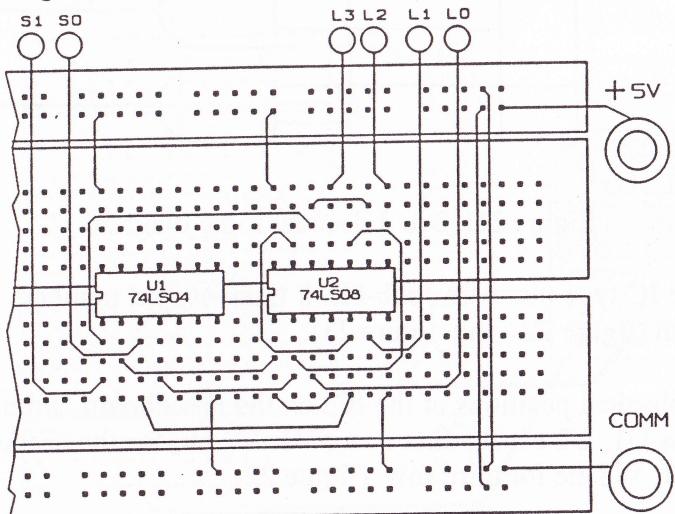


Figure 23 : Decoder Layout and interconnection

Put the ICs at planned positions.

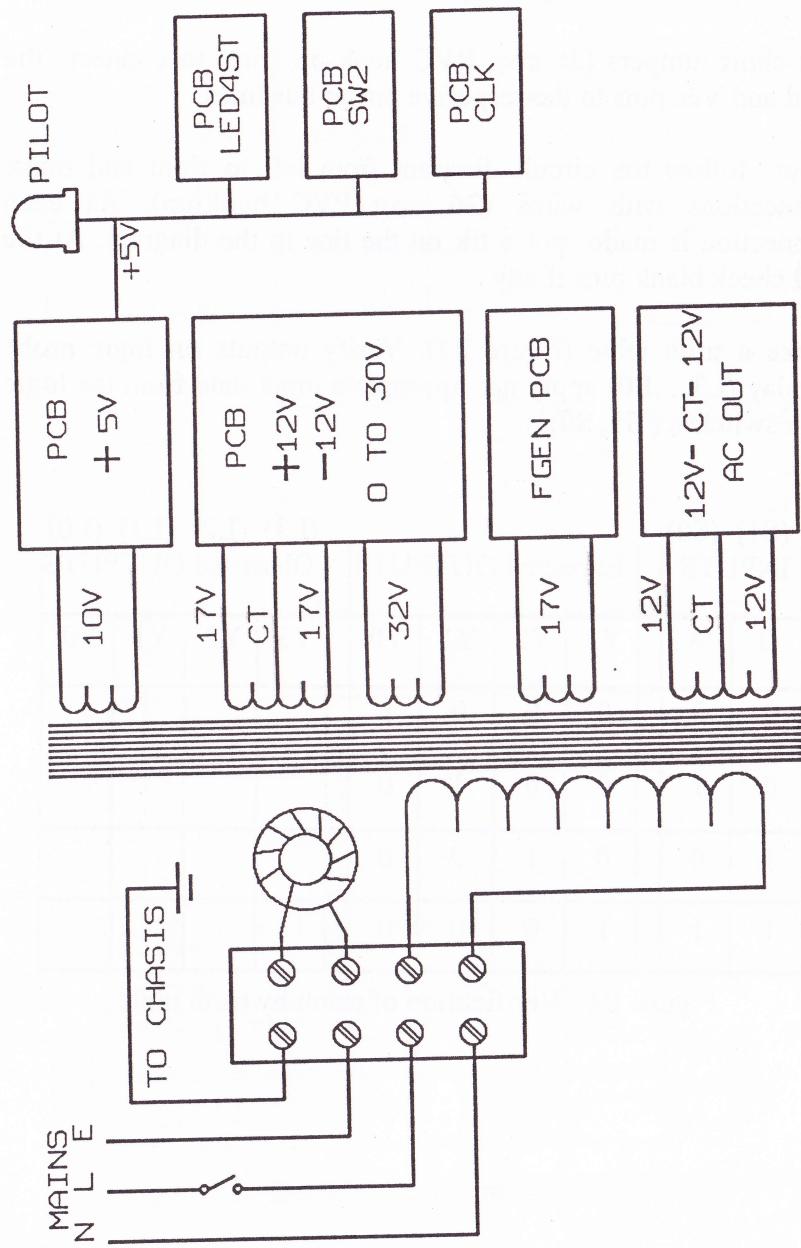
Put short jumpers (26 swg PVC hook up wire) to connect the Gnd and Vcc pins to the respective power bus lines.

Now follow the circuit diagram from left to right and make connections with wires (26 swg PVC hook-up). As each connection is made put a tick on the line in the diagram. At the end check blank pins if any .

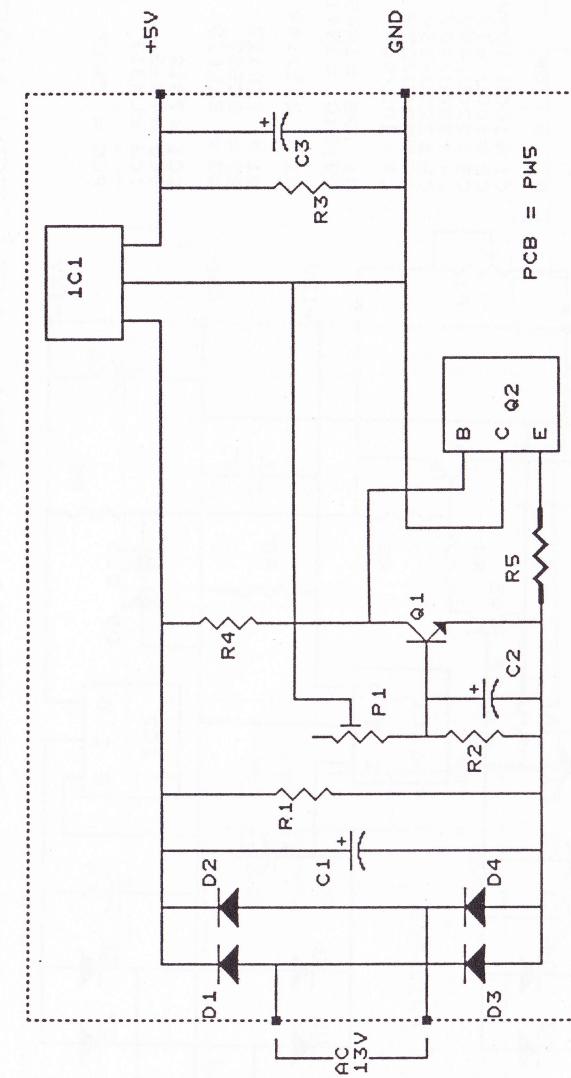
Make a truth table (figure 24). Verify outputs on logic probe display (L3....L0) applying appropriate input data from the logic data switches ( S1, S0).

(S1) (S0) INPUTS	Expected OUTPUTS				(L3) (L2) (L1) (L0) Observed OUTPUTS				
B	A	Y3	Y2	Y1	Y0	Y3	Y2	Y1	Y0
0	0	0	0	0	1				
0	1	0	0	1	0				
1	0	0	1	0	0				
1	1	1	0	0	0				

Figure 24 : Verification of result by truth table

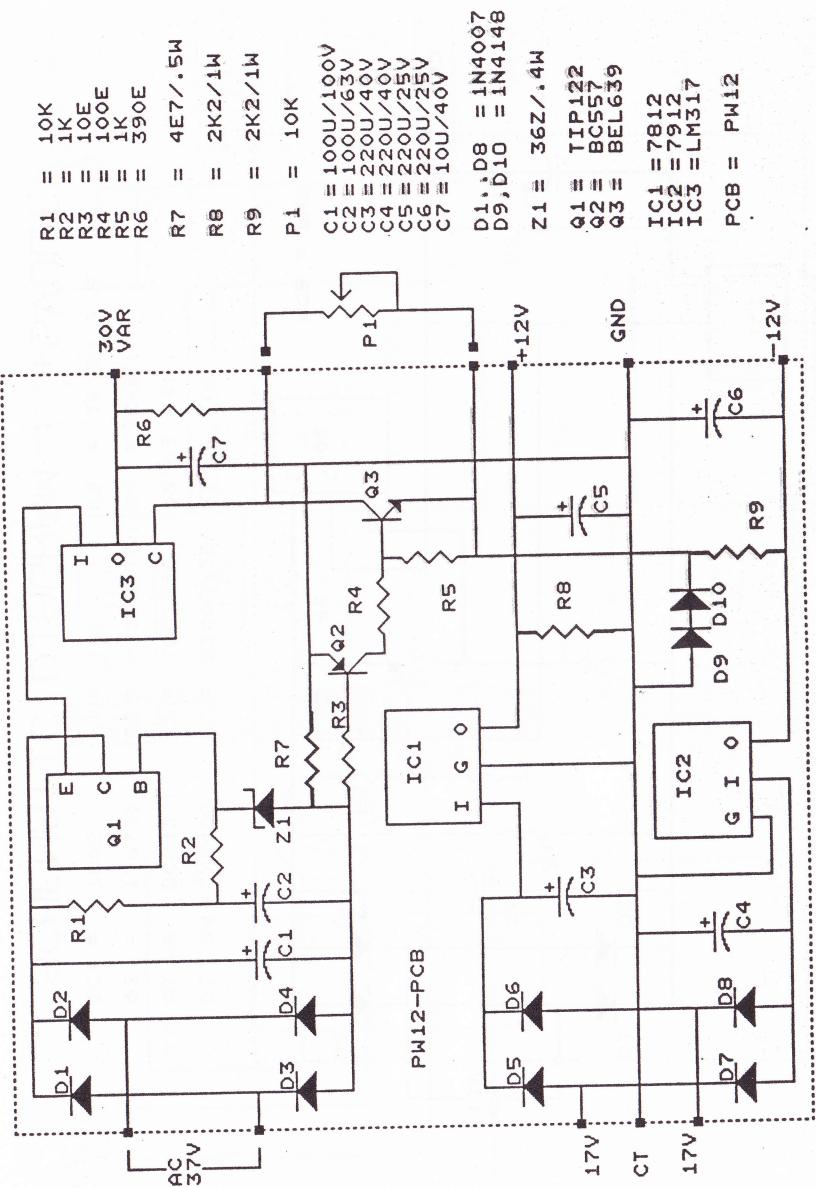


BLOCK DIAGRAM : POWER DISTRIBUTION

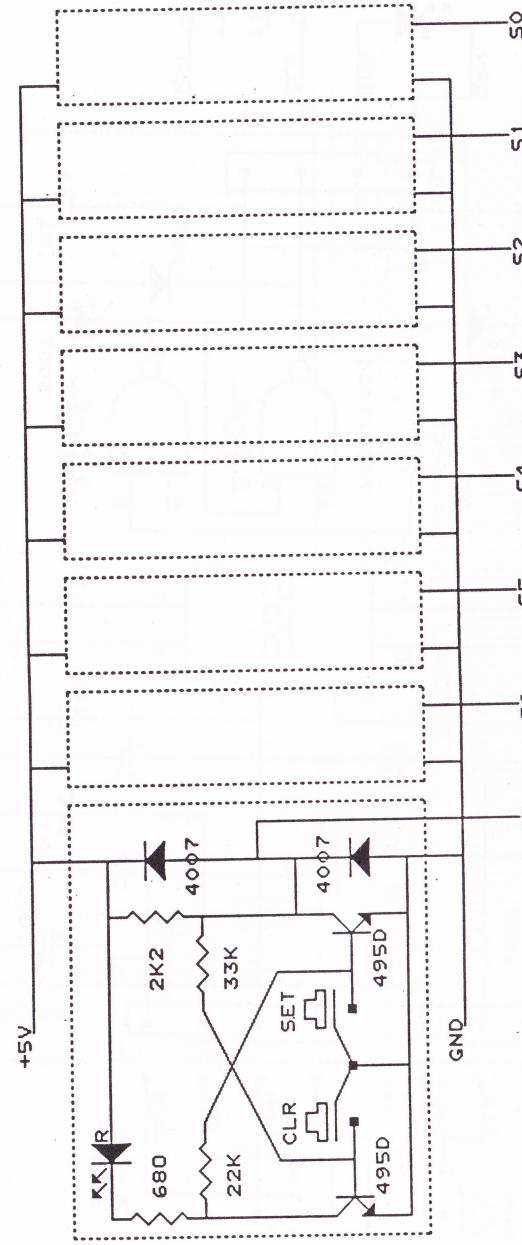


$D_1..D_4 = 1N5408$        $C_1 = 2200\mu\text{F}/25\text{V}$        $R_1 = 10\text{k}$   
 $Q_1 = BC547$        $C_2 = 10\text{uF}/25\text{V}$        $R_2, R_3 = 4\text{k7}$   
 $Q_2 = TIP122$        $C_3 = 4700\mu\text{F}/16\text{V}$        $R_4 = 5\text{k6}$   
 $I_{C1} = 7805$        $P_1 = 10\text{k}$        $R_5 = 1\text{E}/2\text{W} \times 2$

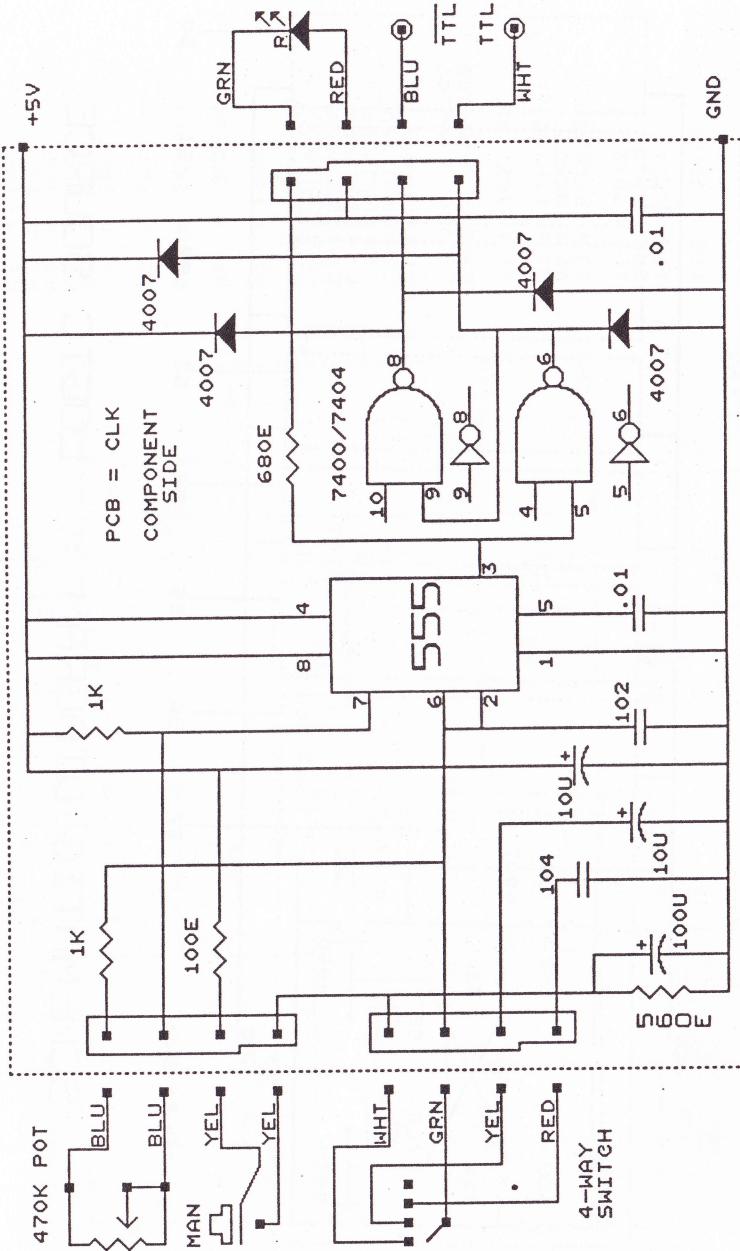
SCHEMATIC DIAGRAM : +5VOLT



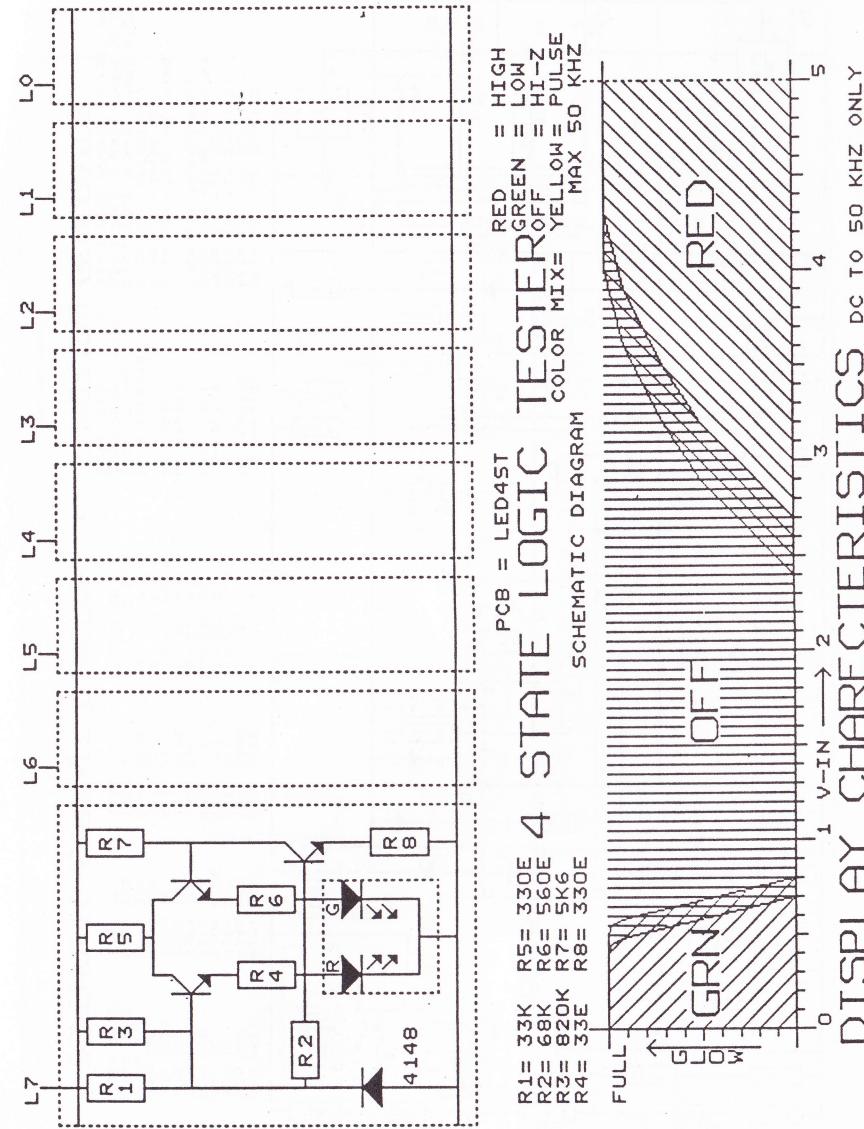
SCHEMATIC DIAGRAM : -12V,+12V,30V VAR

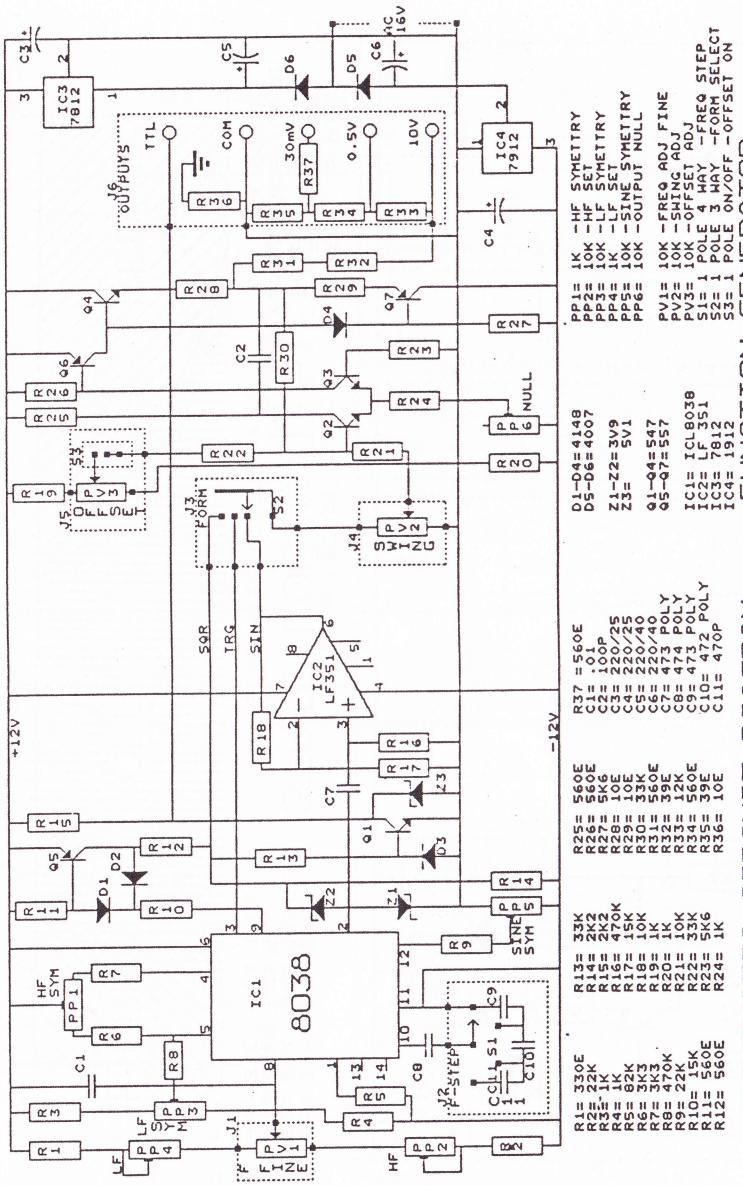


SCHEMATIC DIAGRAM : LOGIC SOURCE

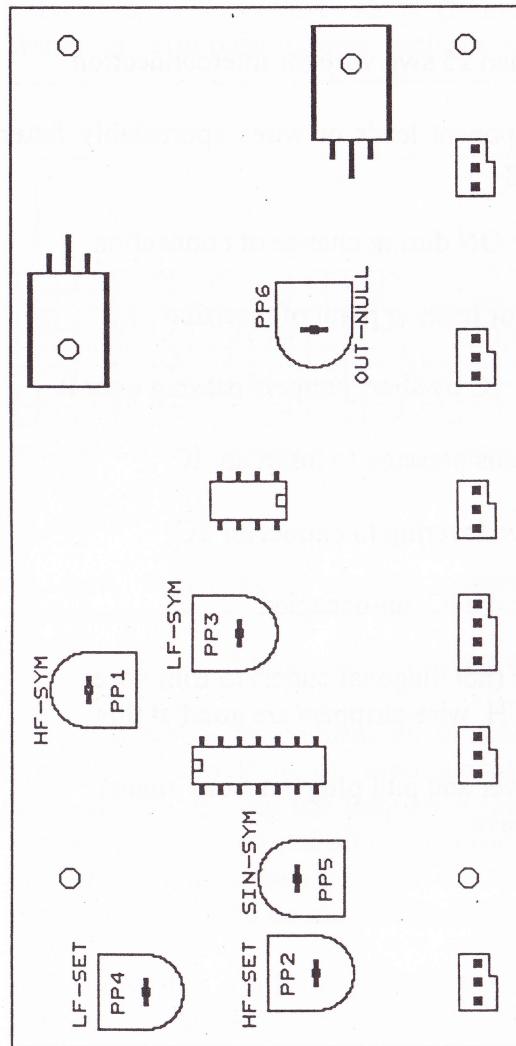


SCHEMATIC DIAGRAM : CLOCK GENERATOR





SCHEMATIC CIRCUIT DIAGRAM : FUNCTION GENERATOR



OSCILLOSCOPE	FORM	SW	OFFSET VAR	FREQUENCY MULT VAR	SWING	ADJUST	TO GET
5VDC VERT HOR	TRIANGLE	OFF	X	100 20	HALF	PP1 PP2	+SLOPE = -SLOPE PERIOD = 10 DIVN
-DO-	-DO-	-DO-	-DO-	-DO-	-DO-	-DO-	-DO-
-DO-	5mS	-DO-	-DO-	-DO- 2	-DO-	PP4	-SLOPE = 5 DIVN
-DO-	-DO-	-DO-	-DO-	-DO-	-DO-	PP3	+SLOPE = 5 DIVN
-DO-	5μS	-DO-	-DO-	10K 20	-DO-	PP2	10 PERIODS IN 10 DIVN
-DO-	.1mS	SINE	-DO-	100 20	-DO-	PP5	SYMMETRICAL SINE WAVE
20mV -DO-	-DO-	-DO-	-DO-	-DO- -DO-	ZERO	PP6	ZERO DC

## DO's and DON'Ts

- **DON'T** Use other than 25 swg wire for interconnection
- **DON'T** Insert component leads or wires appreciably fatter than 25 swg
- **DON'T** Keep power ON during change of connection
- **DON'T** Bend wires or leads at point of insertion
- **DON'T** Entangle an IC by short jumpers passing over it
- **DO** Apply simultaneous pressure to insert an IC
- **DO** Apply successive levering to extract an IC
- **DO** Keep holes near the IC un-occupied
- **DO** Use shear cutter (not diagonal cutter) to trim wires  
MULTITECH wire-strippers are good at this
- **DO** Switch OFF power and pull plug out from mains when you leave

## USING OSCILLOSCOPE

Figure 25 depicts how a free running sweep produces different waveform in successive scans (frame-1 to 3) and how these frames superimpose to form multiple wave display on screen.

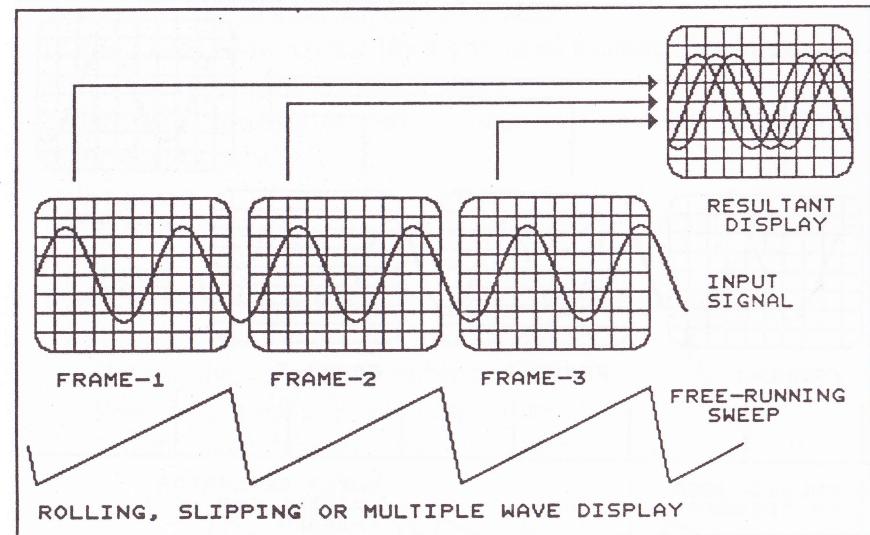


Figure 25 : Slipping waveform

To get a stable waveform on the screen, the sweep frequency must be a submultiple of input signal frequency. This could be done slowly varying the frequency (and obviously the slope) of the sweep. But then stability is lost for very little change of either of them (input or sweep). Also the sweep calibration is lost i.e. time per division is no more calibrated.

In present day oscilloscopes the sweep slope is not modified. Instead the sweep start is delayed until a particular position of the input arrives. So sweep frequency is varied without changing the slope.

## HOW

A train of narrow pulses are generated by a comparator which compares input with a user variable (trigger level) internal DC voltage. After completion of a sweep a flip-flop is reset. The next trigger pulse sets the flip-flop which then starts a sweep.

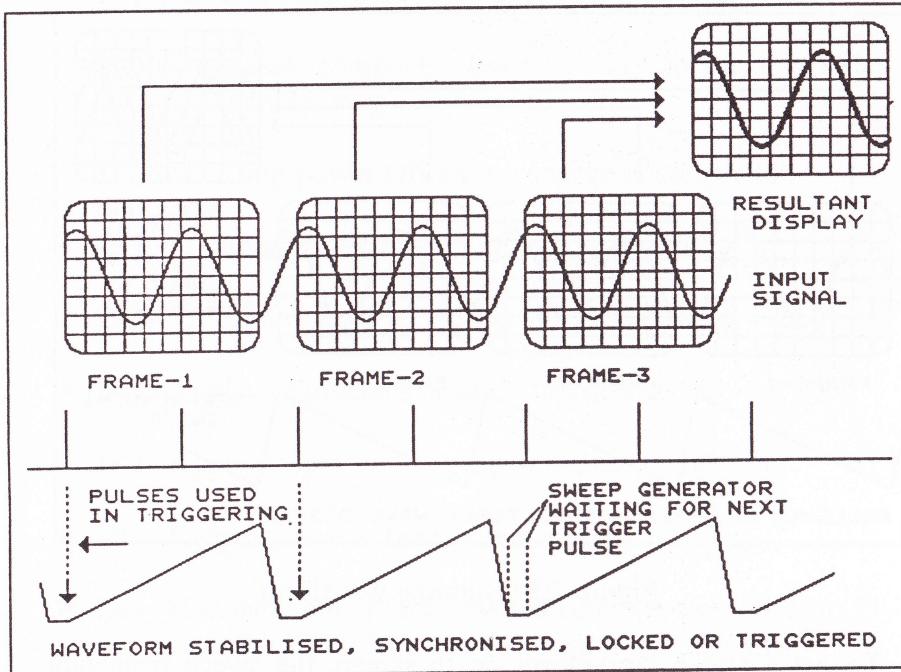


Figure 26 : Stabilised waveform

However in this scheme if there is no input signal no sweep runs and user loses the visible straight trace. To overcome this problem a trigger hold-off circuit starts a sweep after a preset time (trigger hold-off time) if no trigger pulse is available. This mode of operation is called AUTO. The other mode is NORMAL.

So in NORMAL mode no signal no trace. This mode is used only to view single pulses or very low frequency pulses.

## USER CONTROLS TO GET A STABLE WAVEFORM

Select trigger source INT / EXT CH1 / CH2 as suits.

Trigger slope + / -- as wanted.

Adjust trigger level until stabilised.

Sometimes the display appears as a band.

If it consists of horizontal lines you need to compress in time i.e. move sweep control anticlock wise.

If the band consists of vertical lines you need to move sweep control clock wise.

## READING SEQUENTIAL BINARY DATA WITH CRO

Consider the 5 signals (fig. 27) of a sequence generator.

The problem can be divided into three parts

Getting the waveforms stable on CRO.

Reading the states in successive time slices.

Constructing the waveform on paper.

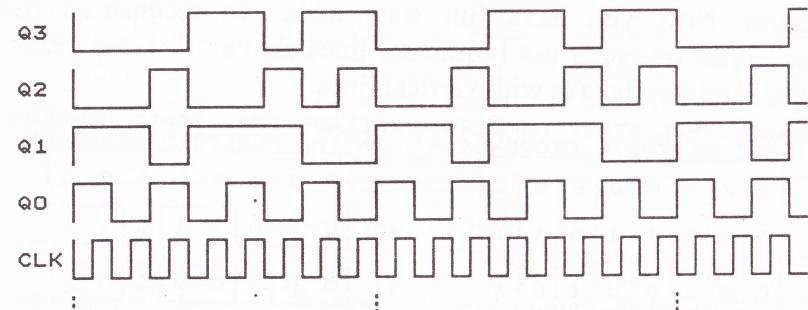


Figure 27 : Multiple binary waveforms

As the CRO has only two traces you can see only two waveforms at one time.

Set CRO

Mode = Dual and Chop

Vertical = 2V/divn

Trig source = CH1

Slope = -ve

Find the signal having least number of transitions i.e. lowest frequency (Q3 in this case). Put it to CH1. Put CLK to CH2. Get a High-to-Low edge stable at left of display. CH1 will show overlapping random sequences. Adjust Sweep-Step and Sweep-Var to get a stable complete period on CH1 and one pulse per time division on CH2. Note now that all transitions of CH1 coincide with vertical graticule lines. Now mark (imagine) the graticule divisions as t0, t1, t2 etc. These timing marks remain valid so long CH1 signal remains same and no controls of CRO moved further. Make a table (5 rows and 8 columns in this case, fig 28). Read the state of CH1 in each time division and note in the table at Q3 row. Take out CH2 probe (CH1 display will remain undisturbed) and put it to Q0. Read CH2 status and fill Q0 row. This way complete the table by reading all other signals. Now you have full state table. To reconstruct the waveforms on paper put horizontal lines above "1" s and below "0"s. And join breaks with vertical lines.

HEXADECIMAL STATE NUMBERS IN THE PERIODIC SEQUENCE									
	3	2	5	A	B	6	9	C	
Q3	0	0	0	1	1	0	1	1	
Q2	0	0	1	0	0	1	0	1	
Q1	1	1	0	1	1	1	0	0	
Q0	1	0	1	0	1	0	1	0	
CLK									

HEXADECIMAL STATE NUMBERS IN THE PERIODIC SEQUENCE									
	3	2	5	A	B	6	9	C	
Q3	0	0	0	1	1	0	1	1	
Q2	0	0	1	0	0	1	0	1	
Q1	1	1	0	1	1	1	0	0	
Q0	1	0	1	0	1	0	1	0	
CLK									

Figure 28 : Tabular data mapping

