01205242 Electronic circuit &System 1

Report on

Final project 2nd semester year 2564

Made by

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Present to

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Preface

This report is a part of 01205242 Electronic circuit &system 1, Semester 2/2564. The report included experiment result, theory and conclusion of Electronic circuit &system's Midterm project. If there are any mistake occurred in the report, we would like to apologize here and now.

Jakkaphob Kongthanarith

1. Circuit's condition

1. let Amplifier ($A_v = V_0/V_s$) have extension rate more or equal to 10 times ($|A_v >= 10|$).

2. the circuit can maintain extension rate in condition 1 in the given temperature.

3. Output signal (V_0) have to be 'Sine' signal.

4. Supply voltage (V_{cc}), Signal input scale (V_a), Output signal frequency (f_{in}), Load resistance (R_L) and temperature (Temp) will be given in the chart below.

V_{cc}	V_a	f_{in}	R_L	Temp
5 V	75 mV	1 KHZ	50	60

2. State and calculate parameters

The transistor that will be used in the project is transistor code 2N2222 which it's data sheet will be shown below

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	75	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	600	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	75	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	—	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{CEX}	—	10	nAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	 — —	 0.01 10	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	10	nAdc
Collector Cutoff Current (V_{CE} = 10 V)	I_{CEO}	—	10	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{BEX}	—	20	nAdc

Since the Datasheet information are calculated by given T = 25C, we will need to recalculate H_{FE} at Temperature 60C using equation below

$$H_{FETemp} = H_{FEMax} \times [1 + (T_{actual} - 25^\circ C)*0.0058]$$

Minimum HF E = 50 at 25◦C and for the maximum HF E = 150 at 75◦C yields an HF ET emp of 194 and VBE of 0.50V

Load line and Q-point

A static or DC load line can be drawn onto the output characteristics curves of the transistor to show all the possible operating points of the transistor from fully "ON" ($I_C = V_{CC}/(R_C + R_E)$) to fully "OFF" ($I_C = 0$). The quiescent operating point or **Q-point** is a point on this load line which represents the values of I_C and V_{CE} that exist in the circuit when no input signal is applied. Knowing V_B, I_C and V_{CE} can be calculated to locate the operating point of the circuit as follows:

$$V_E = V_B - V_{BE}$$

So, the emitter current,

$$I_E \approx I_C = \frac{V_E}{R_E}$$

$$\text{and } V_{CE} = V_{CC} - I_C(R_C + R_E)$$

It can be noted here that the sequence of calculation does not need the knowledge of β and I_B is not calculated. So the Q-point is stable against any replacement of the transistor.

Since the aim of any small signal amplifier is to generate an amplified input signal at the output with minimum distortion possible, the best position for this Q-point is as close to the centre position of the load line as reasonably possible, thereby producing a Class A type amplifier operation, i.e. $V_{CE} = 1/2V_{CC}$.

3. Design stage

I will integrate circuit in to 'Multistage Amplifier' that have 4 stages, which is

Stage 1: Common Collector

Stage 2 and 3: Common Emitter

Stage 4: Darlington Configuration

The calculation part will be done from part 4 to part 1.

- Stage 4: Darlington Configuration

Find H_{FETemp} from $H_{FETemp} = H_{FEMax} \times [1 + (T_{actual} - 25°C)*0.0058]$

$$H_{FETemp} = 300\times [1 + (60°C - 25°C)*0.0058] = 360.9$$

Find V_{CEQ}: $V_{CEQ} = V_{cc}*0.5 = 5/2 = 2.5V$

Use KVL in order to find V_E

$$V_E = 5 – 2.5 = 2.5 \text{ V}$$

Let R_B = 70 Ω and calculate for R_B

$R_B = (360.9 + 1)^2 * (70/10) = 916.801$ k Ω

Calculate $I_{E2} = V_E/R_E = 2.5/70 = 35.7$ mA

Use KCL in the circuit $I_{E2} = (\beta + 1)^2$ and find I_{B1} : $I_{B1} = 38.5\text{mA}/360.9^2 = 0.29\ \mu\text{A}$

By observing the circuit, we know it's Thevenin's Theorem and use these formular below to find R_1 and R_2 :

$V_{TH} = (R_2/(R_1+R_2))*V_{cc}$

$R_B = (R_1*R_2)/(R_1+R_2)$

KVL : $-V_{TH} + I_B R_{B + 2V}BBQ + V_E = 0$

$V_{cc}R_{B/}R_1 = I_B R_{B +} 2V_{BEQ} + V_E$

Calculate R_1: $(5*916.801\text{ k})/R_1 = 0.29\text{u}*916.801\text{ k} + 1.4 + 2.5$

$R_{4,1} = 1099019.413\ \Omega = 1099.019$ k Ω

$R_{4,1} = 1.099$ M Ω

Calculate R_2: $R_B = (R_1*R_2)/(R_1+R_2)$

$916.801\text{ k} = (1099019.413 *R_2)/(1099019.413 +R_2)$

$R_{4,2} = 5529530.562\ \Omega = 5529.53$ k Ω

$R_{4,2} = 5.53$ Meg

Observe the Small Signal Model

$r_{\pi 1} = V_T/I_{B1} = kT/qI_{B1} = ((1.38*10^{-23})*(60+273.15))/(1.152*10^{-19})*(1.152*10^{-6}))$

$= 99083.4\ \Omega = 99.083$ k Ω

$r_{\pi 2} = V_T/I_{B2} = kT/qI_{B1} = ((1.38*10^{-23})*(60+273.15))/(1.16*10^{-19})*(360.9+1)*(1.18*10^{-6}))$

$= 273.78\ \Omega$

$Z_{in4} = R_1||R_2||(r_{\pi 1}+(\beta+1))[r_{\pi 2}+(\beta+1)(R_E||R_L]) = 808811.82\ \Omega = 808.811$ k Ω

Stage 4 Extension rate

$A_{vi} = (181.45)^2(29.16)/((34.642\text{k}+181.45)*(95.7+(181.45*29.16)) = 0.918$

Calculate capacitor

Calculate C in Cut-Off period $C = 1/2\pi fR$

Since we want transistor conduct electricity, C need to be equal or more than $1/2\pi fR$

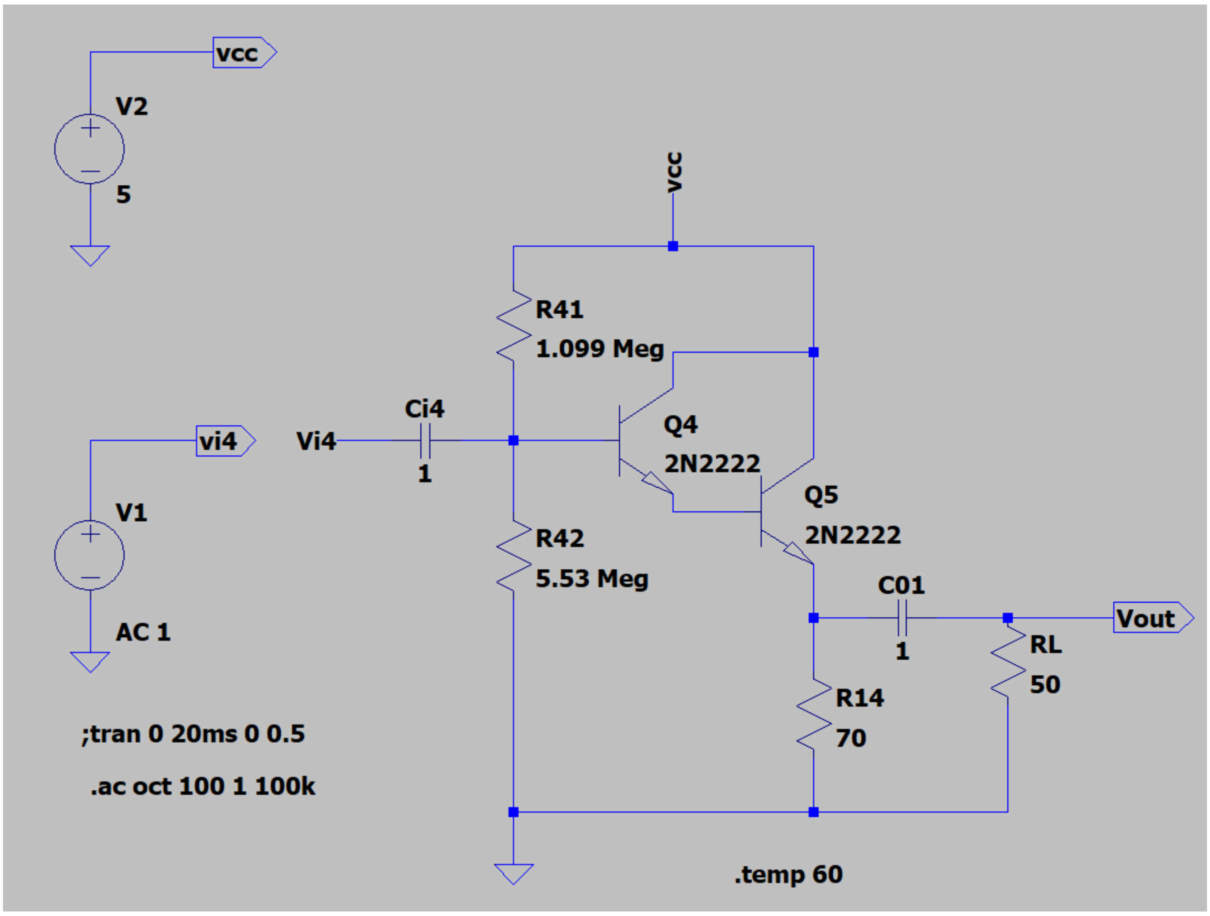
$C >= 1/2\pi fR$

Thus $C_{i4} >= 1/2\pi1000*808811.82$

$C_{i4} >= 1.96776*10^{-10}$ F

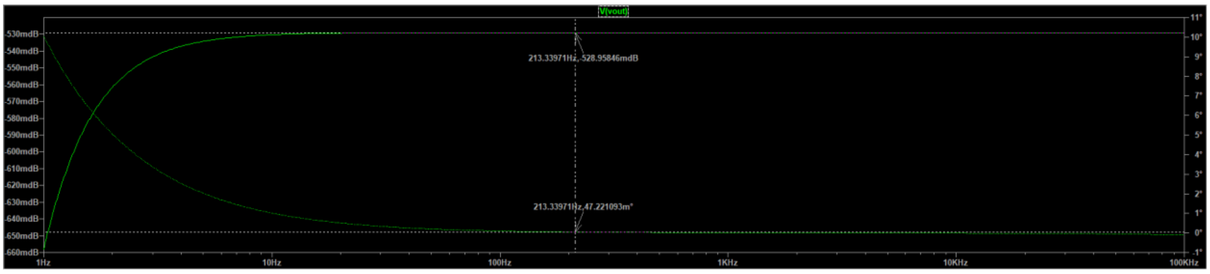
$C_0 >= 1/2\pi1000*70 = 2.27$ µF

Stage 4 circuit



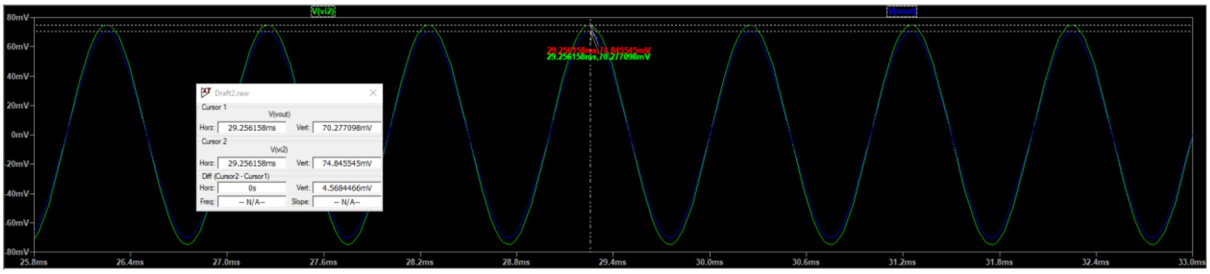
Stage 4 Simulation result

1. Operating point & Analysis



- The graph above shown its frequency response as High Pass Filter with Magnitude = -528.92mdb when frequency more than 1khz and phase = 0 when frequency closer to infinity

2. Circuit extension rate



Extension rate = 70.27/74.84 = 0.938 which Is close to A_{vi} that I've calculated, 0.918

<u>- Stage 3 : Common Emitter</u>

Let R_E = 5000 Ω and A_{vi} = -5

H_{FETemp} from $H_{FETemp} = H_{FEMax} \times [1 + (T_{actual} - 25^\circ C)*0.0058]$

$$H_{FETemp} = 300\times [1 + (60^\circ C - 25^\circ C)*0.0058] = 360.9$$

V_{cc} = 5, VCEQ = 2.5V

Calculate R_c

$$A_{vi} = -(R_c || Z_{in})/R_E$$

$$-5 = -(R_c || Z_{in})/5000$$

$$Rc = 25797.3853\ \Omega = 25.797\ k\ \Omega$$

Use KVL in order to find I_c and I_B

$$I_c = (5-2.5)/(5k+25797.3853)$$

$= 8.117*10^{-5} = 0.811\ \mu A$

$I_B = I_c/\beta = 8.117*10^{-5}/360.9$

$= 2.249258*10^{-7} = 0.2249\ \mu A$

In order to make the circuit stabilize, we need to make Rb value equal 10 time of (β+1) R_E

$R_B = (360.9+1)*(5k/10) = 180950 = 180.95\ k\ \Omega$

Use KVL in order to find R_1

$(5*180950)/R_1 = (2.249258*10^{-7}*180950)+ 0.7+8.117*10^{-5}*5000$

$904750/R_1 = 11.4655$

$R3,_1 = 789106.2271\ \Omega = 798.106\ k\ \Omega$

$R3,_2 = 234951.6238\ \Omega = 234.951\ k\ \Omega$

Observe the Small Signal Model

$r_{\pi} = V_T/I_{B1} = kT/qI_{B1} = ((1.38*10^{-23})*(60+273.15))/((1.6*10^{-19})*(2.249258*10^{-7}))$

$= 127749.629\ \Omega = 127.749\ k\ \Omega$

$Z_{in3} = R_1||R_2||(r_{\pi1}+(\beta+1)R_E)= 181046.2068||1937249.629$

$= 165572.5754\Omega = 165.572\ k\ \Omega$

Extension rate :

$A_{vi} = (-360.9)*(25797.3853||165572.5754)/(127749.629+361.9*5000)$

$= (-360.9*22319.80143)/(127749.629+361.9*5000)$

$= -4.15$

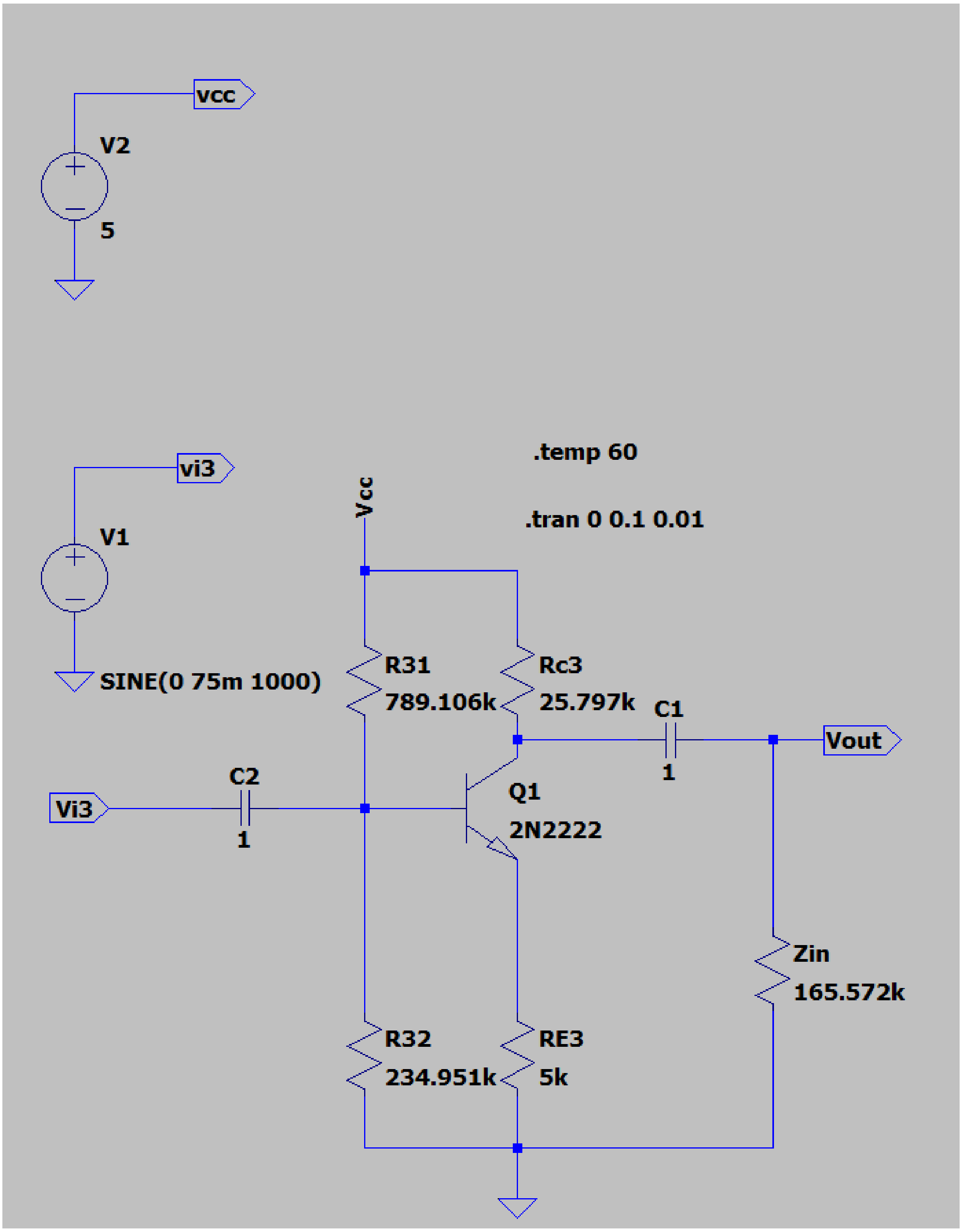
Since we want transistor conduct electricity, C need to be equal or more than $1/2\pi fR$

$C >= 1/2\pi fR$

Thus $C_{i3} >= 1/2\pi1000*165572.5754$

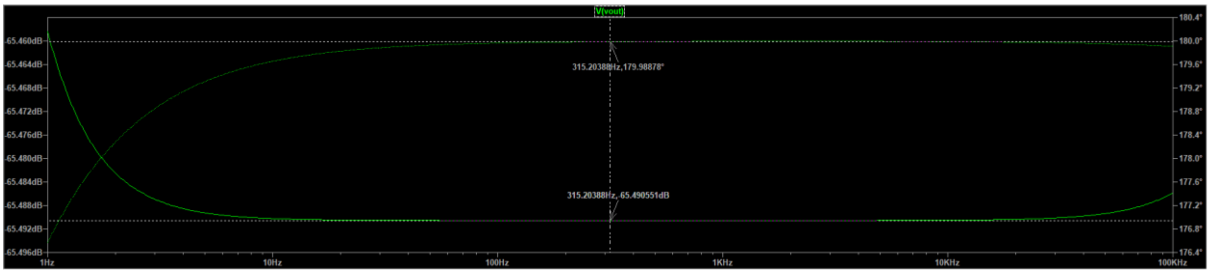
$C_{i3} >= 9.61239*10^{-10}$ F

Stage 3: Circuit design



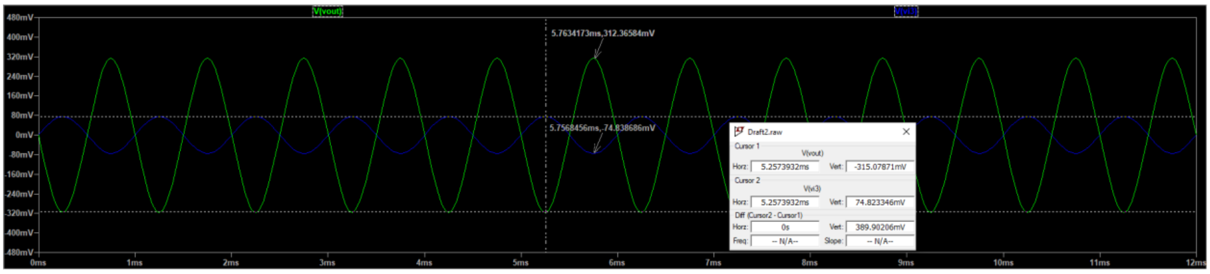
Stage 3 simulation result

1. Operating point & Analysis



The graph above shown its frequency response as High Pass Filter with Magnitude = --65.45 dB when frequency less than 1khz and phase = 179.98 when frequency at 1kHz

2. Circuit extension rate



Extension rate = -312.365/74.838 = -4.1738 which Is close to A_{vi} that I've calculated, -4.15

<u>-Stage 2 : Common Emitter</u>

Let A_{vi} = -3 and R_E = 4000

H_{FETemp} from $H_{FETemp} = H_{FEMax} \times [1 + (T_{actual} - 25∘C)*0.0058]$

$H_{FETemp} = 300\times [1 + (60∘C - 25∘C)*0.0058] = 360.9$

V_{CEQ} = 2.5V

Let A_{vi} = -3 and R_E = 4000 Ω = 4k Ω

-3 = - (R_c || Z_{in})/4000

-3 = - (R_C || 165572.5754) / 4000

Rc = 1986870905/153572.5954

R_c = 12937.66742 Ω = 12.937 k Ω

Using KVL to find I_C and I_B

$I_c = (5-2.5)/(4000+12937.66742)$

$I_c = 1.476*10^{-4}$

$I_B = (1.476*10^{-4})/360.9$

$= 4.089776*10^{-7}$ A = 0.4089 μ A

In order to make the circuit stabilize, we need to make Rb value equal 10 time of (β+1) R_E

$R_B = (360.9+1)*(4000/10) = 144760 = 144.76$ k Ω

Use KVL in order to find R_1

$(5*144760)/R_1 = (4.089776*10^{-7}*144760)+ 0.7+1.476*10^{-4}*4000$

$723800/R_1 = 1.3496$

$R_1 = 536305.62$ Ω = 536.305 k Ω

$R_2 = 198278.3002 = 198.278$ k Ω

Observe the Small Signal Model

$r_{\boldsymbol{\pi}} = V_T/I_{B1} = kT/qI_{B1}= ((1.38*10^{-23})*(60+273.15))/(1.6*10^{-19})*(4.089776*10^{-7}))$

$= 70258.58507$ Ω = 70.258 k Ω

$Z_{in2} = R_1||R_2||(r_\pi+(\beta+1)(R_E)$

$= 144759.1811||70258.58507+(361.9*4000)$

$= 144759.1811 || 1517858.585$

$= 132155.43$ Ω = 132.155 k Ω

Extension rate :

$A_{vi} = -(360.9)*(12937.66742||132155.43)/(70258.58507+361.9*4000)$

$= -(360.9*11784.04095)/ 1517858.585$

$= -2.801$

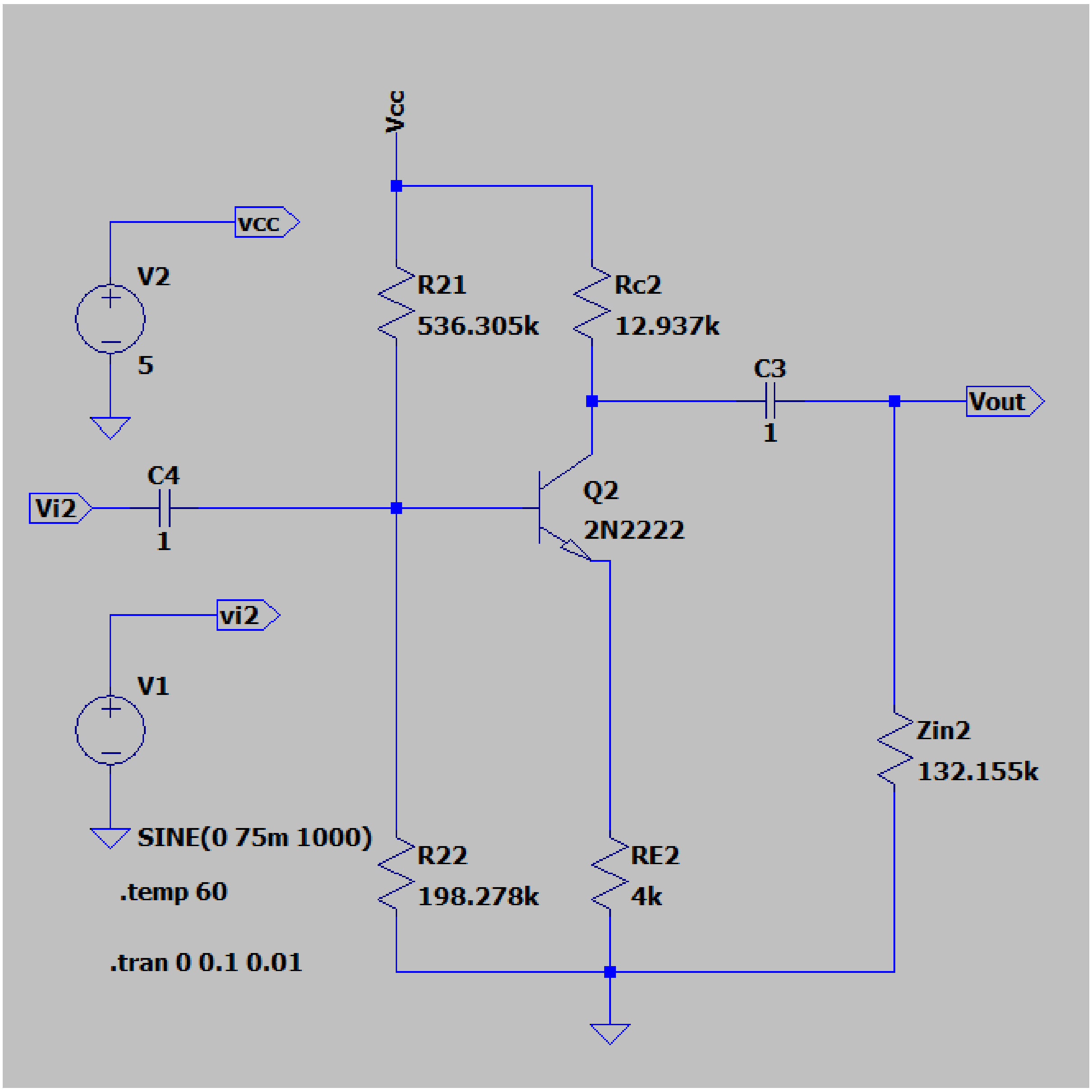
Since we want transistor conduct electricity, C need to be equal or more than $1/2\pi fR$

$C >= 1/2\pi fR$

Thus C_{i3} >= $1/2\pi1000*51462.4415$

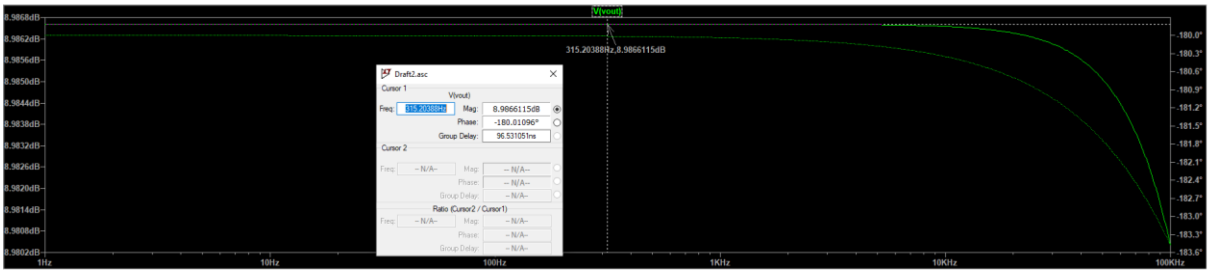
C_{i3} >= $3.09 * 10^{-9}$ F

Stage 2 circuit design



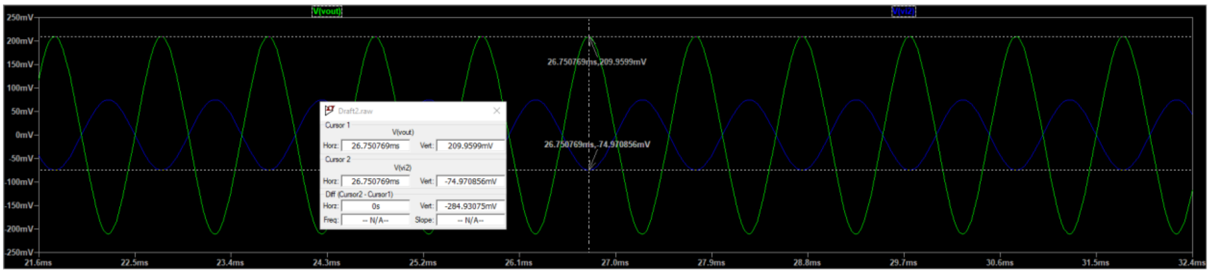
Stage 2 Simulation result

1. Operating point & Analysis



The graph above shown its frequency response as Low Pass Filter with Magnitude = 8.98dB when frequency less than 1khz and phase = -180.01 when frequency at 1kHz

2. Circuit extension rate



Extension rate = 209.96/74.97 = -2.80058 = -2.801 which Is equal to A_{vi} that I've calculated, -2.801

<u>Stage 1 : Common Collector</u>

Let R_E = 100k and A_{vi} = 1

H_{FE} = 360.9, V_{CEQ} = 2.5 v

I_{E2} = V_e/R_E = 2.5/100000 = 0.25 μ A

Thus, I_B = $0.25*10^{/}360.9 = 6.927*10^{-8}$

Use KVL to obtain R_B

$R_B = 5-2.5-0.7/(6.927*10^{-8})$ = 25985275.01 Ω = 25985.275 k Ω

Observe the Small Signal Model

$r_\pi = V_T/I_{B1} = kT/qI_{B1} = ((1.38*10^{-23})*(60+273.15))/(1.6*10^{-19})*(0.4156*10^{-6}))$

= 69139.04 Ω = 69.139 k Ω

$Z_{in1} = R_B||(r_\pi+(\beta+1)(R_E)||R_{in2})$

$= 25985275.01 \mid\mid 69139.04 + 361.9*23738.88$

$= 25985275.01 \mid\mid 8660241.684$

$= 8591045.129\ \Omega = 8591.045\ k\ \Omega$

Extension rate :

$A_{vi} = (360.9)*(100000 \mid\mid 8591045.129)/(69139.04+361.9*(10000 \mid\mid 8591045.129))$

$= 360.9*98849.3904/35842733.39$

$= 0.9953$

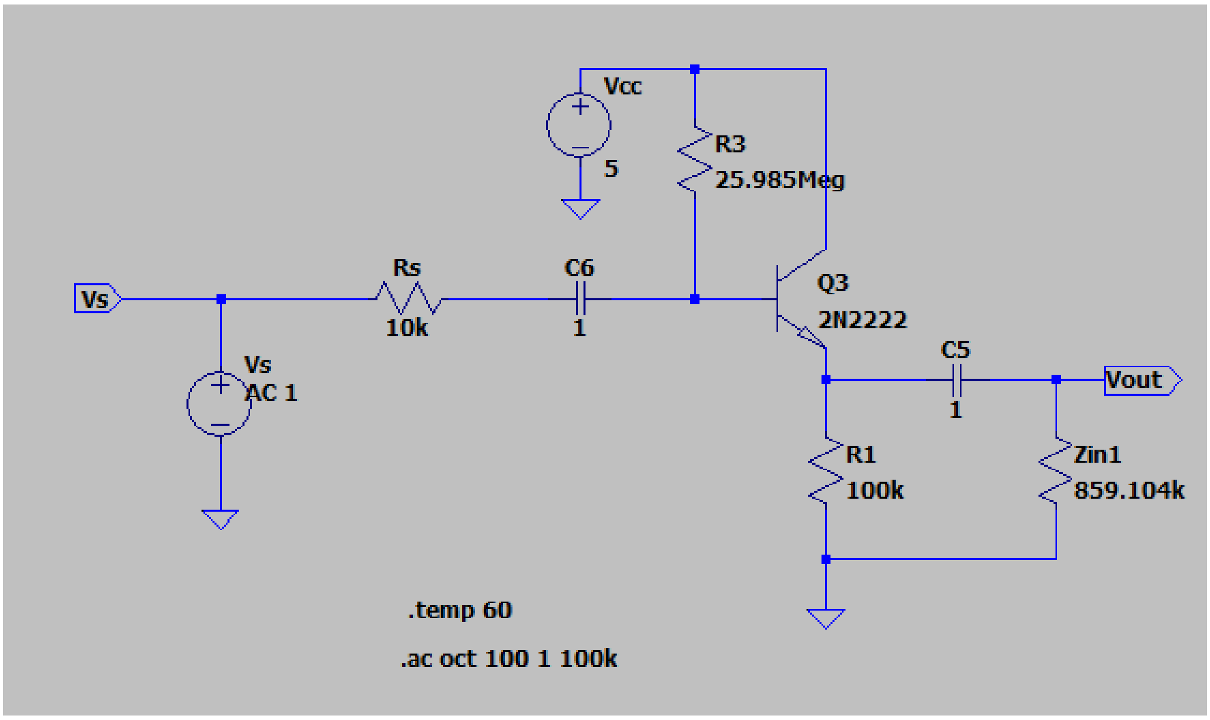
Since we want transistor conduct electricity, C need to be equal or more than $1/2\pi f R$

$C >= 1/2\pi f R$

Thus $C_{i3} >= 1/2\pi 1000*69139.04$

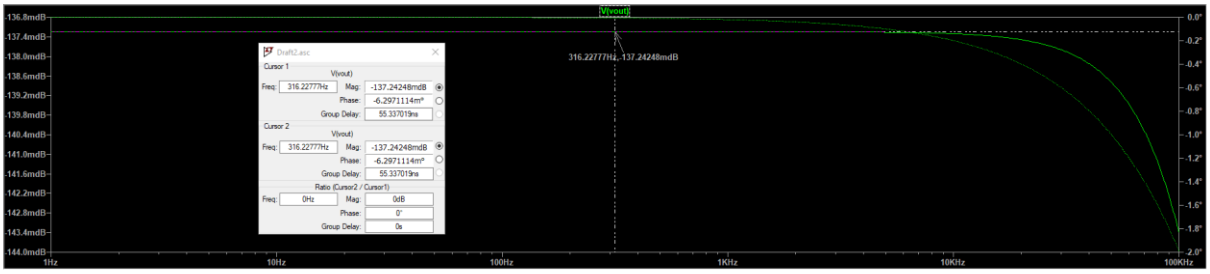
$C_{i3} >= 2.302*10^{-9}$ F

Stage 1 Circuit Design



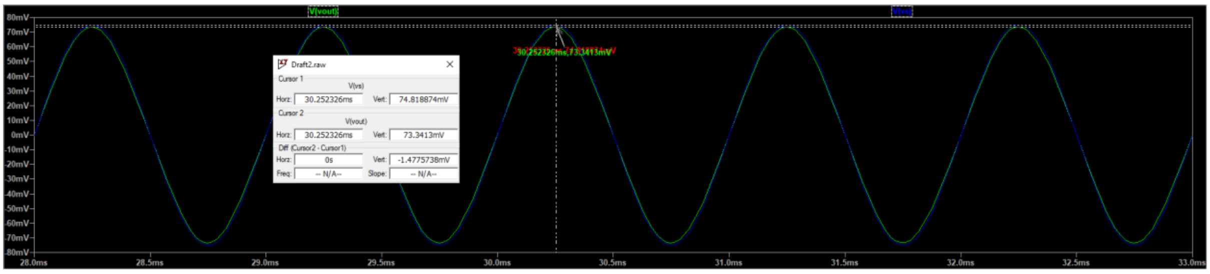
Stage 1 simulation result

1. Operating point & Analysis



The graph above shown it's frequency response as Low Pass Filter with Magnitude = -137.24 mdB when frequency less than 1khz and phase = -6.29 when frequency at 1kHz

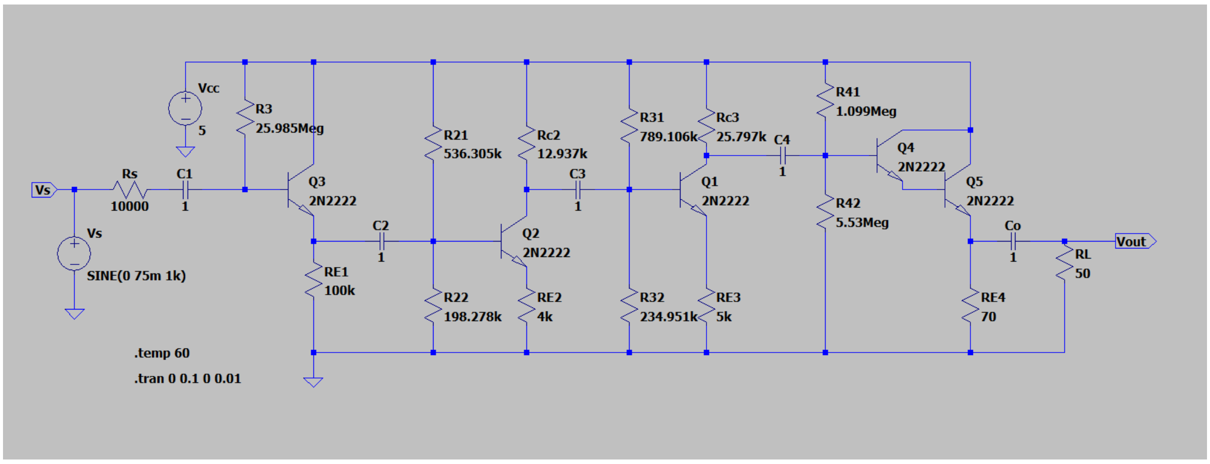
2. Circuit extension rate



Extension rate = 73.578/74.9226 = 0.98205 which Is close to A_{vi} that I've calculated, 0.9953

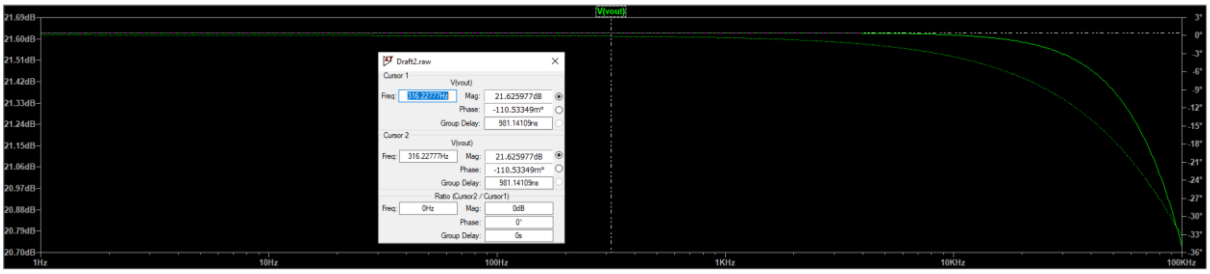
4. Final Result

1. Multistage Amplifier



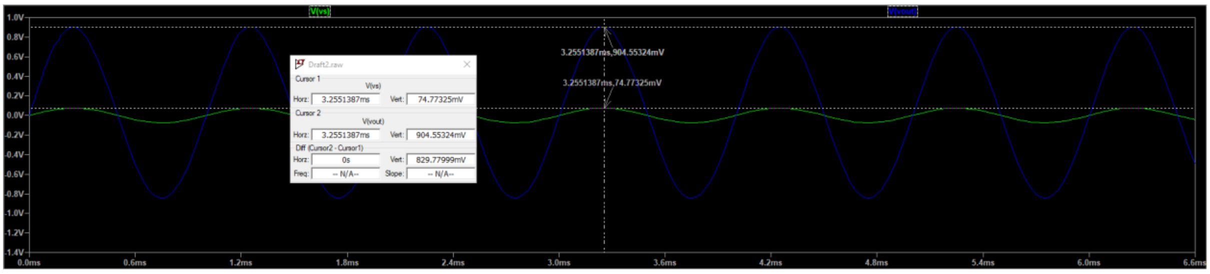
2. Simulation Result

1. Operating point & Analysis



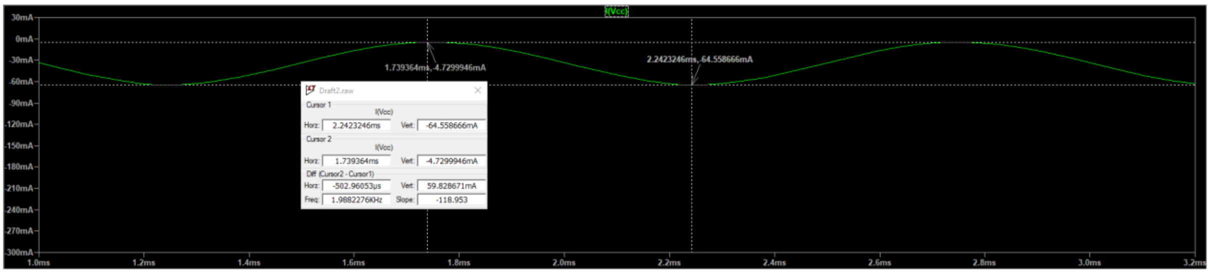
The graph above shown it's frequency response as Low Pass Filter with Magnitude = 21.6259 dB when frequency less than 1khz and phase = -110.533 when frequency at 1kHz

2. Circuit extension rate



Extension rate = 904.553/74.773 = 12.09 which is according to the requirement, which is Extension rate more than 10.

3. Current graph from V_{cc}



V_{ERT} = 59.82 mA

Conclusion

This is BJT circuit were built in order to expand small signal with also achieved all project requirement. The output of this circuit is a sine wave with error less than 3%. The A_{vi} is 0.918, -4.15, -2.801, 0.995 when all of them multiply together, the value will be 10.617, which is more than the requirement (10). Stage 1 and 4 A_{vi} can't be more than 1 since output are pulled by the emitter leg, resulting in calculation of resistor that can active the transistor. 2N2222 Transistor is used because of the fact that its specs are according to project requirement

4 Multistage Amplifier is used in this project, consist of Stage 1: Common Collector, Stage 2-3: Common Emitter, Stage 4: Darlington Configuration. Calculation part is start by define A_{vi} and R_E value, then calculate the other variables. When we got each resistance needed, we use them in the small signal equation in order to find it's real extension rate.

Stage 4 A_{vi} = 0.938 which is close to calculated A_{vi}, 0.918

Stage 3 A_{vi} = -4.173 which is close to calculated A_{vi}, -4.15

Stage 2 A_{vi} = -2.801 which is equal to calculated A_{vi}, -2.801

Stage 1 A_{vi} = 0.982 which is close to calculated A_{vi}, 0.995

$A_{vi,all}$ = 0.918*-4.15*-2.801*0.995 = 10.61