

Electronics Laboratory

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Lab 5 – Digital

Name	Jakob Haverkamp	Reg. Nr.	5932110
Name	Milan Fark	Reg. Nr.	5900383

Score and comments (only for tutors, please leave blank)

Please fill out this cover sheet and submit it with your lab report.

Lab 5 - Bipolars

31. Januar 2026

5.2 Ring oscillator

5.2.1. Simulation

Introduction

This section is about simulating an inverter, built from an N-Channel MOSFET and then simulating a chain made out of three of those inverters. As seen in [Figure 1](#), the source of each transistor is connected to *GND*, while the drain is connected to a *pull-up* resistor. The gate of the first transistor is connected to the input, in this case a *LogiSim PIN* element, while the gate of the other transistors is connected to the output of the previous one.

Circuit diagrams

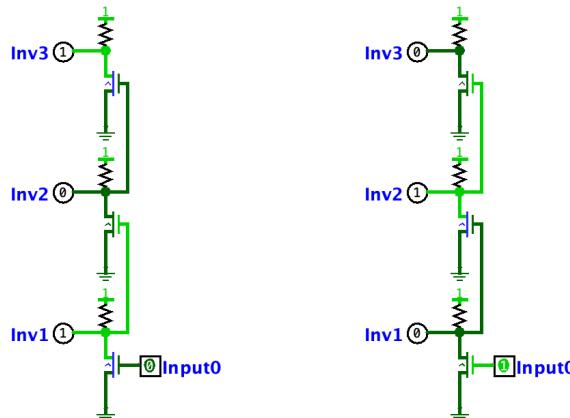


Figure 1: LogiSim circuit diagrams with *input* = 0 (left) and *input* = 1 (right)¹

Text Questions:

Input0	Inv3	Inv2	Inv1
0	1	0	1
1	0	1	0

Table 1: Screenshot of the truth table from *LogiSim*

¹I am on M1 Mac and therefore could not use original LogiSim, I had to download and compile LogiSim-evolution from GitHub instead, but I could follow all the Lab instructions the same, but that's the reason the table and circuit diagram may look different than expected. Also, in LogiSim-evolution i was unable to name the input "input" and so had to name it "input0".

When the input is 0, the output is just connected to the *pull-up* resistor and is therefore 1, when the input is 1, the MOSFET opens and connects the output to *GND*. In the logic table, we can therefore see an alternating pattern between 0 and 1 for input and output respectively.

Conclusion

We successfully simulated the inverter and inverter chain in LogiSim² and generated the truth table, which showed an alternating sequence of 0 and 1 due to its inverting nature.

5.2.2. Measurement

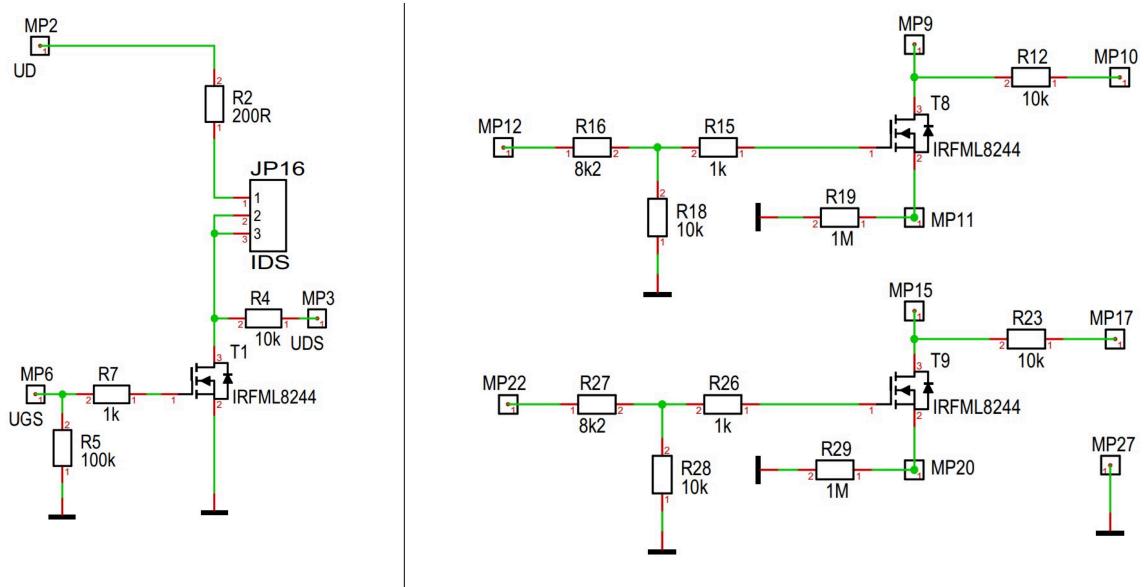
Introduction

In this section, we first build inverter chain and then a ring-oscillator from three MOSFETs, which were all used as inverters.

Two of the three are located in the *MOSFET logic gates* section, the other in the *MOSFET characteristics* circuit, as can be seen in [Figure 2](#).

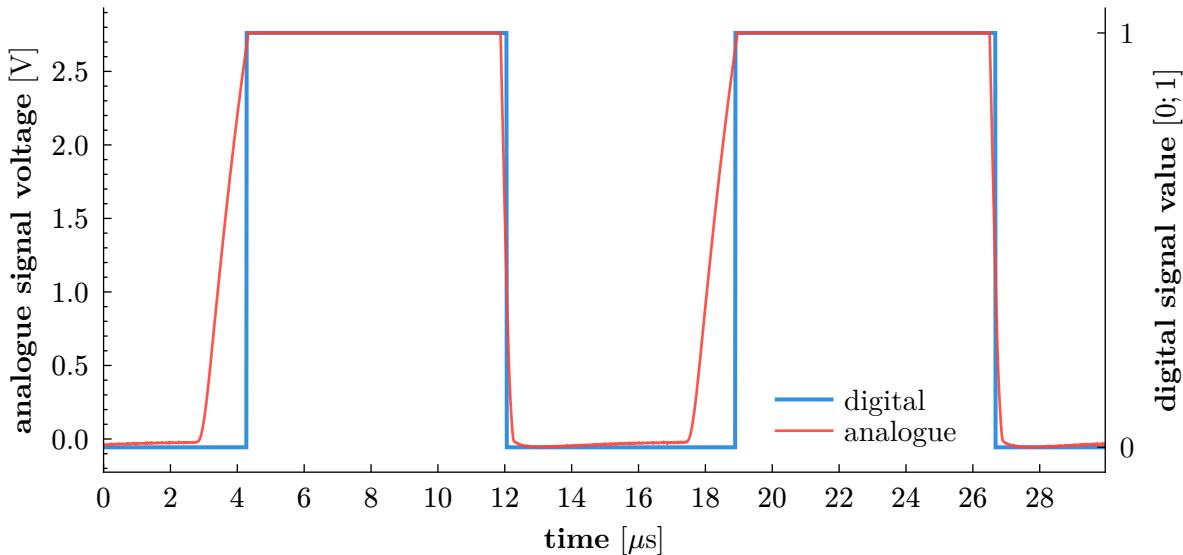
For *Inv1*, which had the closest duty cycle to 50%, we also looked at the shape of the digital vs analogue signal, which can be seen in [Figure 3](#).

Circuit diagrams:



[Figure 2](#): Schematic of the *MOSFET characteristics* circuit (left) and the *MOSFET logic gates* circuit (right)

²Quite a cool program in our opinion!!

PlotsFigure 3: analogue and digital signal course of $Inv1$ over $2.2 \cdot \tau_i = 2.2 \cdot 13.62 \mu\text{s} = 29.96 \mu\text{s}$ **Text questions:**

V_{in}	Inv_1	Inv_2	Inv_3
0	1	0	1
1	0	1	0

Table 2: Truth table of V_{in} , Inv_1 , Inv_2 , and Inv_3

We can see the alternating behavior of the inverters in [Table 2](#), where every signal is the inverted value of the previous.

The time from the first transistor to the third transistor in the chain switching was:

$$t_{pd,rise} = 6.91 \mu\text{s}$$

$$t_{pd,fall} = 7.67 \mu\text{s}$$

From which we estimated the ring-oscillator frequency:

$$f = \frac{1}{7.67 \mu\text{s} + 6.91 \mu\text{s}} = \frac{1}{14.58 \mu\text{s}} = 68.59 \text{ kHz}$$

	$T_{L,i} [\mu\text{s}]$	$T_{H,i} [\mu\text{s}]$	$\tau_i [\mu\text{s}]$	$f_i [\text{kHz}]$	$p_i [\%]$
$Inv1$	6.44	7.18	13.62	73.42	52.72
$Inv2$	4.52	9.08	13.60	73.53	66.76
$Inv2$	8.38	5.24	13.62	73.42	38.47

Table 3: Truth table of V_{in} , Inv_1 , Inv_2 , and Inv_3

As seen in [Table 3](#), $Inv1$ has the closest duty cycle to 50% with 52.72% signal high, so we chose $Inv1$ for the plot.

The actual frequency of the ring-oscillator is about 5 kHz higher than the one estimated earlier. For *Inv1* and *Inv3* we have the same frequency of 73.42 kHz, for *Inv2* we calculated 73.53 kHz which is slightly higher. The difference is probably caused by small measuring errors, as the difference in periods is only 20 ns.

The analogue and digital signal values differ in shape as seen in [Figure 3](#). As the digital signal value can only be 1 or 0 the function resembles a square wave. The analogue signal is measured as the voltage. This leads to a function with a slanted rising edge but a nearly instant falling edge. The difference can be explained by the delayed reaction of the transistors.

Conclusion

In this section the difference between analogue and digital signal became apparent in its reaction speed and edge sharpness. The estimated frequency was quite similar to the actual frequency of the ring oscillator. In [Table 3](#), we could clearly see the different duty cycles, ranging from $\approx 38\%$ to $\approx 67\%$.

Also just seeing the ring-oscillator work in real time was very cool.

5.3 NMOS logic

5.3.1. Simulation

Introduction

This section is about simulating three different logic gates, which can all be seen in [Figure 4](#).

Logic circuit 1 has all diode sources connected to *GND* and all drains connected together, with a *pull-up* resistor and the output pin attached.

Logic circuit 2 has all diodes connected in series, so drain to source for each of them, with the first source connected to *GND* and the last drain connected to a *pull-up* resistor and the output pin.

Logic circuit 3 has two transistors connected in series as seen in gate 2, and the third transistor standing alone, again connected to *GND* at the source and both drains connected to the same *pull-up* resistor and output pin.

All three truth tables and logical formula can be seen in [Table 4](#).

Circuit diagrams:

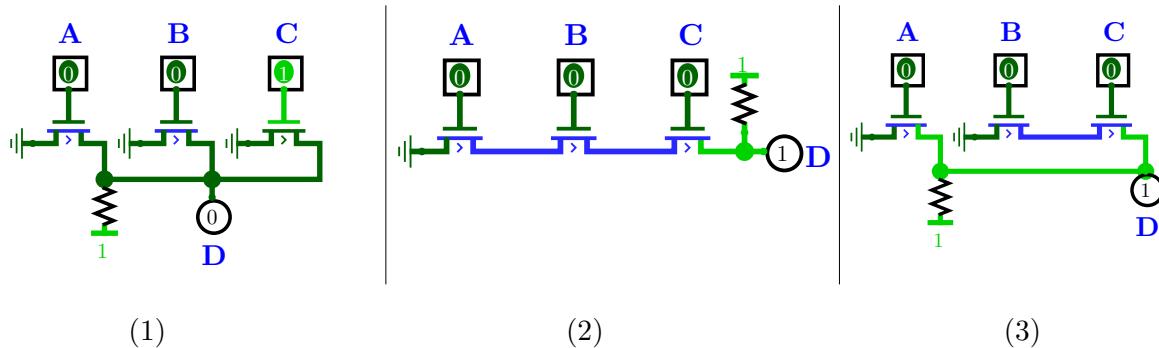


Figure 4: LogiSim-evolution circuit diagrams of the three logic circuits

Text questions:

A	B	C	D
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Logic circuit 1

NOR(A, B, C)

Logic circuit 2

NAND(A, B, C)

Logic circuit 3

 $\overline{A} \cdot \overline{(B \cdot C)}$

Table 4: Truth tables for all three logic circuits

Logic circuit 1 is a standard logic gate, **NOR** to be specific, and **D** is 1 when neither **A** nor **B** nor **C** is active (hence the name), so when even one of them is 1, the output is 0.

Logic circuit 2 is also a standard logic gate, **NAND**, and **D** is 1 when all three inputs are 1 and 0 in all other cases.

Logic circuit 3 is not a standard gate, but its output can be described as $D = \overline{A} \cdot \overline{(B \cdot C)}$ or in words as **NOT A AND NOT (B AND C)** and as seen in the table **D** is 0 for all inputs with **A=1** and 1 for all inputs with **A=0** except **ABC=011**.

Conclusion

We successfully built, simulated and evaluated all three logic circuits and found that circuit 1 and 2 were standard logic gates, namely **NOR** and **NAND**, while the third one was not a standard one, but could be described with the logic formula $D = \overline{A} \cdot \overline{(B \cdot C)}$.

5.3.2. Measurement

Introduction

In this section we measured, analyzed and generated truth tables for three logic circuits similar to the ones simulated in the previous section. For that, we used the same three MOSFETS as in the prior measurement, which can be seen again in the circuit diagram in [Figure 5](#) and connected them to the digital IO of the USB-XLAB.

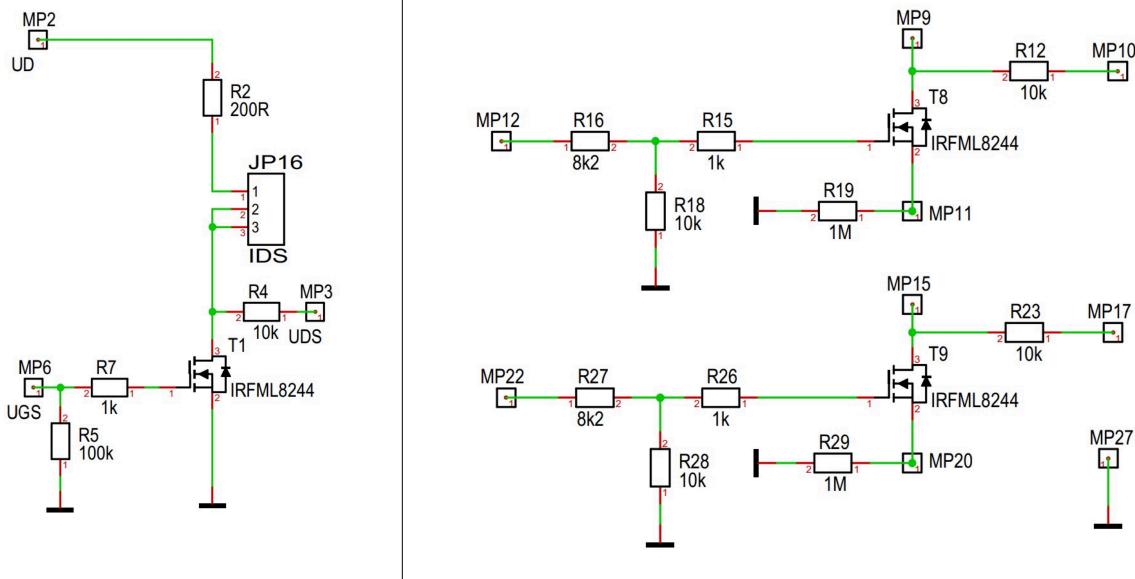
Circuit diagrams:

Figure 5: Schematic of the *MOSFET characteristics* circuit (left)
and the *MOSFET logic gates* circuit (right)

Truth tables

D_0	D_1	D_2	D_{18}
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Logic circuit 1
 $\text{NOR}(A, B, C)$

D_0	D_1	D_2	D_8
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Logic circuit 2
 $\text{NAND}(A, B, C)$

D_0	D_1	D_2	D_8
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Logic circuit 3
 $\overline{D_2} \cdot \overline{(D_0 \cdot D_1)}$

Table 5: Truth tables for logic circuits 1, 2 and 3

Text questions:

The truth tables can be found in [Table 5](#). We can see the same **NOR** and **NAND**-gates we simulated and even have the same third circuit with A corresponding to D_2 , B corresponding to D_0 and C corresponding to D_1 .

Conclusion

We successfully measured the same gates we saw in the simulation, with Logic circuit 1 being a **NOR**-Gate, 2 being a **NAND**-Gate and three being the logic clause: $\overline{D_2} \cdot \overline{(D_0 \cdot D_1)}$, which corresponded to the simulated one with different variables as described in the text questions.