IMTEK
DEPARTMENT OF
MICROSYSTEMS ENGINEERING

universität freiburg

Electronics Laboratory

Winter semester 2025

Lab 5 – Digital

Name ______________________ Reg. Nr. ____________

Name ______________________ Reg. Nr. ____________

Score and comments (only for tutors, please leave blank)

Please fill out this cover sheet and submit it with your lab report.

5 Lab 5 – Digital

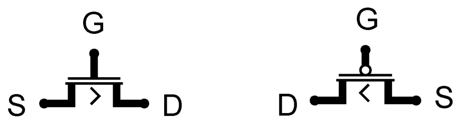
Introduction

In this one digital lab, we will use the components in the electronics kit for the analog labs and reconfigure them into a variety of digital circuits. In two measurement sections, we will first wire up a MOSFET-based inverter chain and then configure it as a ring oscillator. We will subsequently use the three MOSFETs in various configurations, with varying inputs and loads, to realize three different logic functions.

Notes

- The simulations performed in this lab will use *LogiSim*, which is open source software available at www.cburch.com/logisim/download.html. You should download, install and familiarize yourself with it before beginning with the digital modeling.

- Pay attention to the wiring conventions for NMOS and PMOS transistors in *LogiSim*, as shown in Figure 5.0.1. Note the direction of the caret (∧) and do not confuse source and drain.



(a) NMOS (b) PMOS

Figure 5.0.1: Wiring convention for FETs in *LogiSim*.

5.1 Preparation

Please answer the following questions *before* beginning with the simulations or experiments. Then complete the preparation quiz "Preparation 5.1 – Digital" on Ilias using your results. The points for this preparation section will only be awarded via Ilias.

5.1.1 Logic families

Review the different kind of loads (pull-ups) that can be used with an N-channel and P-channel MOSFETs to realize a simple inverter circuit.

5.1.2 Logic function

Write down a logic equation defining the logic function of the circuit shown in Figure 5.1.1 below.

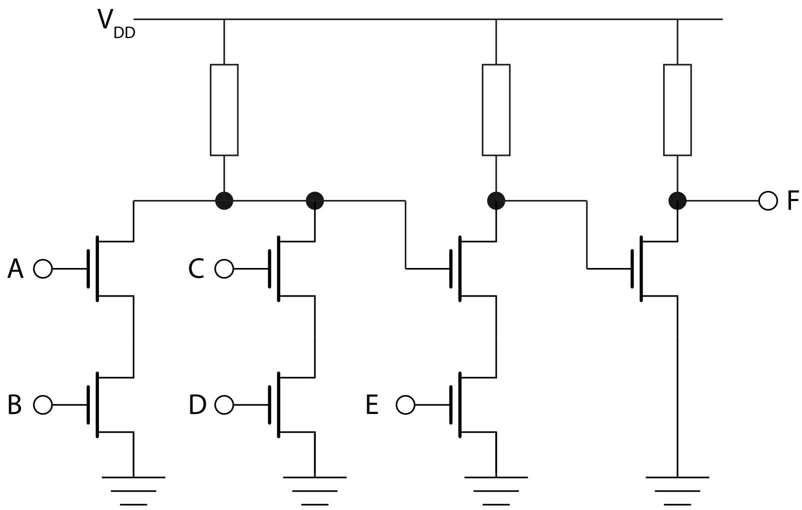


Figure 5.1.1

5.1.3 Ring oscillator

You are given a nine-stage ring oscillator, where each stage consists of an inverter with a switching delay time of 55.55 µs. Calculate the oscillation frequency.

5.1.4 Longer ring oscillator

The oscillation frequency of the ring oscillator in Section 5.1.3 is too high, so you exactly double the number of stages. What is the oscillation frequency now?

5.1.5 Gate widths

Consider a 3-input CMOS NOR gate. If the pull-up MOSFETs have $(\frac{W}{L})_{pu} = \frac{36}{2}$, what is the optimal sizing for the pull-down MOSFETs, $(\frac{W}{L})_{pd}$?

5.2 Ring oscillator

We will begin by simulating a three-inverter chain to see how basic logic simulation on transistor level works. We will then wire up and measure such an inverter chain and then make a ring oscillator from that. We will look at its oscillation speed and determine the propagation delay of each inverter.

5.2.1 Simulation

(a) Using Logisim, set up a three-inverter ring oscillator.

(b) Place a "pull resistor"[1]. Set its *Pull Direction* to *ONE* to create a pull-up resistor.

(c) Place a ground below the pull up.

(d) Place a MOSFET between the two (rotate to to face *North*). Set its *Type* to *N-TYPE*. Connect the drain to the pull resistor and the source to the ground.

(e) Place a pin and attach it to the gate of the transistor. Set *Three-state?* to *NO*. Name this pin *Input* (under *label*).

(f) Attach another pin to the drain of the transistor. Again set *Three-state?* to *NO* but set *Output?* to *YES*. Name this pin *Inv1*.

(g) Using the "finger pointer" tool, toggle the input from 1 to 0 and back, and verify that the circuit acts as an inverter.

(h) Copy everything (except the input pin) two more times and name the new output pins *Inv2* and *Inv3*.

(i) Connect *Inv1* to the gate of the second transistor and *Inv2* to the gate of the third transistor, making a three-inverter chain.

(j) Again verify that the circuit works as you expect.

(k) Using *File/Export Image*, save two versions of this circuit[2], one with input 1, the other with input 0; save these for your report.

(l) Generate the truth table of this circuit (*Project/Analyze Circuit*). Make and crop a screen shot for your report.

[1] All the components you need for this part are found under "wiring".
[2] Uncheck "Printer View" for a color image.

5.2.2 Measurement

For the measurements, we will use the three MOSFETs found in the "MOSFET" section of the electronics board, one in the *MOSFET characteristics* circuit, shown in Figure 5.2.1, and two in the *MOSFET logic gates* circuit, shown in Figure 5.2.2.

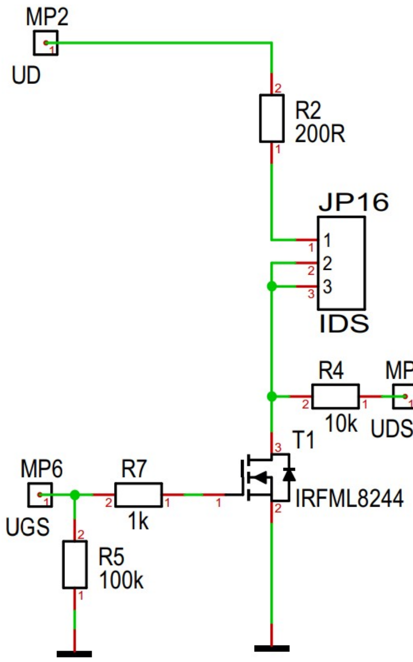


Figure 5.2.1: Schematic of the *MOSFET characteristics* circuit

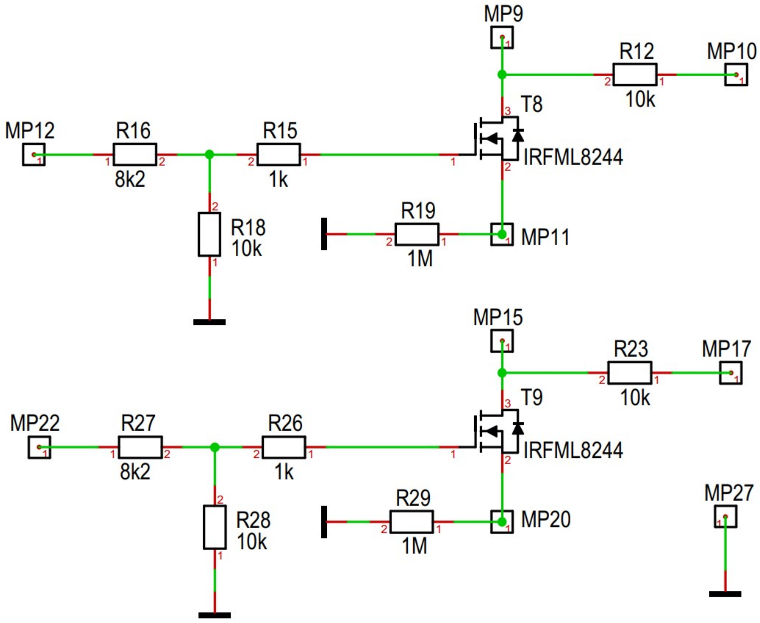


Figure 5.2.2: Schematic of the *MOSFET logic gates* circuit

In the first part of this measurement section, we will first connect three inverters (with active pull-down and passive pull-up) in series: *T1* is the first inverter; *T8* the second; and *T9* the third. We will record the logic functions of the individual signals and determine the propagation delay. In the second part, we will then realize a ring oscillator by connecting the output of inverter 3 back to the input of inverter 1.

Inverter chain

(a) Connect *MP3*, *MP10* and *MP17* to the output of the AC power amplifier (*MP35*) to supply the passive pull-up of all three inverters.

(b) Connect *MP11* and *MP20* to *GND* (*MP27*) for the active pull-down of the second and third inverters; the source of *T1* is already at *GND*.

(c) Connect the output of the first inverter (*PIN2* of jumper *JP16*) to the input of the second inverter (*MP12*).

(d) Connect the output of the second inverter (*MP9*) to the input of the third inverter (*MP22*).

(e) On the USB-XLAB there are two pin rows with the digital input and output pins *DI_0/DO_0* to *DI_15/DO_15*, where the inputs are on the left pin row (blue) and the outputs are on the right pin row (black). Connect the inputs *DI_0* to *MP69*, *DI_1* to *MP12*, *DI_2* to *MP22* and *DI_3* to *MP15*. This way, the input signal as well as the individual output signals are sampled.

(f) Create corresponding digital channels in *WaveForms/Scope*. To do this, select *Add Channel/Digital/Signal* on the right-hand side and successively name *DIO 0* Vin, *DIO 1* Inv1, *DIO 2* Inv2 and *DIO 3* Inv3.

(g) Set the time scale to 5 µs/div.

(h) Connect the control signal of *W1* (*MP69*) to the input of the first inverter at *MP6*.

(i) Apply the 5 V of *MP32* to the *Ux2* input of the AC power amplifier (*MP40*) to switch on the voltage supply of the pull-ups.

(j) Set up a PWM signal in *WaveForms/Wavegen* with 25 kHz, a duty cycle of 50 % and a voltage of 0 V to 5 V.

(k) Create the truth table for the input signal V_{in} and the three outputs Inv_1, Inv_2 and Inv_3.

(l) Measure (by double left-clicking on the digital area) the delay $t_{pd,rise}$ ($t_{pd,fall}$) from V_{in} to Inv_3 with a rising (falling) edge of V_{in}. Sum up both values and determine a frequency from this time. This is an estimate of the frequency of the ring oscillator which we will see in the next measurement task.

Ring oscillator

(m) Start with the circuit from the previous task.

(n) Remove the connection between *MP32* and *MP40* to switch off the power supply to the pull-ups while the circuit is being converted.

(o) Switch off the signal of the wavegen *W1* and then remove the connection between *W1* (*MP69*) and the input of the first inverter (*MP6*).

(p) Connect the output of the third inverter (*MP15*) to the input of the first inverter (*MP6*) to close the ring oscillator.

(q) Apply the 5 V of *MP32* to the *Ux2* input of the AC power amplifier (*MP40*) to switch on the voltage supply of the pull-ups.

(r) Measure for each inverter $i \in [1, 2, 3]$: The duration for which the signal of a cycle is low ($t_{L,i}$) or high ($t_{H,i}$) and calculate the period τ_i and frequency f_i as well as the duty cycle p_i (for signal high).

(s) Compare the frequencies f_i with each other as well as with the estimated value of the previous task.

(t) Determine which duty cycle of the three signals is closest to 50 %. Connect its signal/pin to the first input of the oscilloscope (*MP72*).

(u) Measure and plot the analogue and the digital signal course over a period of $2.2 \cdot \tau_i$ in a diagram, each with its own ordinate (y-axis). Explicitly address their shape and compare both signals.

5.3 NMOS logic

We will simulate and then construct and measure three different NMOS logic gates using three MOSFETs in varying configurations.

5.3.1 Simulation

Logic circuit 1

(a) Place three N-type MOSFETs with one input pin each (A, B and C) at their gates.

(b) Connect all sources to ground.

(c) Connect all the drains together, with a single pull-up resistor and a single output pin labeled D.

(d) Save a copy of the schematic of this circuit (*File/Export Image*) for your report.

(e) Generate the truth table of this circuit (*Project/Analyze Circuit*). Make and crop a screen shot for your report.

(f) Is this a standard logic gate and, if so, which one?

Logic circuit 2

(g) Again place three N-type MOSFETs with one input pin each (A, B and C) at their gates.

(h) Connect the source of the first transistor to the drain of the second and the source of the second to the drain of the third transistor.

(i) Connect the source of the third transistor to ground.

(j) Connect the drain of the first transistor to a single pull-up resistor and a single output pin called D.

(k) Save a copy of the schematic of this circuit (*File/Export Image*) for your report.

(l) Generate the truth table of this circuit (*Project/Analyze Circuit*). Make and crop a screen shot for your report.

(m) Is this a standard logic gate and, if so, which one?

Logic circuit 3

(n) Finally, again place three N-type MOSFETs with one input pin each (A, B and C) at their gates.

(o) Connect the source of the first transistor to the drain of the second transistor.

(p) Connect the source of the second and third transistors to ground.

(q) Connect the drain of the first and third transistors with each other, with a single pull-up resistor and a single output pin called *D*.

(r) Save a copy of the schematic of this circuit (*File/Export Image*) for your report.

(s) Generate the truth table of this circuit (*Project/Analyze Circuit*). Make and crop a screen shot for your report.

(t) Is this a standard logic gate and, if not, what is the logic formula of this circuit?

5.3.2 Measurement

We will again use the three MOSFETs found in the "MOSFET" section of the electronics board, one in the *MOSFET characteristics* circuit, shown in Figure 5.2.1, and two in the *MOSFET logic gates* circuit, shown in Figure 5.2.2.

Logic circuit 1

(a) Connect *MP17* to the output of the AC amplifier (*MP35*) for the supply of the passive pull-up. Then connect *MP11* and *MP20* to *GND* (e.g. *MP27*) for the active pull-down of both MOSFETs.

(b) Connect the digital outputs of the USB-XLAB to the inputs of the MOSFETs: *DO_0* with *MP6*, *DO_1* with *MP12* and *DO_2* with *MP22*. Then connect the digital input of the USB-XLAB to the output of the MOSFET *T9*: *DI_8* with *MP15*.

(c) Short-circuit *MP9*, *MP15* and *PIN2* of jumper *JP16* with each other.

(d) Apply the 5 V of *MP32* to the *Ux2* input of the AC amplifier (*MP40*) to switch on the voltage supply of the pull-ups.

(e) In *WaveForms*, open the menu *Static IO*, in which the digital input and output pins can be statically controlled or read.

   - Click *DIO 15-8* on the left and then select *Bit IO/LED* to set pins 8 to 15 as inputs to represent their values as LEDs.

   - Click *DIO 7-0* on the left and then select *Bit IO/Switch/Push/Pull (1/0)* to set pins 0 to 7 as output to adjust their values using sliders.

(f) Select *Control/Run* to start the application.

(g) Determine the truth table of this circuit by setting *DIO 0*, *DIO 1* and *DIO 2* and reading *DIO 8*.

Logic circuit 2

(h) Connect *MP17* to the output of the AC amplifier (*MP35*) for the supply of the passive pull-up. Then connect the digital outputs of the USB-XLAB to the inputs of the MOSFETs: *DO_0* with *MP6*, *DO_1* with *MP12* and *DO_2* with *MP22*.

(i) Connect the digital input of the USB-XLAB to the output of the MOSFET *T9*: *DI_8* with *MP15*.

(j) Short circuit *MP20* and *MP9* with each other and short circuit *MP11* and *PIN2* of Jumper *JP16* with each other.

(k) Apply the 5 V of *MP32* to the *Ux2* input of the AC amplifier (*MP40*) to switch on the voltage supply of the pull-ups.

(l) In *WaveForms*, open the menu *Static IO*, in which the digital input and output pins can be statically controlled or read.

- Click *DIO 15-8* on the left and then select *Bit IO/LED* to set pins 8 to 15 as inputs to represent their values as LEDs.
- Click *DIO 7-0* on the left and then select *Bit IO/Switch/Push/Pull (1/0)* to set pins 0 to 7 as output to adjust their values using sliders.

(m) Select *Control/Run* to start the application.

(n) Determine the truth table of this circuit by setting *DIO 0*, *DIO 1* and *DIO 2* and reading *DIO 8*.

Logic circuit 3

(o) Connect *MP17* to the output of the AC amplifier (*MP35*) for the supply of the passive pull-up. Then connect *MP11* to *GND* (e.g. *MP27*) for the active pull-down.

(p) Connect the digital outputs of the USB-XLAB to the inputs of the MOSFETs: *DO_0* with *MP6*, *DO_1* with *MP12* and *DO_2* with *MP22*. Then connect the digital input of the USB-XLAB to the output of the MOSFET *T9*: *DI_8* with *MP15*.

(q) Short circuit *MP20* and *MP9* with each other and short circuit *MP15* and *PIN2* of Jumper *JP16* with each other.

(r) Apply the 5 V of *MP32* to the *Ux2* input of the AC amplifier (*MP40*) to switch on the voltage supply of the pull-ups.

(s) In *WaveForms*, open the menu *Static IO*, in which the digital input and output pins can be statically controlled or read.

- Click *DIO 15-8* on the left and then select *Bit IO/LED* to set pins 8 to 15 as inputs to represent their values as LEDs.

- Click *DIO 7-0* on the left and then select *Bit IO/Switch/Push/Pull (1/0)* to set pins 0 to 7 as output to adjust their values using sliders.

(t) Select *Control/Run* to start the application.

(u) Determine the truth table of this circuit by setting *DIO 0*, *DIO 1* and *DIO 2* and reading *DIO 8*.