ECE 340 Project 2: Homemade Transistor Curve Tracer

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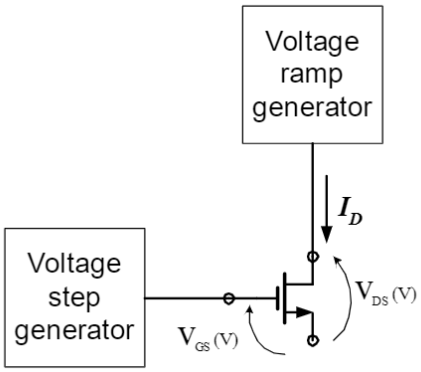
Problem statement and specifications

Problem Statement

Design and build a transistor curve tracer without using microprocessor or micro controllers. The curve tracer should graph i_D vs V_{DS} (drain current vs drain-source voltage), and be made up of a voltage ramp generator and voltage stair step generator in the following configuration:



Specifications

1. Display i_D vs V_{DS} (drain current vs drain-to-source voltage) characteristics of the MOSFET (2N7000) on an oscilloscope
2. On use power supply voltages +5V and +/- 15V
3. The HMCT should generate eight 0.5V VGs steps: 0 to 3.5V, accurate to 5%
4. Drain current display range: 0-80mA (10mA/division vertical)
5. Drain-to-source voltage range: 0-1W (1V/division horizontal)
6. Use 5% resistors and only components from component list
7. Minimize part count and display flicker.

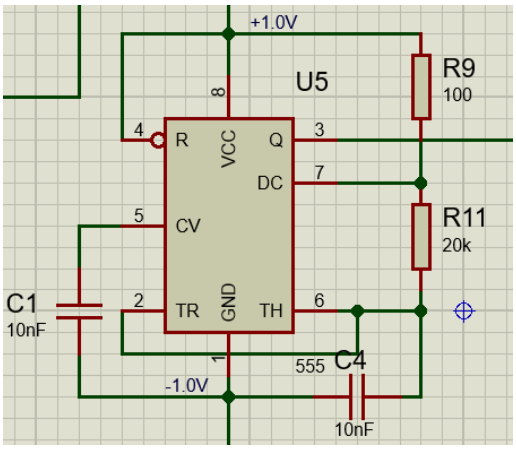
Circuit Design Options

Clock

In order to generate a stairstep and ramp signal with the same frequency and phase, a shared clock is required. We went through a few designs, ultimately settling for a 555-timer configured to output a pulse signal.

555 Timer

The following is a 555-timer configured to output a pulse signal:

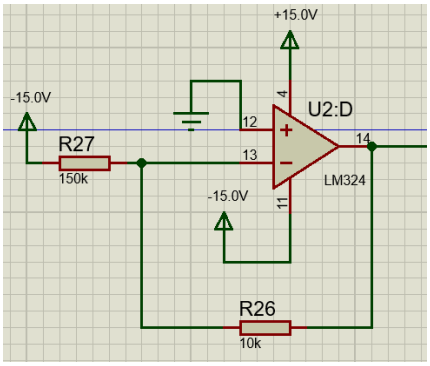


This circuit outputs a series of voltage pulses out of pin 3. The voltage range of these pules is determined by VCC and GND, which in this diagram are +1.0V and -1.0V respectively.

The frequency of the pulse signal is given by the capacitor C4 and resistors R9 and R11. From the data sheet for the LM555, we can see that in an astable operation like this the frequency is given by:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

Its important to note that in order to supply this 555-timer with +/-1.0V, an op-amp would have be used to decrease voltage from the +/-15.0V power rails. Here is an example of such an op-amp:

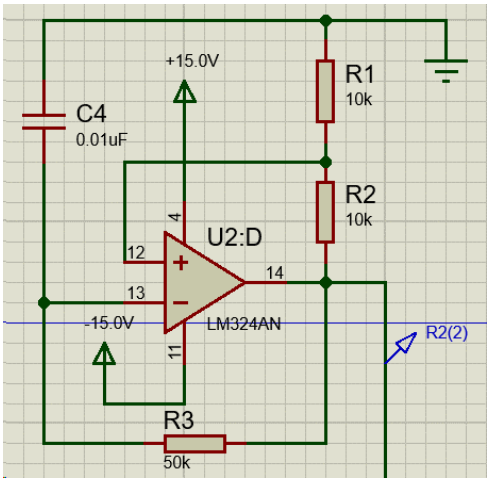


It uses an inverting op-amp configuration provide a +1.0V output from an -15.0V input. The gain is:

$$AV = -\frac{Rf}{Rin} = -\frac{R26}{R27} = -\frac{1}{15}$$

OP-AMP Astable Multivibrator

The following is an op-amp configuration we tested to use as a pulse clock:



Here, as with the 555 above, the triggering signal is provided by the charge/discharge cycles of the capacitor.

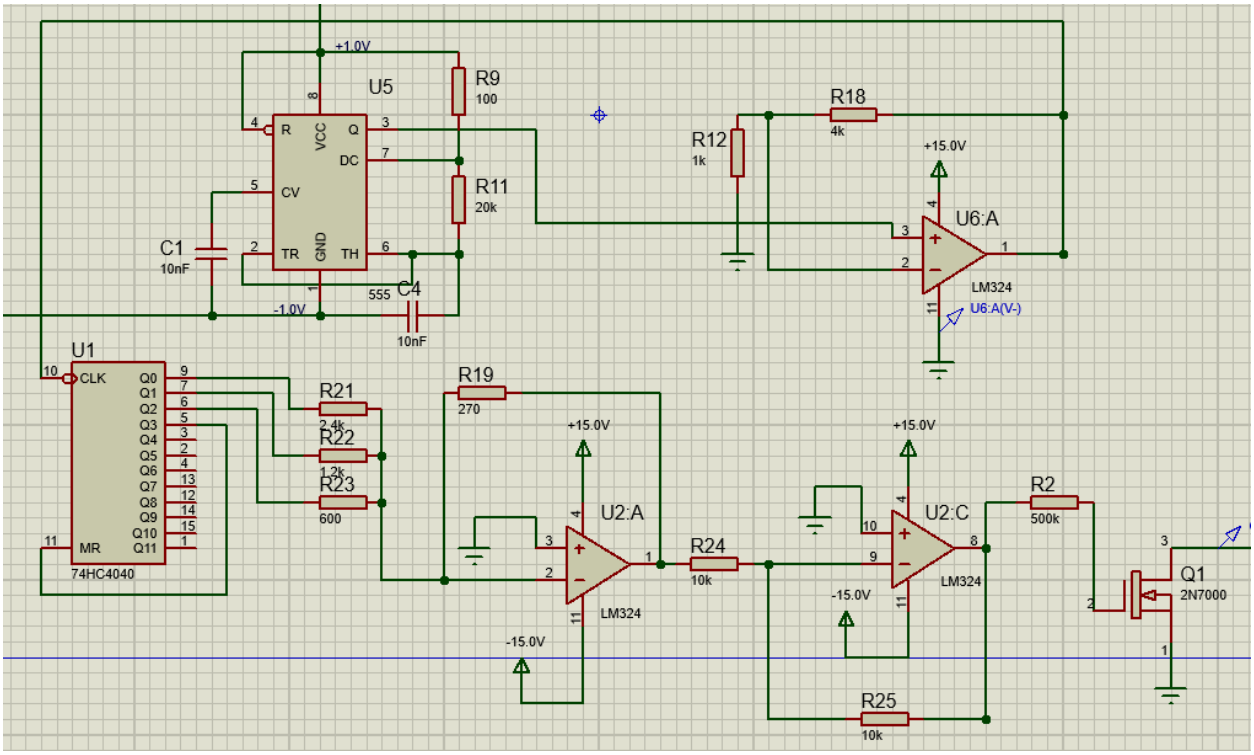
The period of the pulse signal output from pin 14 is:

$$T = 2C(R3) * \ln\left(1 + \frac{R1}{R2}\right)$$

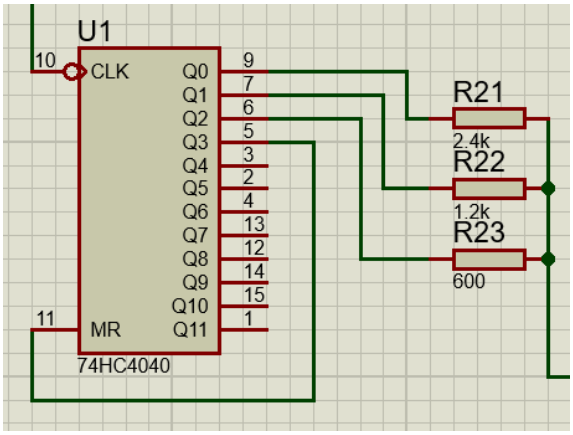
The voltage range of the signal is about +/- Vsat, however this is not exact, and the voltage limits have a magnitude of about 1V less than this. For this reason we decided to go with the 555 configuration as it had a simpler equation for frequency, and had more accurate voltage ranges.

Stairstep Generator

The following circuit was our chosen option for the stairstep wave:



It operates from the primary square pulse train that gets outputted from pin 3 of the 555-timer. The voltage range of this signal is +/-1.0V, which we then convert to a +5.0V/0V range using a simple non-inverting amplifier configuration. We do this because the 12-stage binary counter (74HC4066) requires a clock with this range to operate.



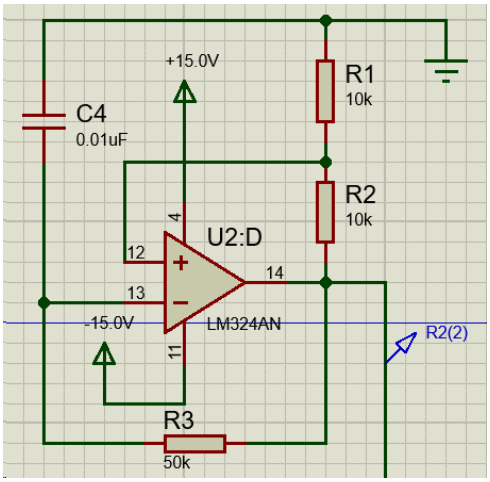
Now fed with a clock, The 12-stage binary counter begins to output pulse waves of different frequencies. Starting with pin 9 (the pin highest up on the counter), it outputs a signal with period 1T. The pin below (pin 7) outputs a signal with period 2T, and the period of the signals continue to double as you down the pins. All signals start low (0V).

Pin 5 is fed to the reset pin of the counter (MR) so that once 8T has passed, the counter will reset itself and output from the beginning again.

The three outputs signals can then be modulated with an op-amp in an inverting summer configuration, resulting in one signal with a period of 8T with a range that can be adjusted with the inverting summer op-amp as well (from +5.0V/0V to +3.5V/0V). It was necessary to use the inverting configuration as the non-inverting configuration does let us have a gain with a magnitude less than one. This is our inverted stairstep function. Finally, the stairstep must invert one last time to give us a voltage range of +3.5V/0V instead of 0V/-3.5V.

Modification: OP-AMP Astable Multivibrator

Instead of using a binary counter to generate pulses wave signals, we could use three op-amp multivibrators whose signals each get fed into the inverting op-amp summer.



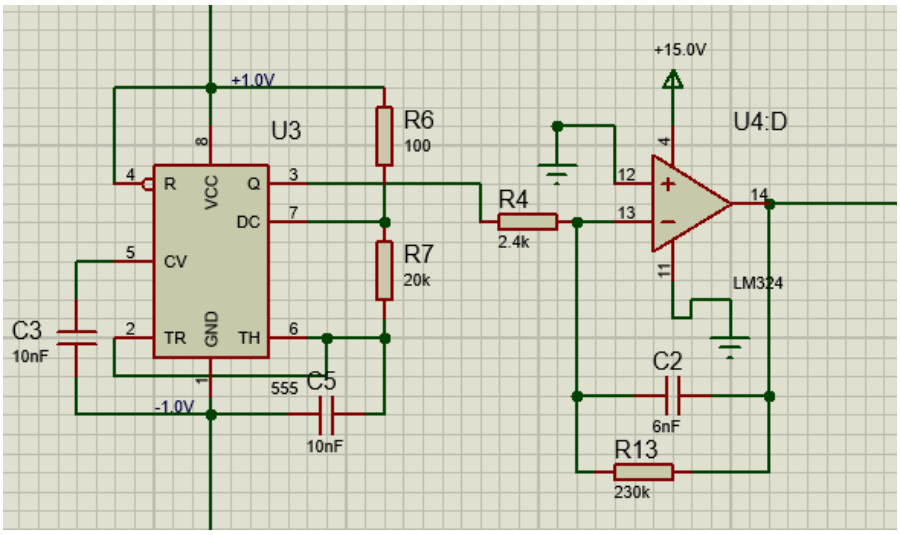
As previously seen with the clock, the period of the output signal can controlled by the following equation:

$$T = 2C(R3) * \ln\left(1 + \frac{R1}{R2}\right)$$

While using three op-amp multivibrators would work, it would increase our part count significantly and would be harder to debug. We made use of our 12-stage binary counter allotted to us and chose the configuration with it instead.

Ramp Generator

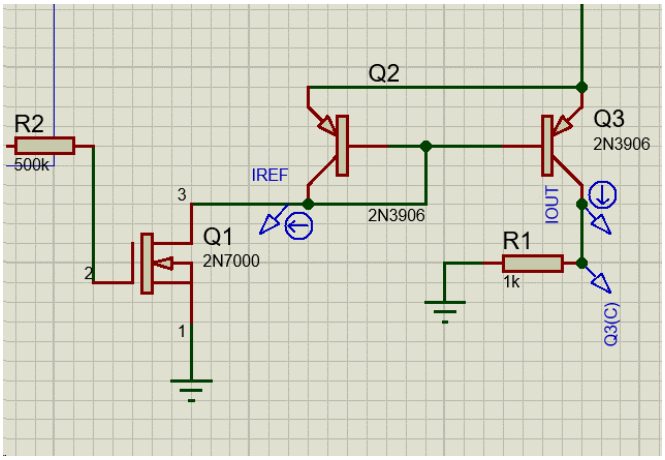
The following is the circuit for our ramp generator:



As with the stairstep, we start with a +1.0V/-1.0V clock output (both the stairstep and ramp generator use the same clock). This square wave centered at 0V is then passed into an op-amp Integrator circuit. This circuit integrates the square wave into a triangle wave of the same frequency with a phase shift of 180° (which is fine for our purposes). The voltage range of this triangle wave can be adjusted using the resistors R4 and R13. Note the ground at the negative power terminal of the op-amp, which limits the output triangle wave to a minimum voltage of 0V.

Current Mirror

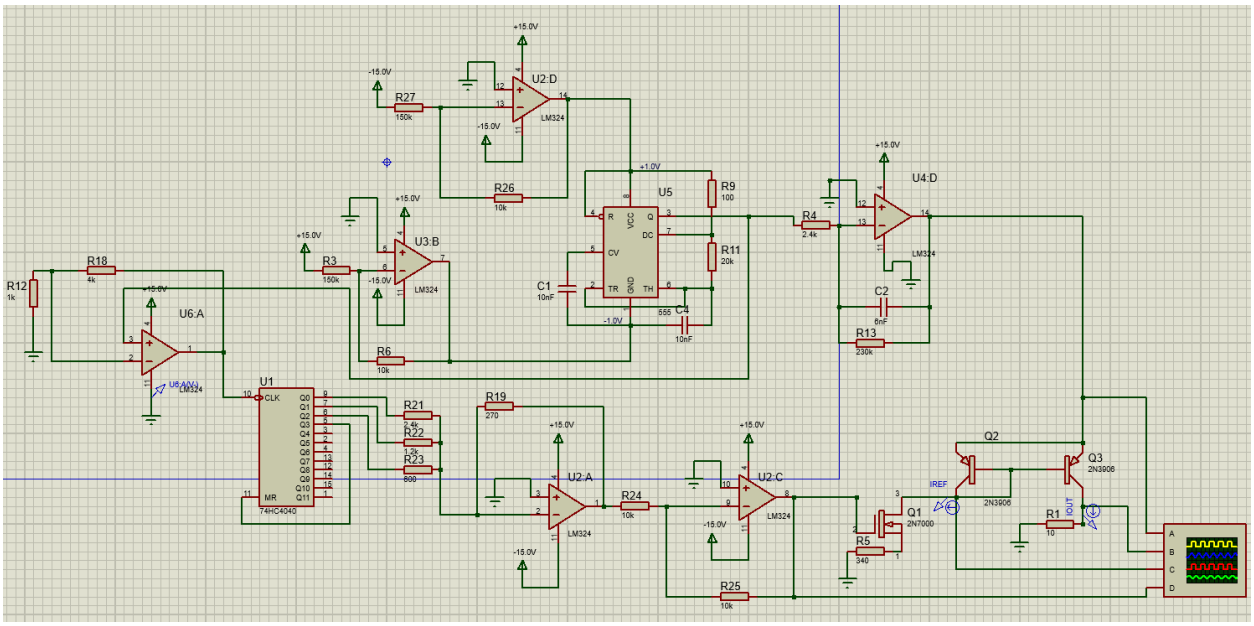
We decided to use a simple PNP BJT current mirror.



We chose this method of converting drain current to voltage as it is very accurate and non-intrusive to the circuits its attached too. It should not have an effect on MOSFET or ramp function its attached to (partly due to lack of resistance).

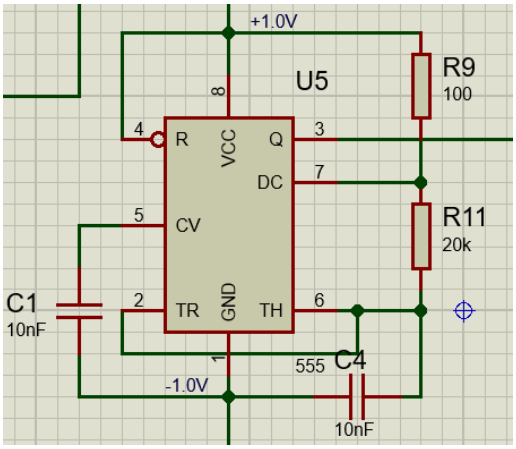
Here the reverse bias of the transistors (base-collector junction), allowing us to get closer to a linear approximation of drain current as a voltage. Importantly, this also does not add a resistance to the source of the MOSFET.

Final Complete Circuit



Analytical and Computer Simulation

Clock



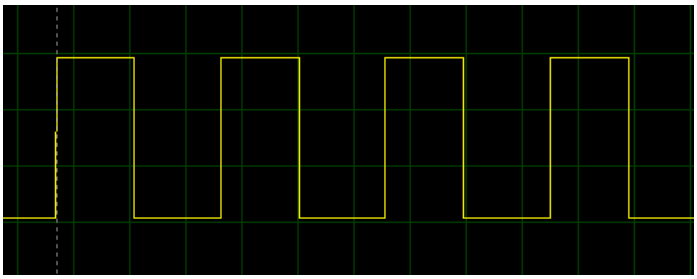
As stated before, the output signal frequency of the 555-timer in astable operation can be described by the following equation:

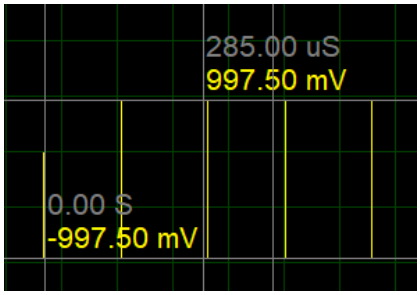
$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

Here R_A = 100 Ω, R_B = 20k Ω, C = 10nF

$$f = \frac{1.44}{(100+40{,}000)10*10^{-9}} = 3591 \text{ Hz}$$

If f = 3951 Hz, T = 1/f = 278uS. Simulating this wave form, we see:





Our measured period is 285uS, which is only has an error of 2.5%. Additionally, as expected the voltage range of this waveform is +1.0V/-1.0V, which has identical vales the voltages applied to VCC and GND pins of the 555-timer.

Note that the rise and fall time of the pulse train can be found on the spec sheet.

The charge time (output high) is given by:

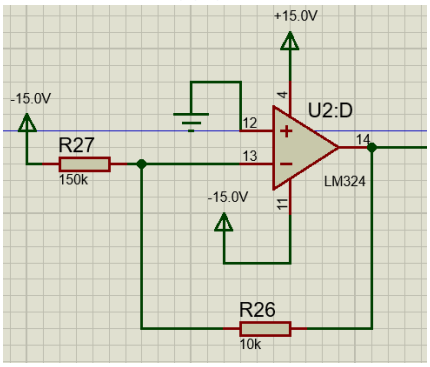
$t_1 = 0.693 (R_A + R_B) C$

And the discharge time (output low) by:

$t_2 = 0.693 (R_B) C$

This is the why we set R9 (RA) to a low resistance of 100 Ω, as we wanted the waveform to have a very similar rise and fall time. With our resistor values, the rise time is only 0.5% larger than the fall time which is an acceptable error.

Clock Power Supply

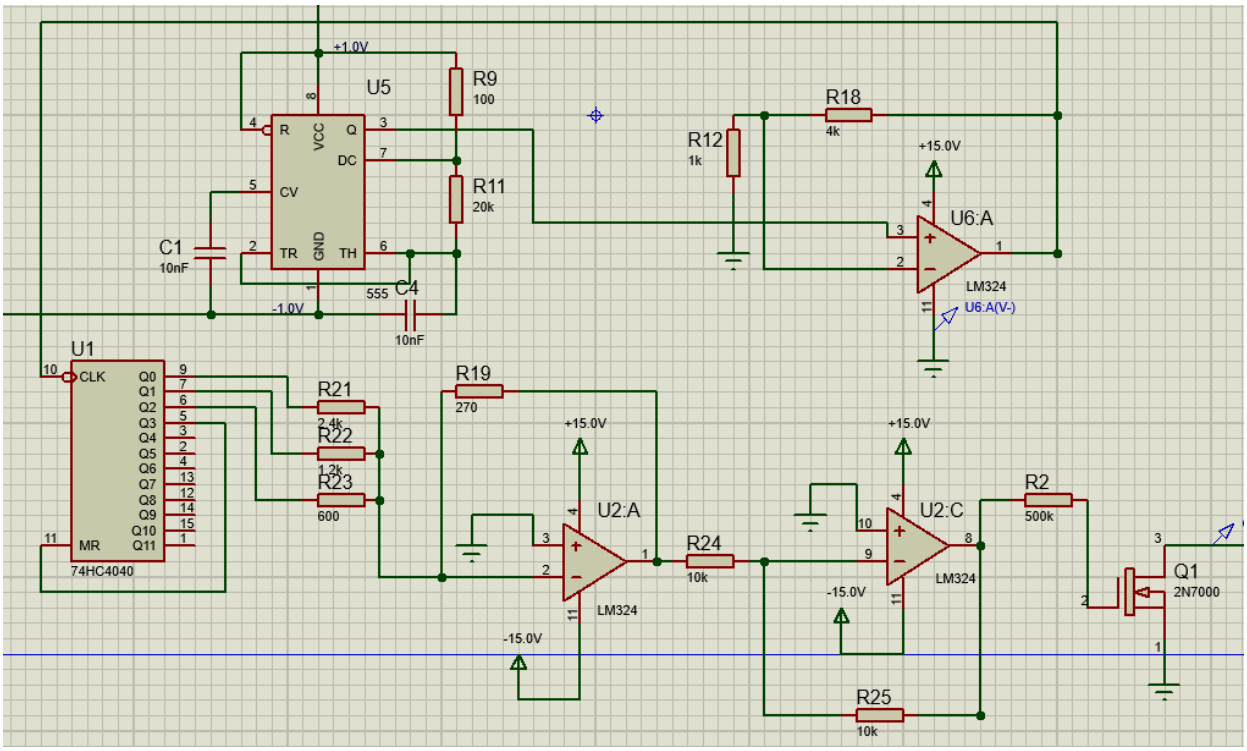


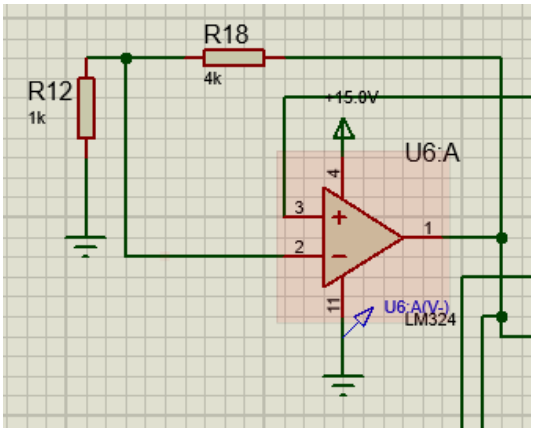
This inverting op-amp configuration converts -15.0V to +1.0V. The gain is:

$$AV = -\frac{\text{Rf}}{\text{Rin}} = -\frac{\text{R26}}{\text{R27}} = -\frac{10\text{k}}{150\text{k}} - \frac{1}{15}$$

For the -1.0V power to the GND pin, a +15.0V signal is used instead to achieve the voltage 15*(-1/15) = -1.0V.

Stairstep Generator



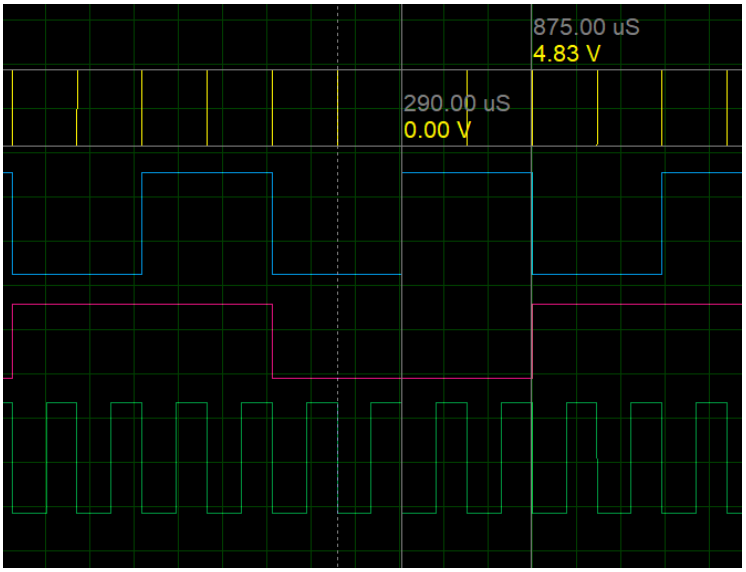


To generate a stairstep function first the clock is fed into a non-inverting op-amp. The gain equation for this op-amp is:

$$AV = 1 + \frac{\text{R18}}{\text{R12}} = 1 + \frac{4\text{k}}{1\text{k}} = 5$$

We also ground our negative power terminal for the op-amp, so the voltage output can never be less than 0V. This way our output range is +5.0V/0V, which is needed as the clock for our binary counter.

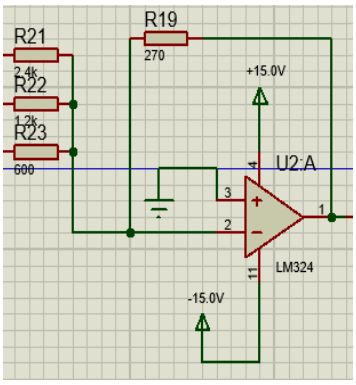
Using the oscilloscope, the following shows the outputs of the binary counter and its clock:



The output of pin9 is yellow, pin7 is blue, and pin6 is red. The clock is shown in green. We can see that the pin9 period is twice the period of the clock, or 585uS. The pin7 output is twice that value at 1170uS, and the output for pin6 has a period of 2340uS.

Each of the signals have a voltage range of +5.0V/0V

To generate a stairstep function with these pulse waves, they must be summed together with a summing amplifier. To generate a stair step with this, we want the blue signal to have half the amplitude of the red signal, and the yellow signal to have half the amplitude of the blue signal. This allows for 8 different voltage levels for one period of the red signal. After the red signal cycles for one period, the counter is reset as pin5 goes high and enables the reset pin MR. This drops all outputs to 0V and starts each signal at the voltage low part of their cycle, allowing us to start the stairstep over again.

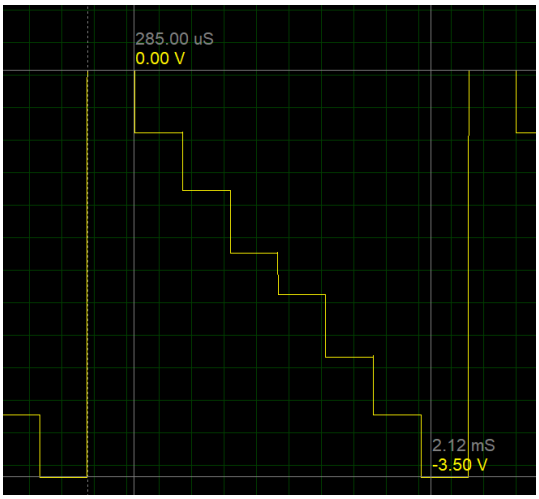


To make sure the voltage ranges of each individual waveforms are as described above, the resistors at the output of each waveform were set accordingly.

The output of our summing amp can be described as:

$$Vo = -(\frac{\mathrm{Rf}}{\mathrm{R21}}\mathrm{V1} + \frac{\mathrm{Rf}}{\mathrm{R22}}\mathrm{V2} + \frac{\mathrm{Rf}}{\mathrm{R23}}\mathrm{V3})$$

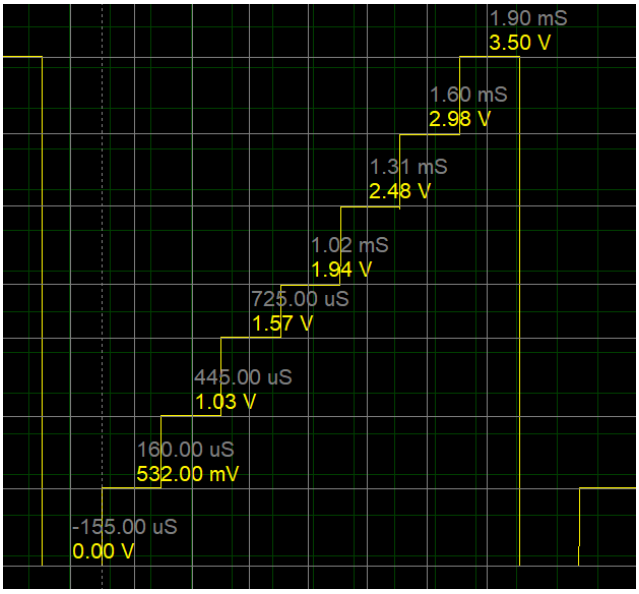
Where Rf = 270 Ω and V1, V2, V3 = output of pin9, pin7, pin6 respectively



Using this summing amplifier with Rf = 270 Ω, R21 = 2.4k Ω, R22 = 1.2k Ω and R23 = 600 Ω, we are able to get an inverted stair step with a voltage range of 0V/-3.5V.

Now all we have to do is invert it. To do that we use a simple inverting op-amp with a unity gain, which can be easily done by setting input resistance equal to feedback resistance.

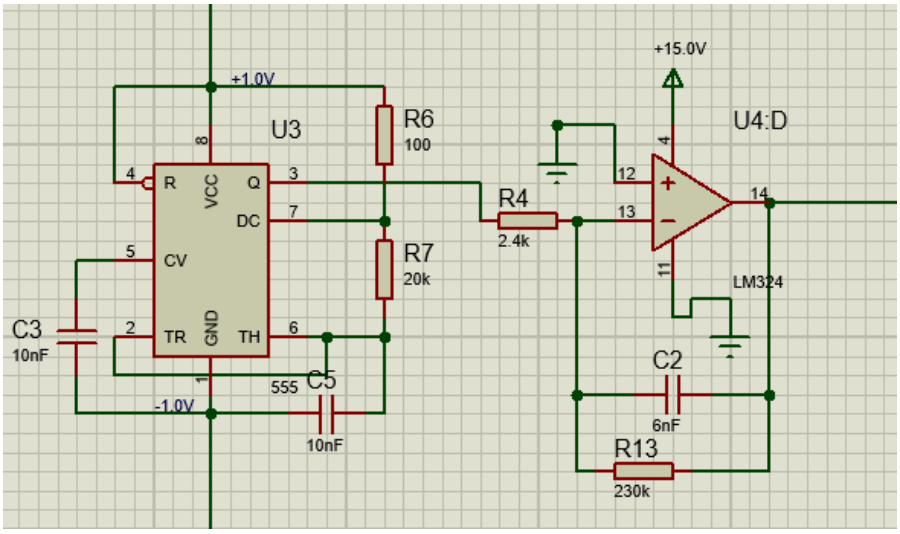
The following image shows our final stairstep waveform:



The specifications were to generate a stairstep function with eight +0.5V steps, accurate to 5%.

Our least accurate step is 532mW, with an error of 6.4%. All of our other steps fall within 5% error. With only one step not meeting the criteria, and just barely, we find this to be an acceptable stairstep function.

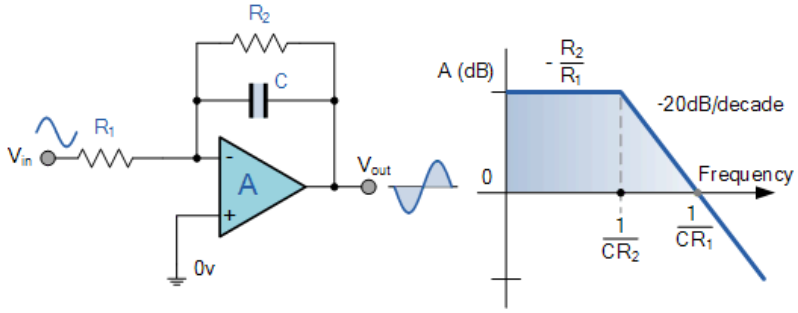
Ramp Generator



Compared to the stairstep, the ramp generator uses few components. Not including the clock, there is only one circuit that processes the signal, an op-amp Integrator with DC gain control.

This op-amp configuration outputs the integral of the input function, with a negative gain of magnitude we will calculate below.

$$Vo = -Av\int_0^1 Vin\, dt$$



The gain of the op-amp is dependant on its capacitor, the frequency at which it operates, and both of its resistors. To find it, we must first calculate:

$$\frac{1}{C * R13} = \frac{1}{230{,}000 * 6 * 10^{-9}} = 725\ Hz \qquad \frac{1}{C * R4} = \frac{1}{2400 * 6 * 10^{-9}} = 69444\ Hz$$

The frequency of the clock is 3591 Hz as calculated earlier. We can use this to find the input frequencies relative location on the graph above.

$$\log_{10}\frac{3591}{724} = 0.695 \qquad \log_{10}\frac{69444}{724} = 1.981$$

We observe that the gain decreases by about 1.981 decades (-39.62 dB or -95.72 Av) from the drop off point. This makes sense as -R13/R4 = 95.83. Since the gain decreases 20dB/decade, at 3591 Hz the gain is:

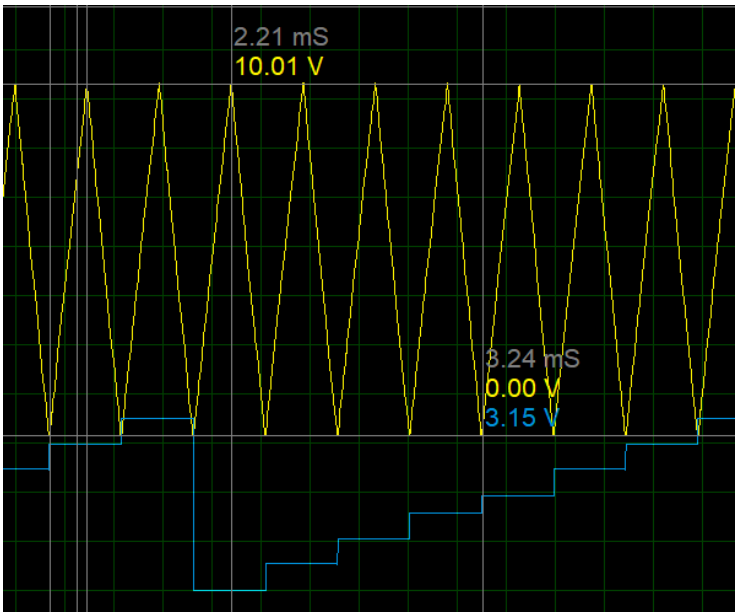
$$10^{(1.981-0.695)} = 19.32\ dB$$

Finally, you can convert this to ordinary gain:

$$10^{\frac{19.32}{20}} = 9.246 \approx 10$$

This is what we are looking for, as for an input square wave with voltage range +1.0V/-1.0V the resulting triangle wave will have the range +10V/-10V.

To create a ramp function with a range of +10V/0V, we simply ground the negative power pin of the op-amp so instead of integrating a square wave from +1.0V/-1.0V, it integrates a square wave with a voltage range +1.0V/0V, giving us our desired ramp function.

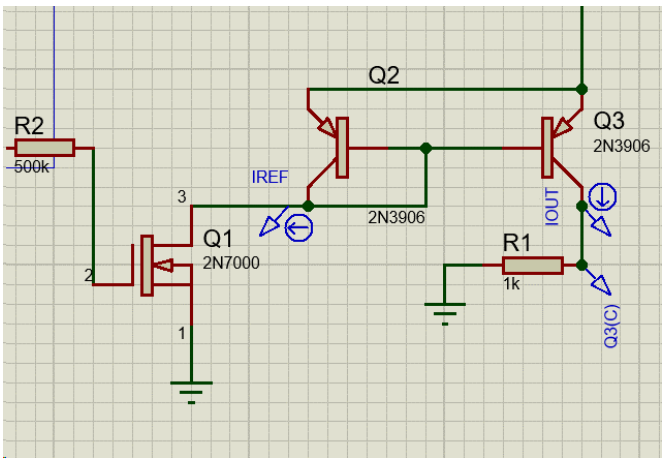


Here we see the ramp function with the stair step over laid on top. We can see that the rise and fall of the ramp is timed accordingly with the stairstep. Just like the clock, the ramp function has a rise time only 0.5% larger than the fall time.

The voltage range of the ramp is very close to the +10V/0V we need, and together these two waves will give us our transistor curves.

Current Mirror

Here we have a simple PNP BJT current mirror.



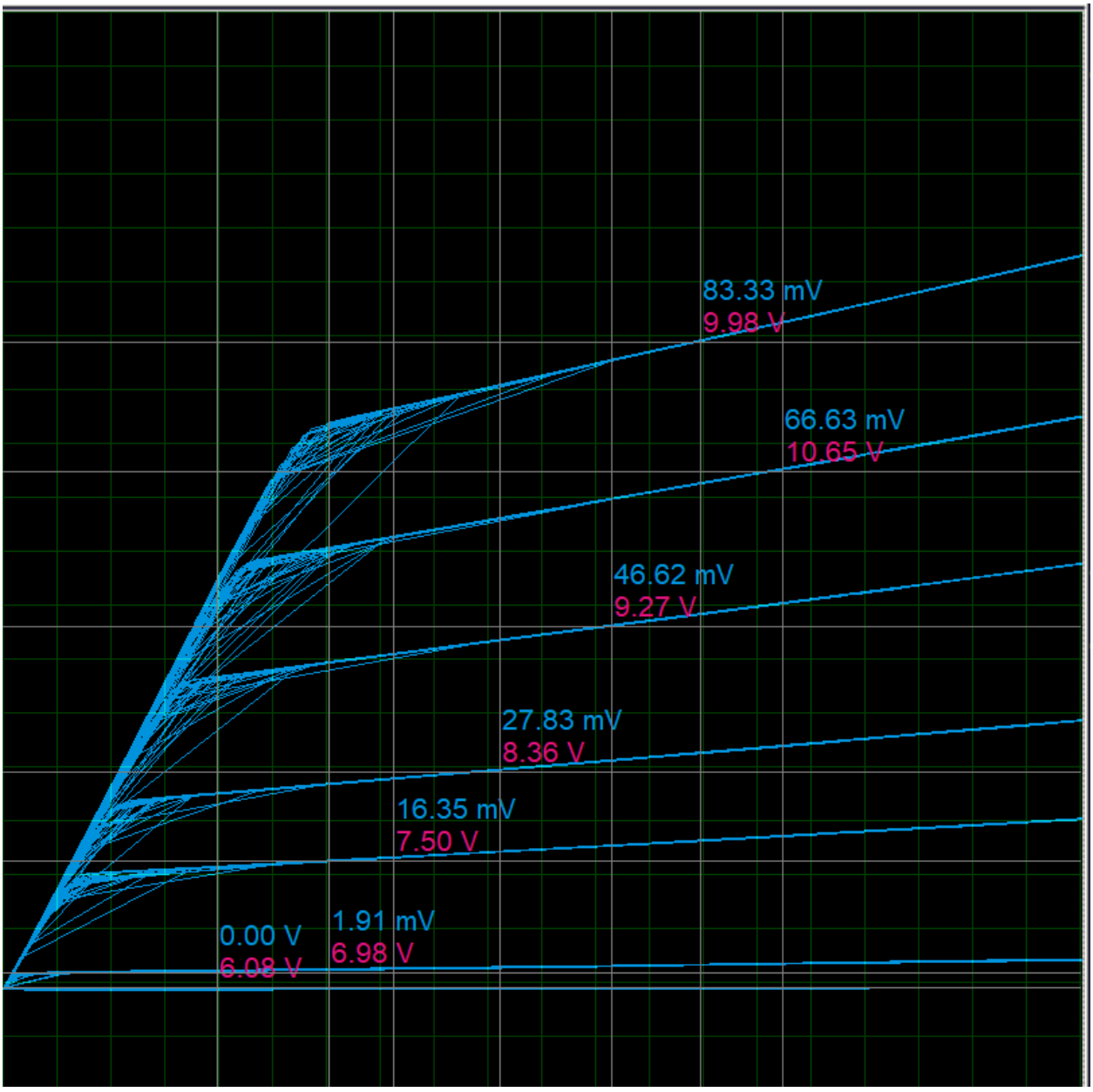
We can write: $Iout = \frac{\text{Iref}}{1+2/\beta}$

We can use the voltage over the resistor R1 from the mirrored current I_{OUT} to plot a logarithmic equivalent to the drain current of the MOSFET.

Here the reverse bias of the transistors (base-collector junction), allowing us to get closer to a linear approximation of drain current as a voltage. Importantly, this also does not add a resistance to the source of the MOSFET.

Transistor Curve Simulation

The following is the transistor curve we obtained from the 2N7000 MOSFET:

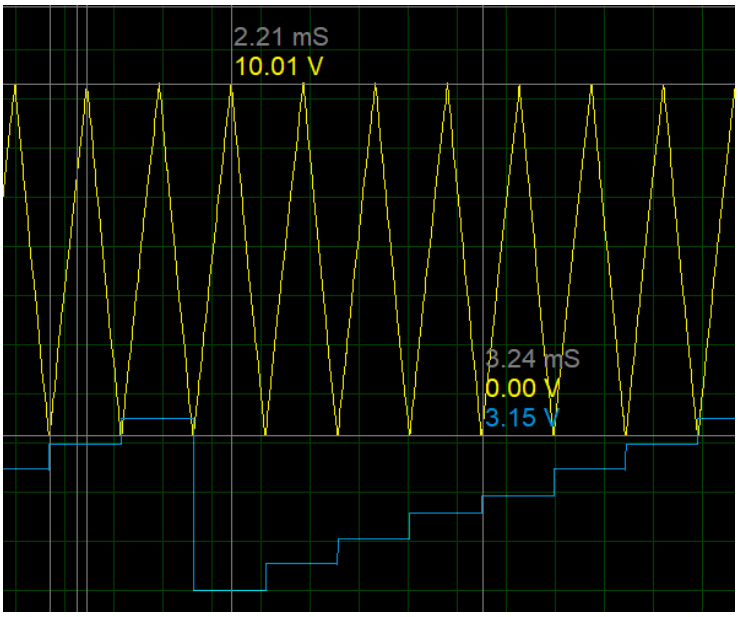


Here we can see the curves for the voltage steps from the stairstep wave. While most steps are showing, not all of them are, which could be due to them bunching up together.

The range of drain currents present is on the 0mV-80mV range as required, and the drain to source voltage range falls between 0V to 10V when triggered independently (values over 10V don't actually exist).

Test Methodology Employed

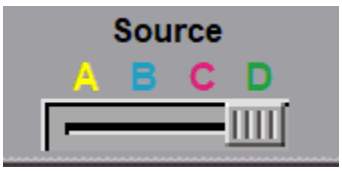
The above section, analytical and computer simulation, showed a variety of tests we did to achieve our simulations. We will simply continue to examine our testing process in this section.

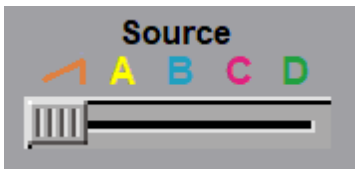


It was very important to make sure the ramp function was in sync with the stairstep as shown in the diagram. Our 555-timer clock made this very easy to accomplish, as both functions were made from the same square pulse train.

To test whether they were in sync and had the desired period, we simply hooked both functions to the built in oscilloscope and set the stair step function as the trigger. We also made sure the horizontal source was set to the sawtooth function.

Trigger and horizontal source respectively:

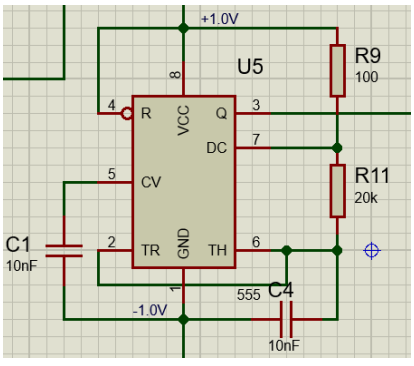




Effect of Frequency on Curve Trace

One variable that impacted how our final curve tracer looked was the frequency of the stairstep and ramp functions.

As shows earlier, the frequency of these functions is controlled by the 555-timer clock, which can be calculate as:



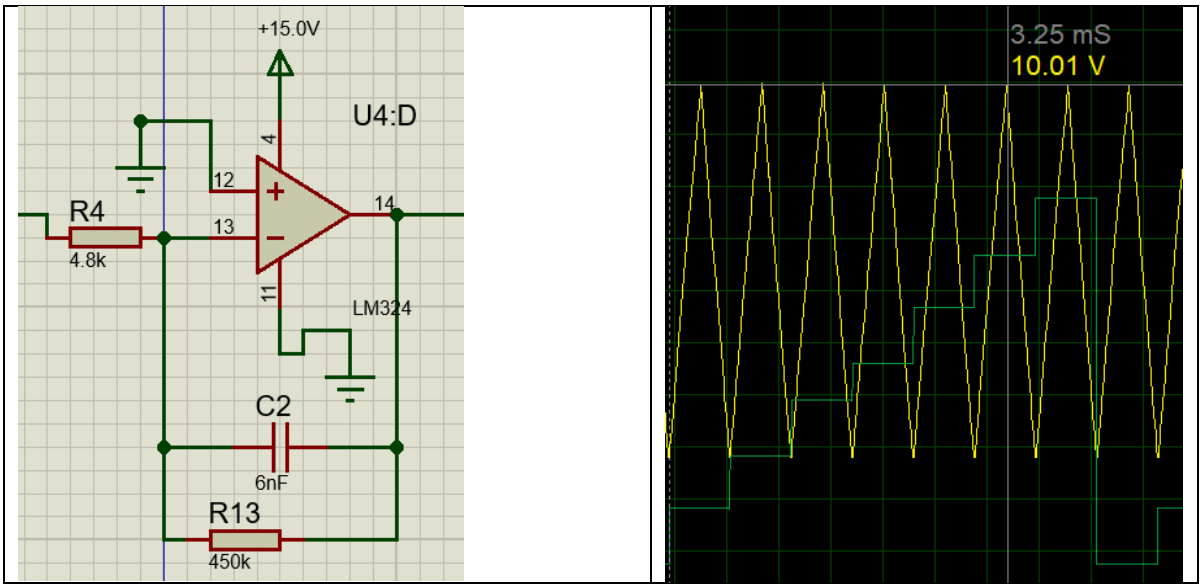
$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

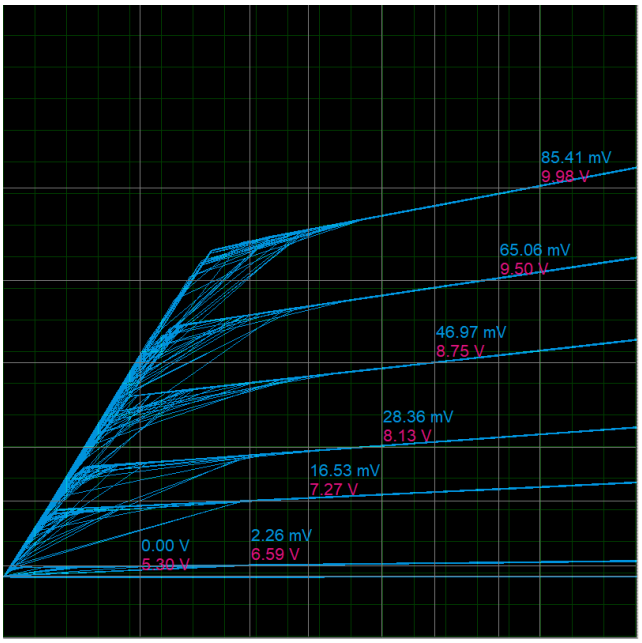
Here R_A = 100 Ω, R_B = 20k Ω, C = 10nF

$$f = \frac{1.44}{(100+40{,}000)10*10^{-9}} = 3591 \text{ Hz}$$

We will change our clock capacitor to 20nF from 10nF, resulting in a frequency of 1795 Hz.

The following shows adjustments made to our integrator op-amp as its frequency dependant:





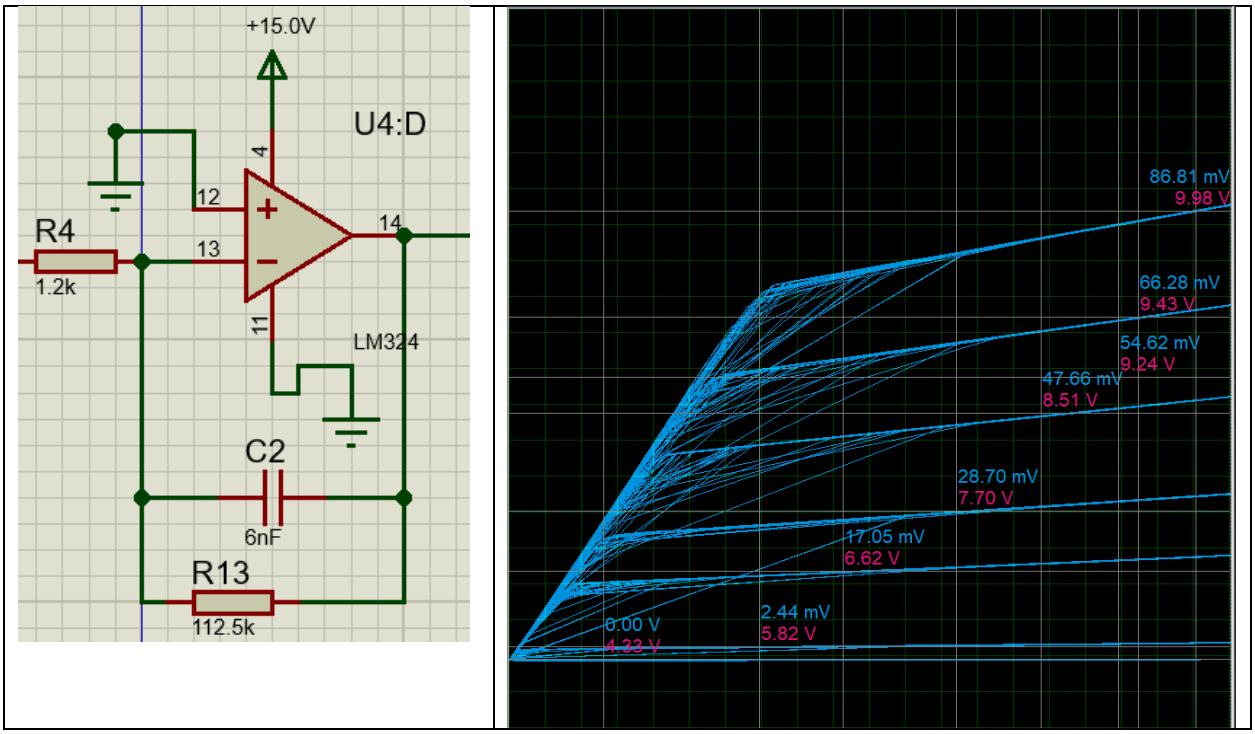
Here is the resulting curve trace.

At lower frequencies the curve trace looks similar, not significantly more or less distorted.

1795 Hz was our initial frequency, so we initially had this result. Only after increasing the frequency we were able to get the curve shown initially.

Improving Curve Trace

In an attempt to get a better curve trace than the one we did calculations on, we tried to increase the frequency of the clock. To do this we changed the clock capacitance from 10nF to 5nF, and halved our integrator op-amp resistors. The following is the resulting circuit and curve trace:



It looks slightly worse, and the curves are starting to interfere with each other more. We have learned that for these kind of simulations, higher frequencies may be worse, and you should always try to see the different frequency responses of your circuit.

Conclusion

To create a transistor curve tracer with a stairstep and ramp function there are a few things we learned to keep in mind:

- The stairstep and ramp bust be synchronized, a clock is a very good way of doing this.
- Grounding power pins of op-amps is an easy way of limiting the voltage range of a signal passing through it.
- Integrated circuits such as a binary counter are a very effective way of cutting down on components, are more accurate, and are simpler to implement than less complicated parts such as op-amps.
- There should not be any current flowing into or out of IC pins unless explicitly needed. While a voltage divider might seem like a good idea to control the voltage going into a pin, the current it creates flows into the IC pin and messes up its functionality. Its safer and functionally better to use an op-amp to control IC pin voltages.
- The frequency the circuit operates at can impact how it performs, especially when dealing with non-linear devices such as transistors.