1) Using only NAND gates, draw this equation's circuit:  $a + (\bar{b}*c)$  (1 point)

- 2) Now draw it using only NOR gates. (1 point)
- 3) What does it mean for a gate to be "functionally complete"? (1 point)

4) COmplete the timing diagram (assume 1 delays) for the circuit shown below.
(2 points)



