Hw 8

1. Truth Table

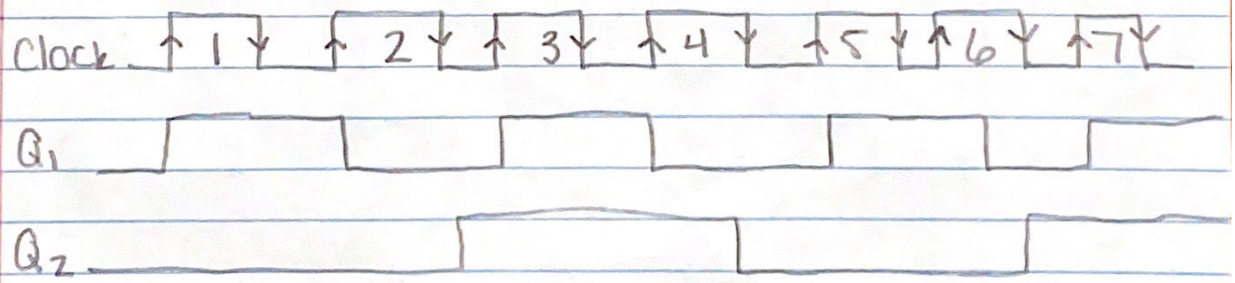
J	K	Q(n+1)
0	0	Q(n)
0	1	0
1	0	1 → set
1	1	Q(n)↓ toggle state

flip-flop (D-f/f) is positive-edge triggered;

JK flip-flop is negative-edge triggered

$Q_1 = Q_2 = 0$

Clock	Q_1	Q_2
0	0	0
1	1	0
2	0	1
3	1	1
4	0	0
5	1	0
6	0	1
7	1	1



2. i.)

Current State	Input		Output	f/f input		Next States
T	X	Y	Z	Q	$\bar{Q}$	$\hat{T}$
0	0	0	0	0		1
0	0	1	1	1		1
0	1	0	1	0		1
0	1	1	0	1		1
1	0	0	0	0		0
1	0	1	1	1		0
1	1	0	1	0		0
1	1	1	0	1		0

→ XOR gate

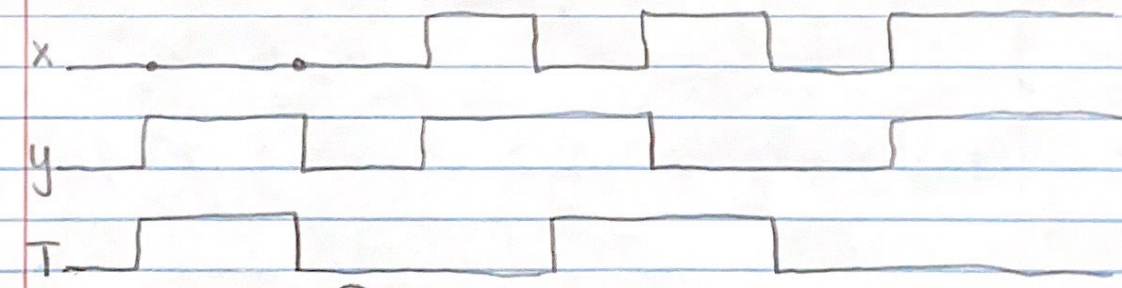
0	0	0
0	1	1
1	0	1
1	1	0

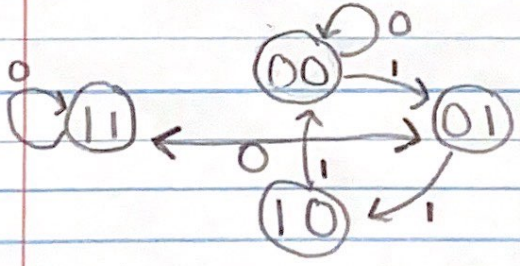
x \ Q	0	1
0		1
1	1	1

$\bar{x}Q + x\bar{Q} + xQ = T$

$\bar{x}Q + x = Q(x + \bar{x}) = Q$

$= T = Q$





3. $J_1 = x + y_2$ $\quad J_2 = \overline{x} \cdot \overline{y_1}$ (Flip-flop Input Eq.)

$K_1 = \overline{x}$ $\quad K_2 = x$

$Z = y_1 + \overline{y_2}$

State Table

Current State y_1	y_2	Input x	Output Z	f/f J_1	K_1	Inputs J_2	K_2	Y_1	Y_2
0	0	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	0
0	1	0	0	1	1	1	0	1	1
0	1	1	0	1	0	0	1	1	0
1	0	0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	1	1	0
1	1	0	1	1	1	0	0	0	1
1	1	1	1	1	0	0	1	1	0

J	K	Q
0	0	Q_0
0	1	0
1	0	1
1	1	$\overline{Q_0}$

State diagram