JUSTIN ALLEN

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Results-driven Engineer with 4.5 years of experience in semiconductor manufacturing process development and engineering. Significant experience in defect reduction, yield increases, process control improvements, and process monitoring. Heavily involved in cross-functional diverse teams, including daily interactions with senior leadership and local process teams. Strong time management and technical communication skills. Searching for an opportunity to utilize an expansive engineering skillset in unique and noticeable ways.

ENGINEERING EXPERIENCE

***Process Control Systems Engineer*,** IM Flash Technologies, LLC, Lehi, UT *June 2018 – July 2019*
1 yr 0 mos

- Served as process control Subject Matter Expert for semiconductor manufacturing line
- Using state-space for single and multiple input/output systems to improve process models and reduce wafer to wafer variation by as high as 40%
- Utilized Statistical Process Control (SPC) principles to monitor ~50 processes and identify controller issues
- Developed robust Web App using HTML, JavaScript, and Python to create area documentation repository
- Presented streamlined and innovative controller logic to global manufacturing colleagues in Singapore and Japan

***RDA Module Owner*,** IM Flash Technologies, LLC, Lehi, UT *August 2015 – June 2018*
2 yr 10 mos

- Led and directed multi-process area focus teams to drive defect reduction and improve wafer yields by ~25%-50% using Real-Time Defect Analysis (RDA)
- Utilized IDEAS (Identify, Define, Evaluate, Act, Share) problem solving techniques to determine root cause and initiate CAPAs within team
- Collected necessary defect data without exceeding Wafer Inspection and SEM (Scanning Electron Microscope) tool utilization constraints
- Improved line yields by 35% by identifying issues found during Wafer Inspection and SEM data monitoring
- Authored and shared technical reports on analyzation of defect data associated with experimental processes
- Completed internal leadership program and absorbed immediate manager's duties during role transition

***RDA Development Engineer*,** Micron Technology, Inc., Boise, ID *January 2014 – August 2015*
1 yr 8 mos

- Developed innovative, industry-leading manufacturing processes for three next-generation semiconductors
- Increased wafer starts by 10% by identifying issues found during Wafer Inspection and SEM data monitoring
- Identified undiscovered defect modes associated with process development
- Analyzed experimental data and reported defect issues to appropriate process teams

***Senior Design Project*,** Boise State University, Idaho National Laboratory *October 2012 – May 2013*

- **Task:** Predict lifetime creep behavior in next-generation alloys using CAD and mathematical modeling
- **Actions:** Employed SolidWorks FEA to model and predict creep in samples
- Designed and constructed experimental setup to run successful creep tests on alloys
- Collected experimental data in addition to simulations to better characterize failed samples
- **Result:** Findings published in International Journal of Undergraduate Research and Creative Activities

EDUCATION, SKILLS, AND PUBLICATIONS

B.S. in Mechanical Engineering**, Boise State University***,* Boise, ID*,* May 2013
Minor in Mathematics, **Boise State University**, Boise, ID, May 2013

Skills and Involvement: JMP Statistical Software, JMP Scripting Language, Microsoft Office, SPC, DOE, ANOVA, Certified Engineer in Training (EIT), SolidWorks, Matlab, Python, HTML, JavaScript, Boise State Athletics Tutor

Allen, Justin et al. (2014) "Predicting Creep in Alloy 617 Pressurized Tubes Using Uniaxial Bar Test Data", International Journal of Undergraduate Research and Creative Activities: Vol. 6, Article 2.