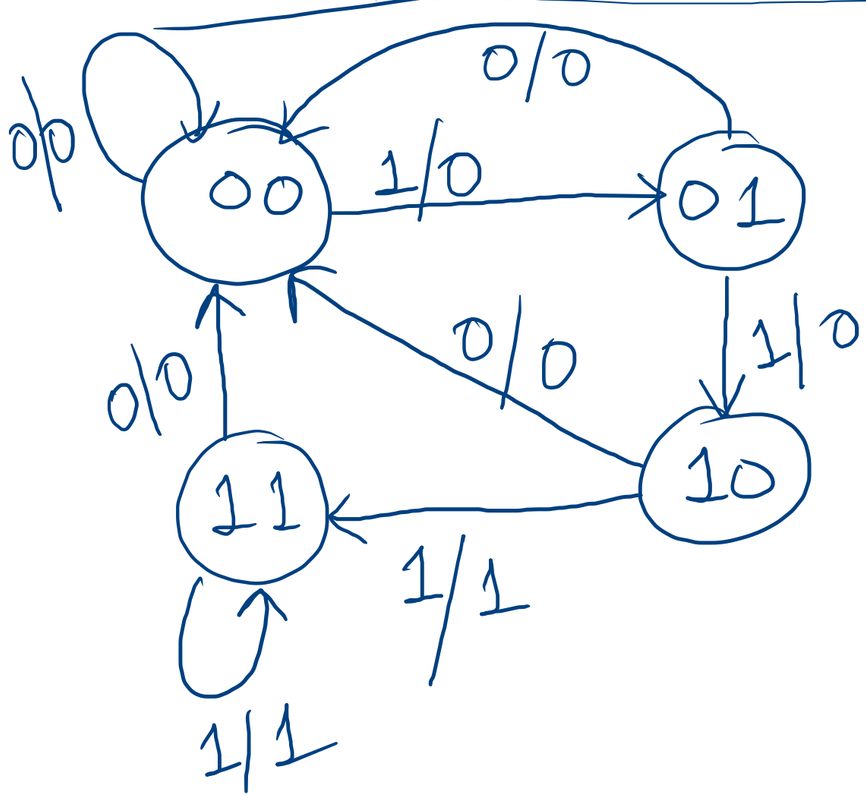
Design a circuit to detect 3 or more 1s in a serial bit stream using T flip flops.

i/p bit stream X — 0 1 0 1 1 0 1 1 1 1

o/p Z — 0 0 0 0 0 0 0 0 1 1



1 1 1

1 0 1 1

00 A – initial state

01 B – when first 1 is received.

10 C – when system receives 2 consecutive 1s.

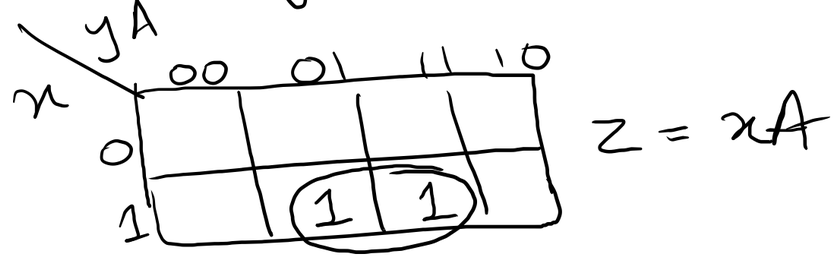
11 D – when systems 3 or more consecutive 1s.

State table

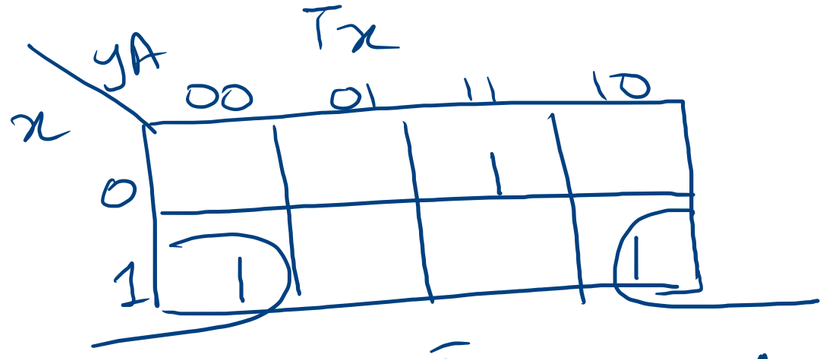
	PS		I/p	NS		Flipflop i/ps		o/p
	x	y	A	x^+	y^+	Tx	Ty	Z
A	0	0	0	0	0	0	0	0
A	0	0	1	0	1	0	1	0
B	0	1	0	0	0	0	1	0
B	0	1	1	1	0	1	1	0
C	1	0	0	0	0	1	0	0
C	1	0	1	1	1	0	1	1
D	1	1	0	0	0	1	1	0
D	1	1	1	1	1	0	0	1

$$Ty = \bar{y}A + y\bar{A} + \bar{x}A$$

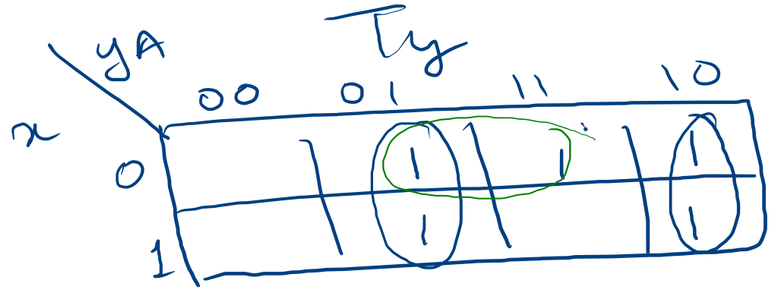
$$= y \oplus A + \bar{x}A$$



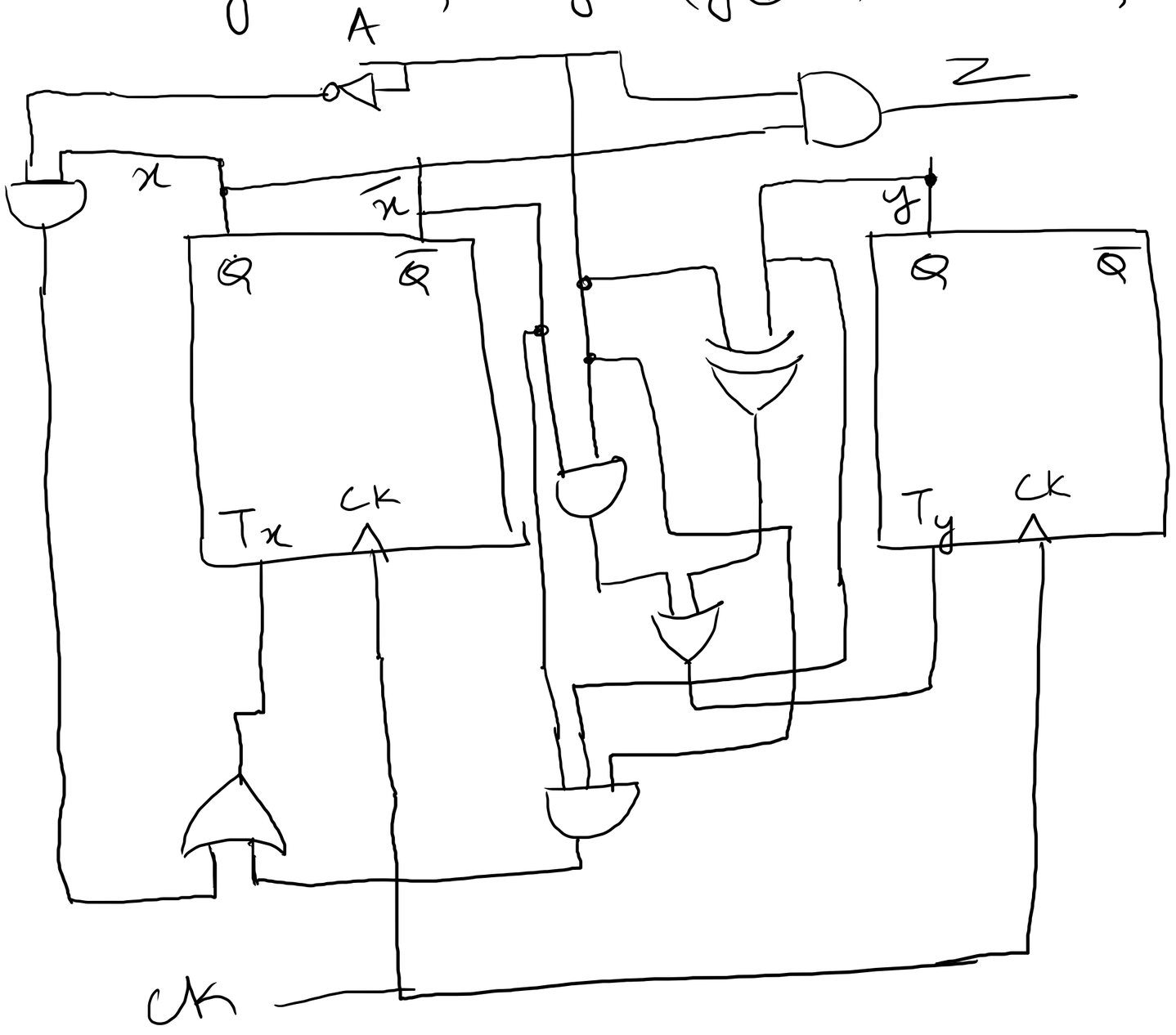
$$Z = xA$$



$$Tx = x\bar{A} + \bar{x}yA$$



$T_x = x\bar{A} + \bar{x}yA$, $T_y = (y \oplus A) + \bar{x}A$, $Z = xA$



Design of counters

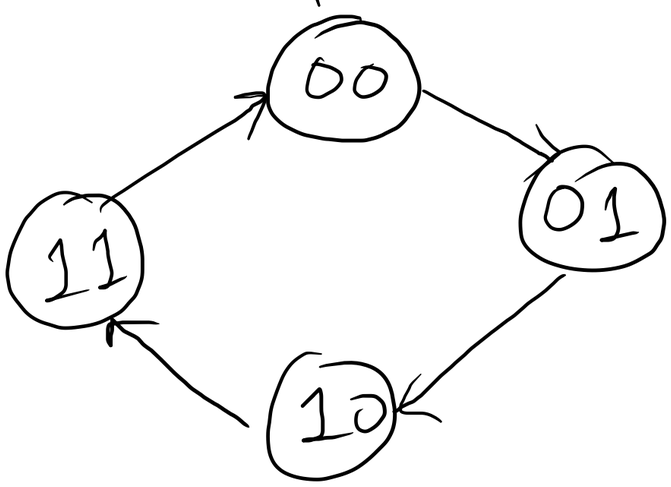
A group of ffs — register

A counter is a synchronous sequential circuit that moves through a predefined sequence of states upon the application of clock pulses.

Binary counter — n bit binary counter.

can count from 0 to $2^n - 1$.

Design a 2 bit counter in the sequence 00, 01, 10, 11 and repeat the sequence using T ffs.



PS		NS		FF i/ps	
x	y	x^+	y^+	T_x	T_y
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

T_x

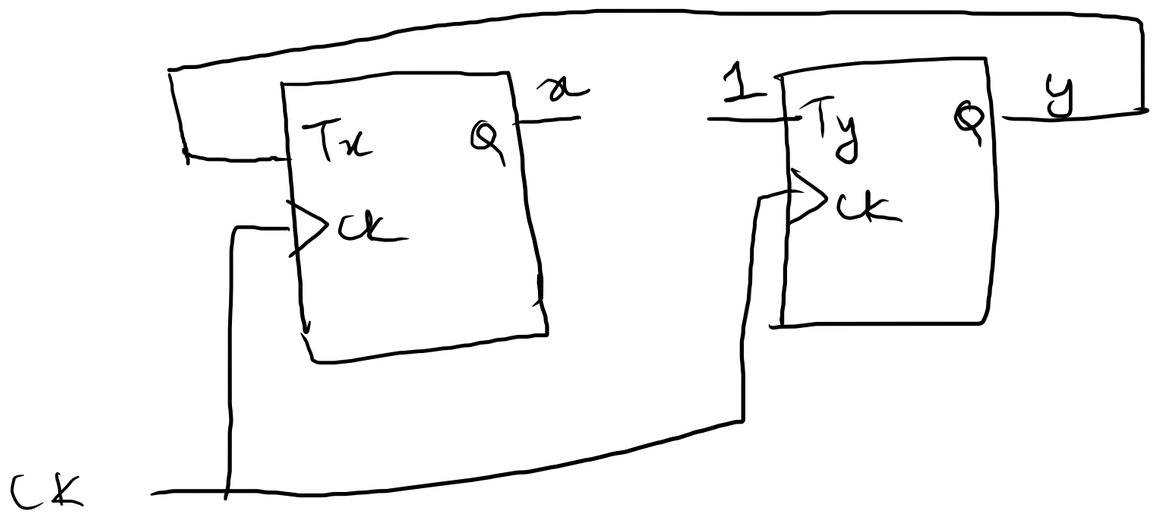
x \ y	0	1
0		1
1		1

$T_x = y$

T_y

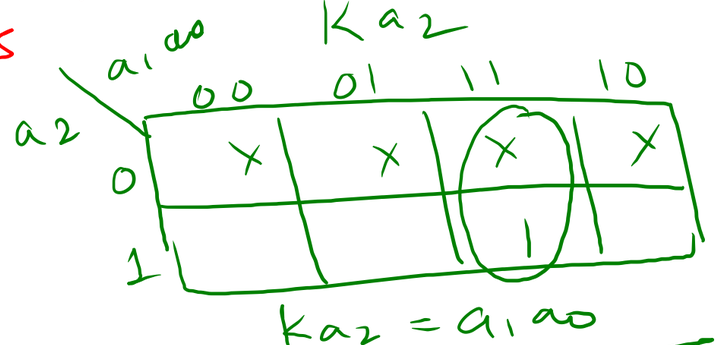
x \ y	0	1
0	1	1
1	1	1

$T_y = 1$

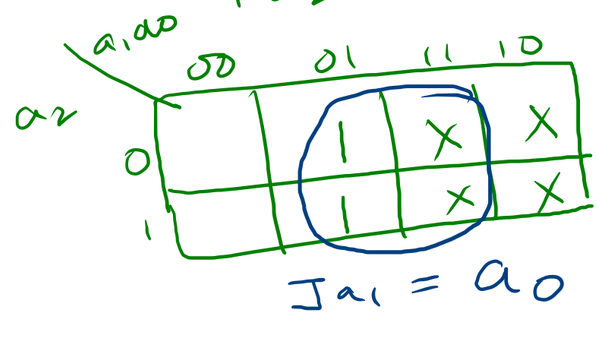


Design a 3 bit counter to count in the sequence 000 to 111 & return to 000 & repeat. Use JF ffs

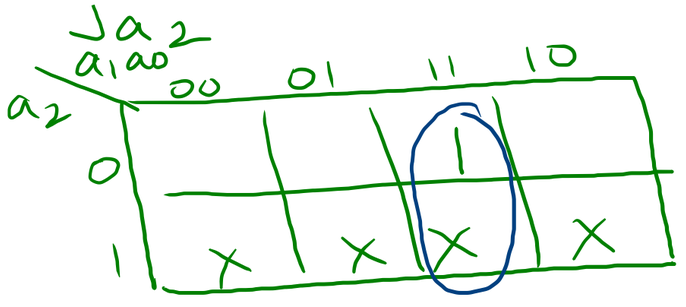
PS	NS	FF i/ps					
$a_2\ a_1\ a_0$	$a_2^+\ a_1^+\ a_0^+$	J_{a_2}	K_{a_2}	J_{a_1}	K_{a_1}	J_{a_0}	K_{a_0}
0 0 0	0 0 1	0	x	0	x	1	x
0 0 1	0 1 0	0	x	1	x	x	1
0 1 0	0 1 1	0	x	x	0	1	x
0 1 1	1 0 0	1	x	x	1	x	1
1 0 0	1 0 1	x	0	0	x	1	x
1 0 1	1 1 0	x	0	1	x	x	1
1 1 0	1 1 1	x	0	x	0	1	x
1 1 1	0 0 0	x	1	x	1	x	1



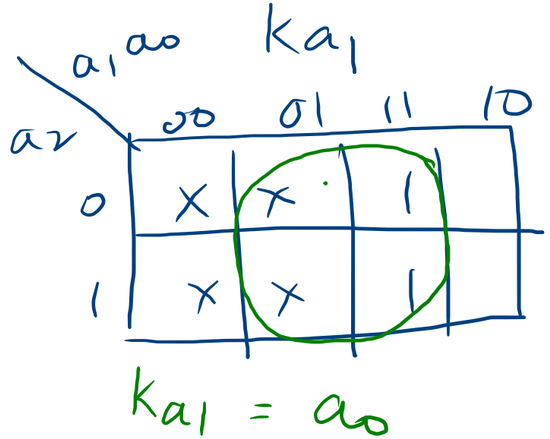
$Ka_2 = a_1 a_0$



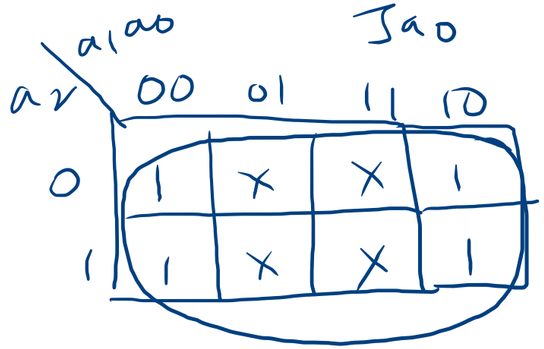
$Ja_1 = a_0$



$Ja_2 = a_1 a_0$



$K_{a_1} = a_0$



$J_{a_0} = 1$

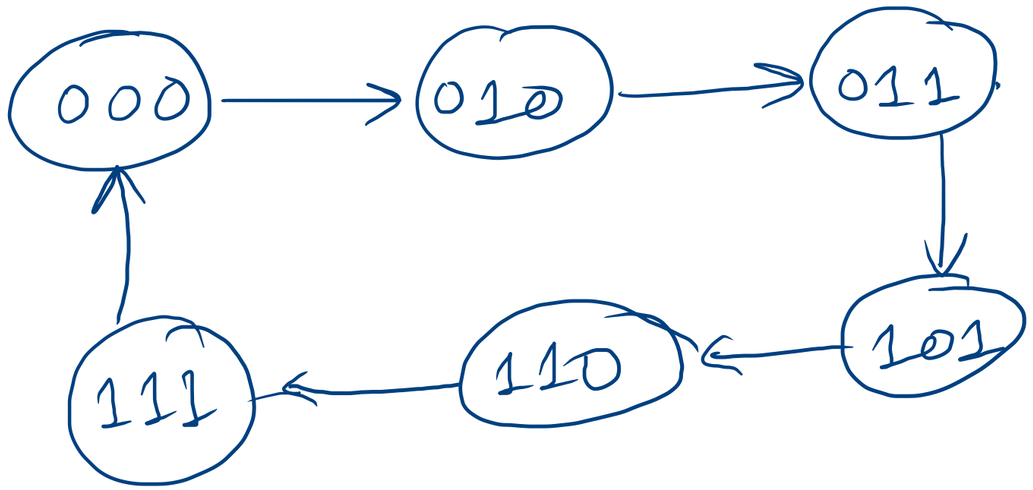
$K_{a_0} = 1$

Design a 3 bit counter that counts the sequence

000, 010, 011, 101, 110, 111 & repeats the sequence

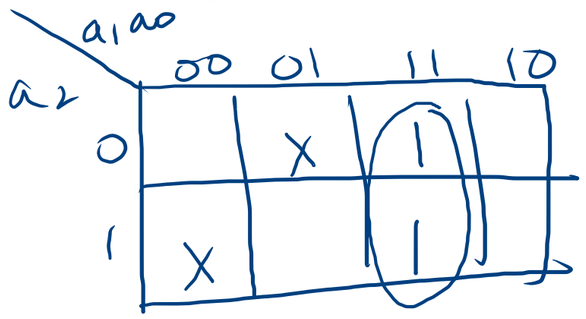
Use T ffs.

2 unused states (001 & 100)



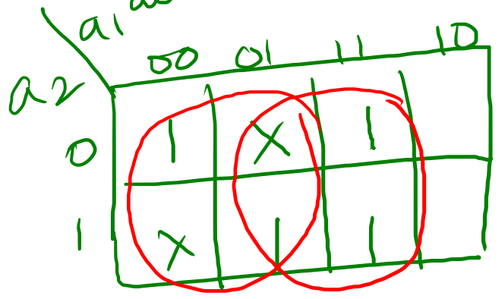
PS $a_2\ a_1\ a_0$	NS $a_2^+\ a_1^+\ a_0^+$	T_{a_2}	T_{a_1}	T_{a_0}
000	010	0	1	0
010	011	0	0	1
011	101	1	1	0
101	110	0	1	1
110	111	0	0	1
111	000	1	1	1

T_{a_2}

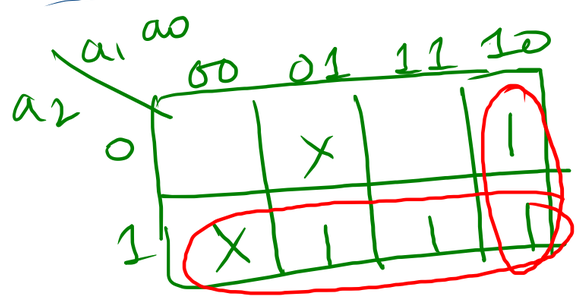


$T_{a_2} = a_1 a_0$

T_{a_1}



$T_{a_1} = a_0 + \overline{a_1}$



$T_{a_0} = a_2 + a_1 \overline{a_0}$

Draw the ckt.

Application of ffs.

(1) Counters

(2) Frequency divider

Up counter.

0 0

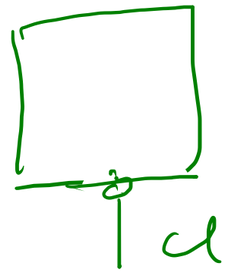
0 1

1 0

1 1

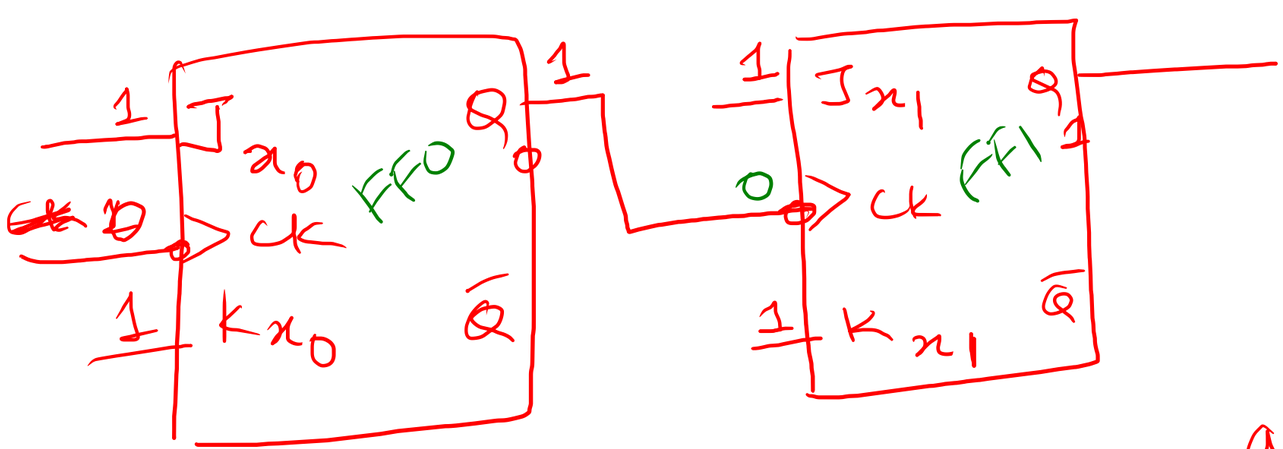
pulse

CK	Q_1	Q_0
0	0	0
1	0	1



Asynchronous sequential ckts

Asynchronous 2 bit up counter using JK ff.



active low

$Q_0 = 0$ FF1 will work

-ve edge triggered

JK = 1