

Syllabus

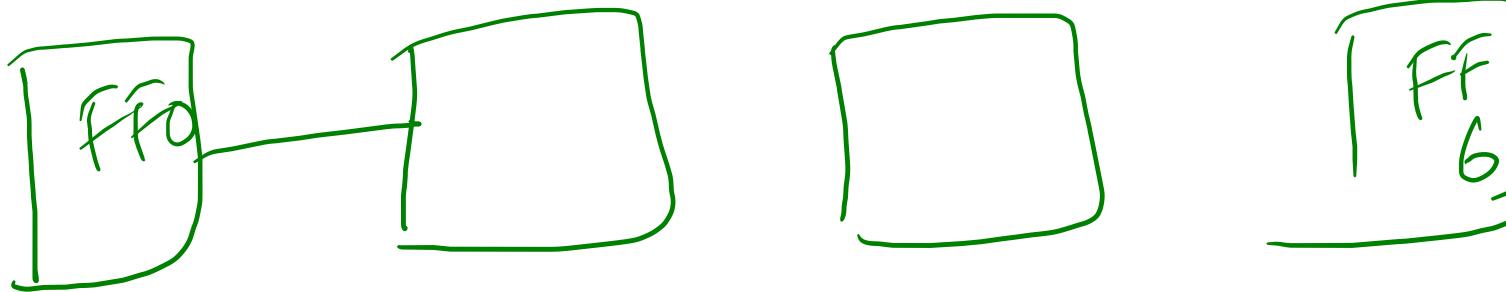
Combinational circuits

## Registers

Combination of Jf's.

64-bit

64 bit long word



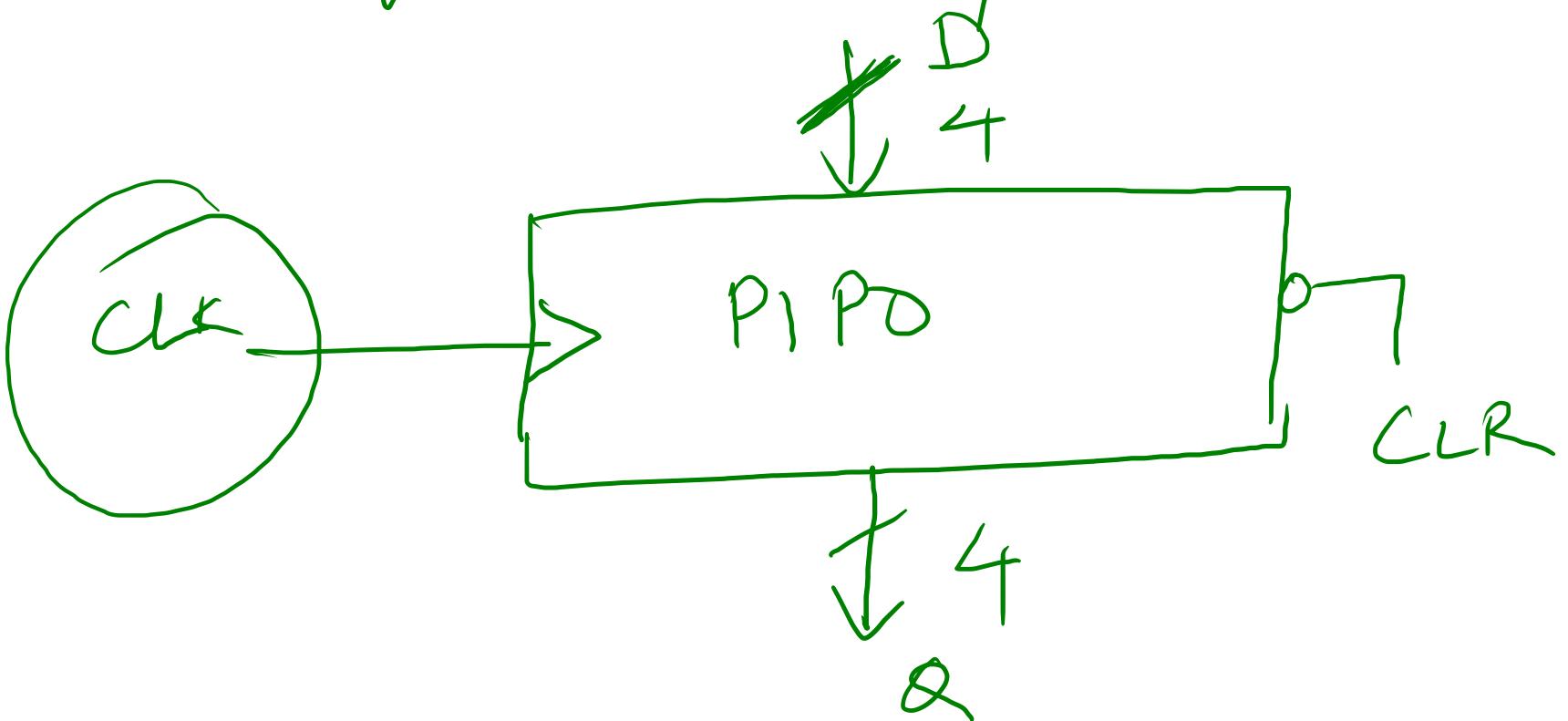
Different) types of registers

- ① PIPO ( Parallel In Parallel Out )
- ② SI SO ( Serial In Serial Out )
- ③ SI PO ( Serial In Parallel Out )
- ④ PI SO ( Parallel In Serial Out )

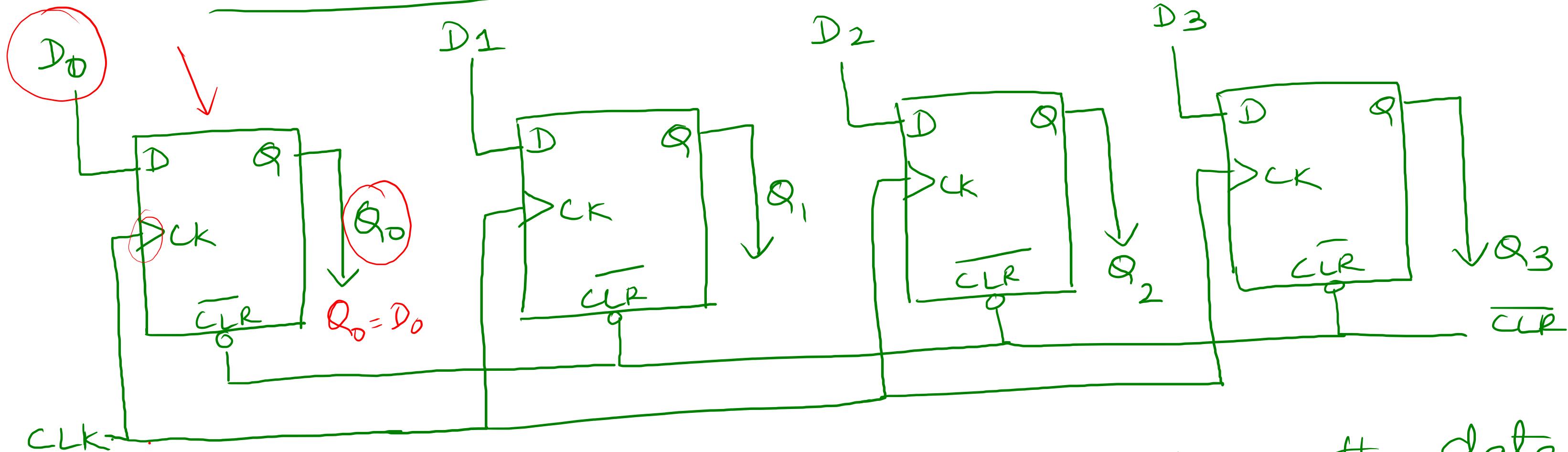
## PIPO

Data is fed in parallelly and data is read out parallelly across multiple JF's.

Symbolic representation



# 4 bit PIPD register (synchronous circuit)



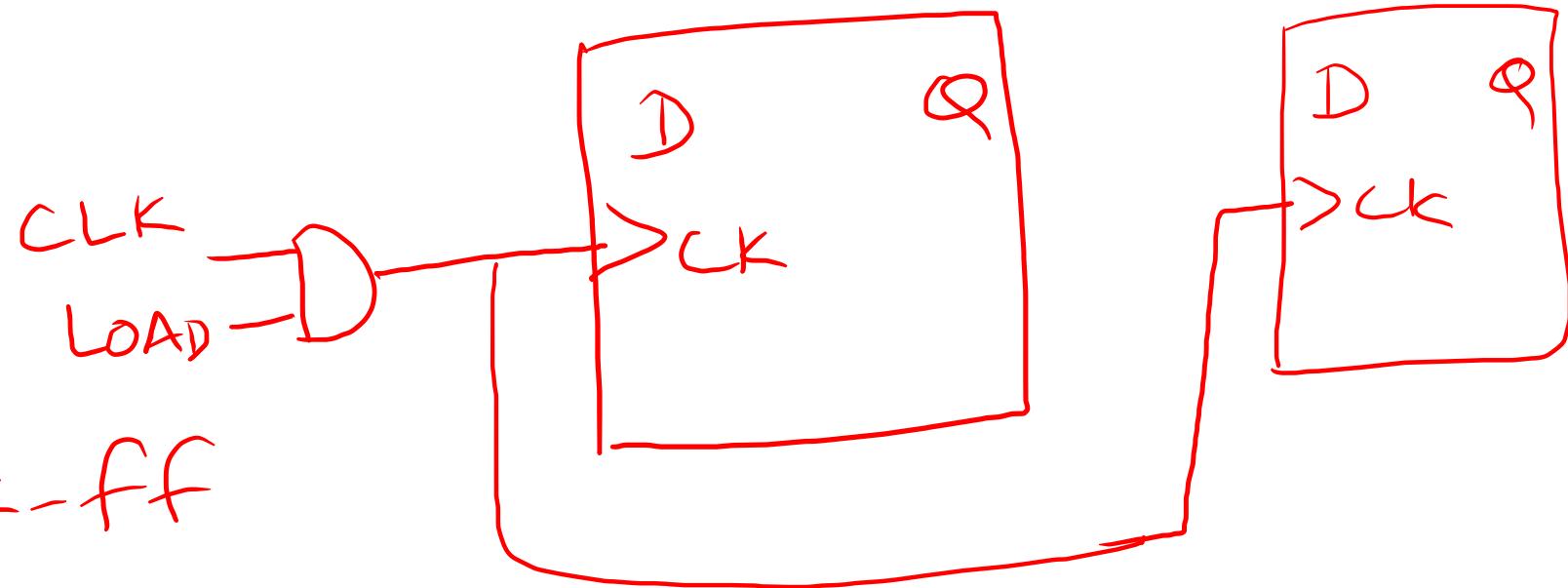
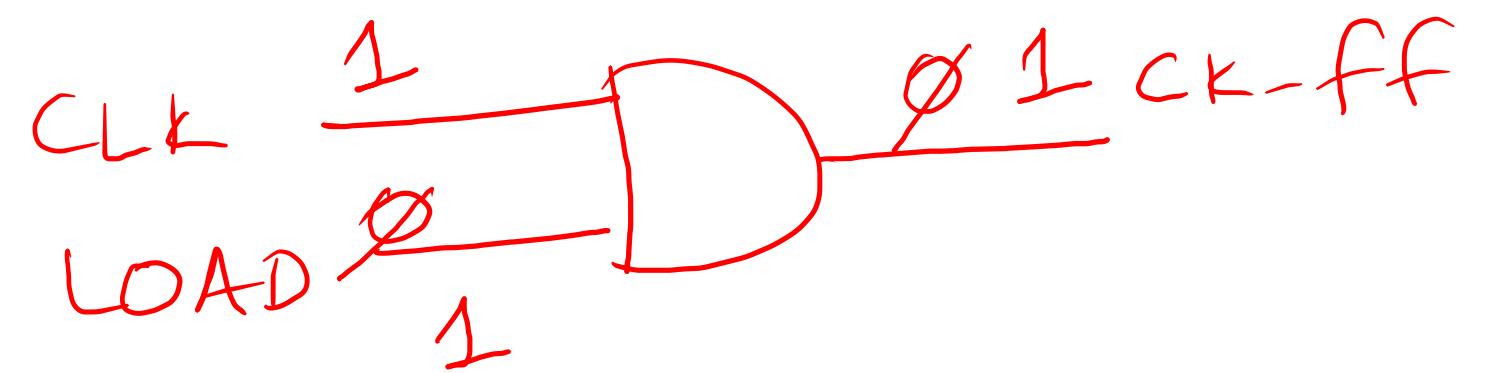
When active edge of clock arrives the data word  $D_0 D_1 D_2 D_3$  gets stored in the register & is available on the outputs  $Q_0 Q_1 Q_2 Q_3$ .

## Additional control signal.

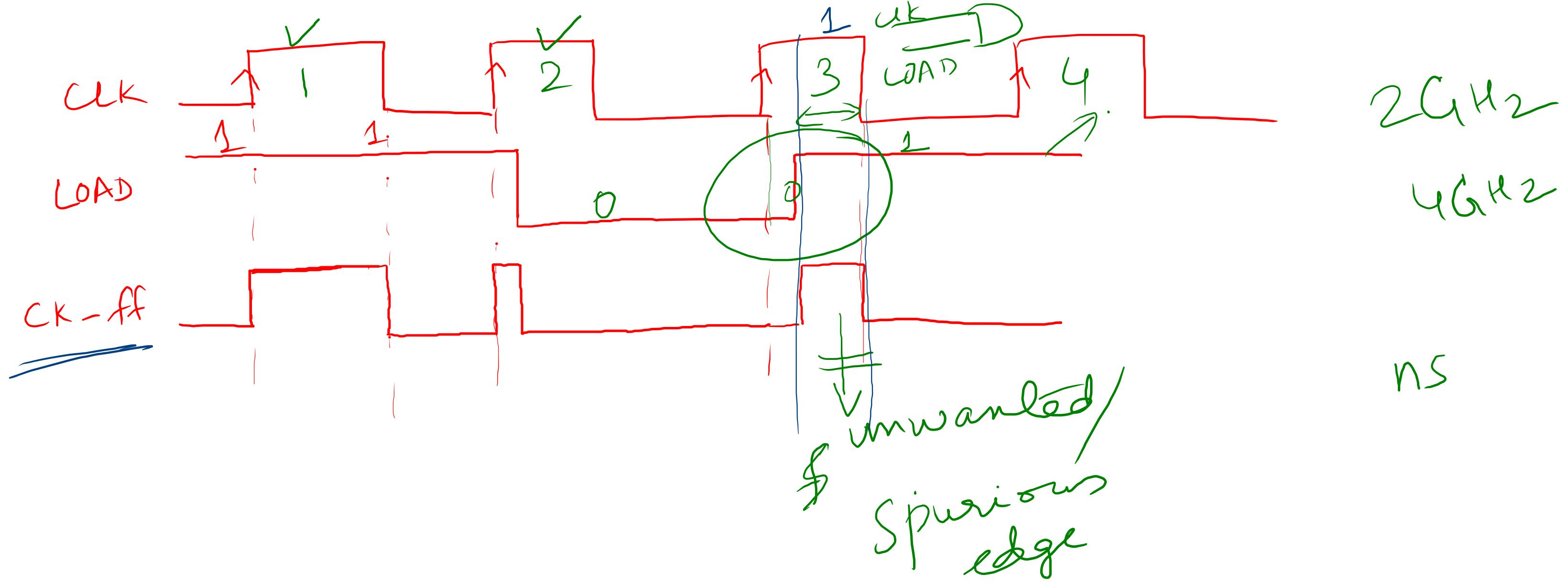
LOAD sig - tells us when we need to change the content of the register.

### 2 Approaches

#### ① Gated clock



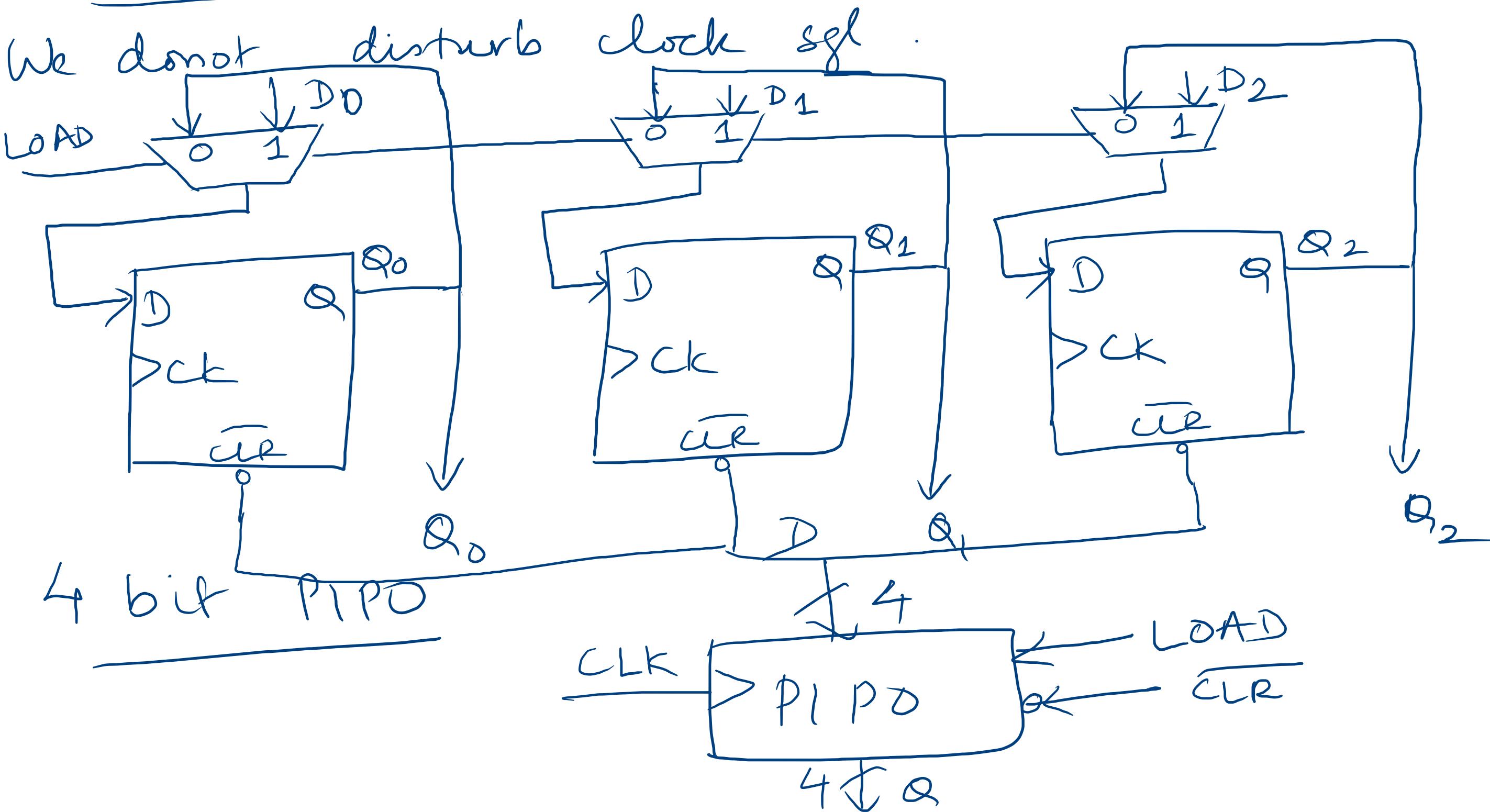
Timing issue.



②

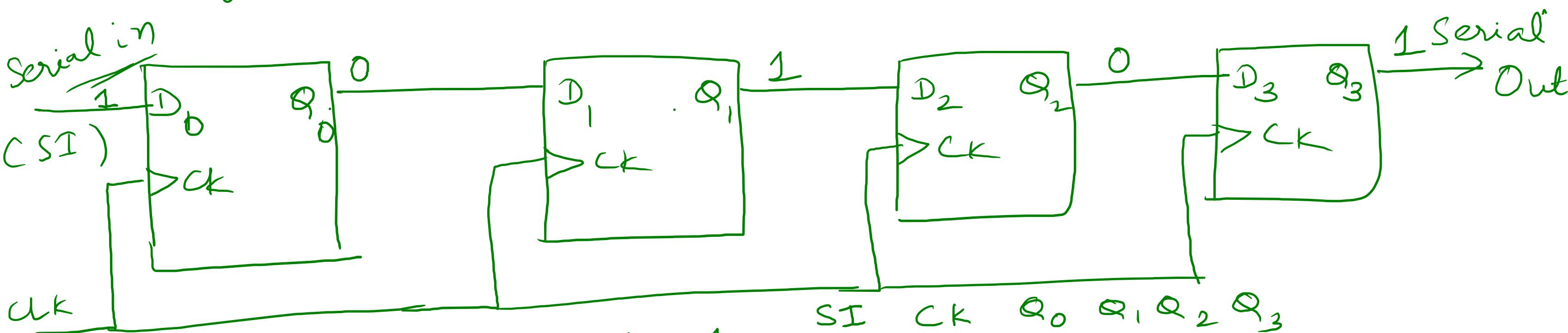
## Multiplexer circuit .

Recommended approach .



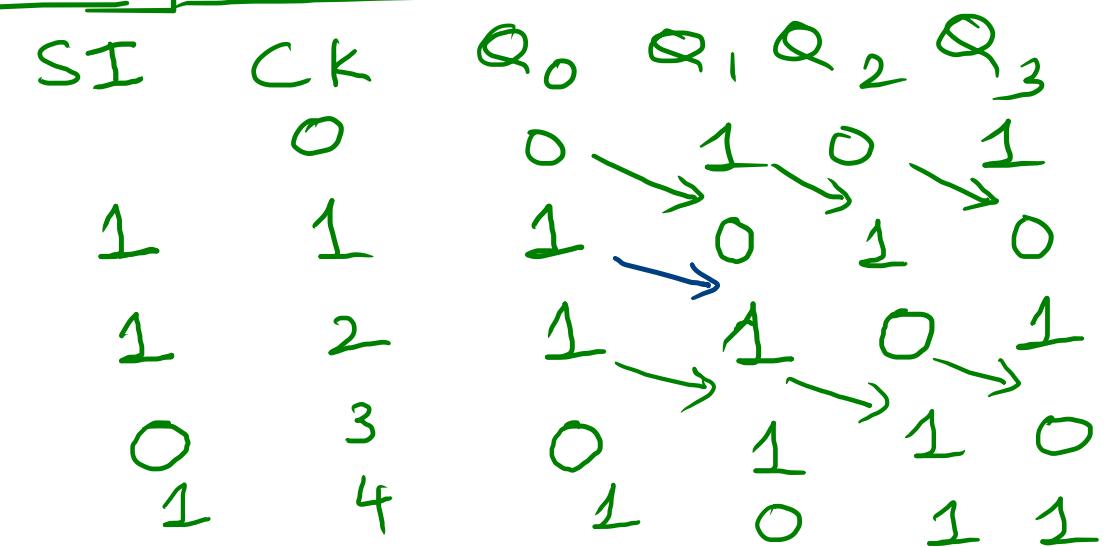
# Serial In Serial Out (SISO) [Shift register]

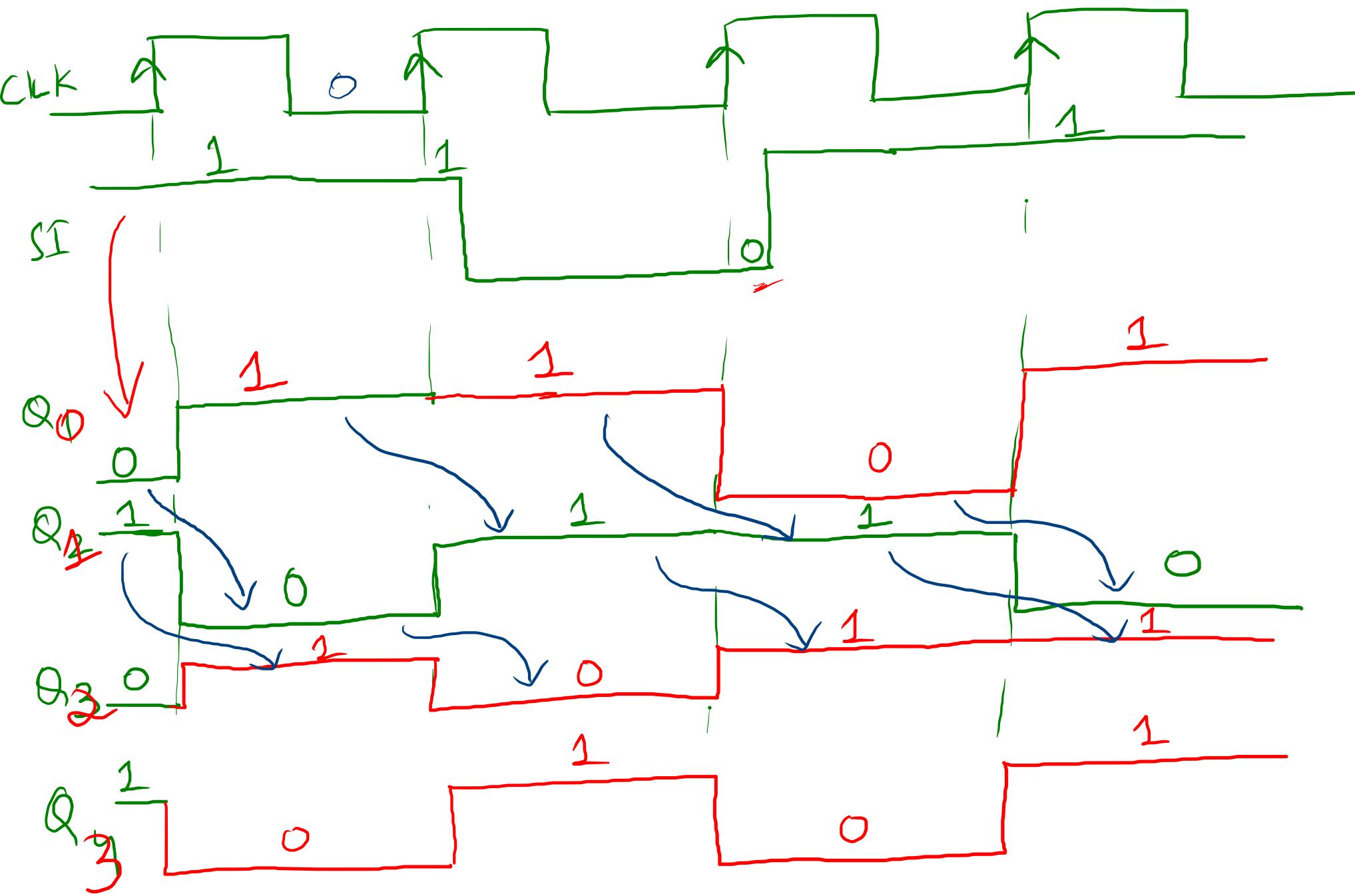
Data can be stored and can be shifted to left or right when a shift signal is applied.



$$Q_0 \ Q_1 \ Q_2 \ Q_3 = 0101$$

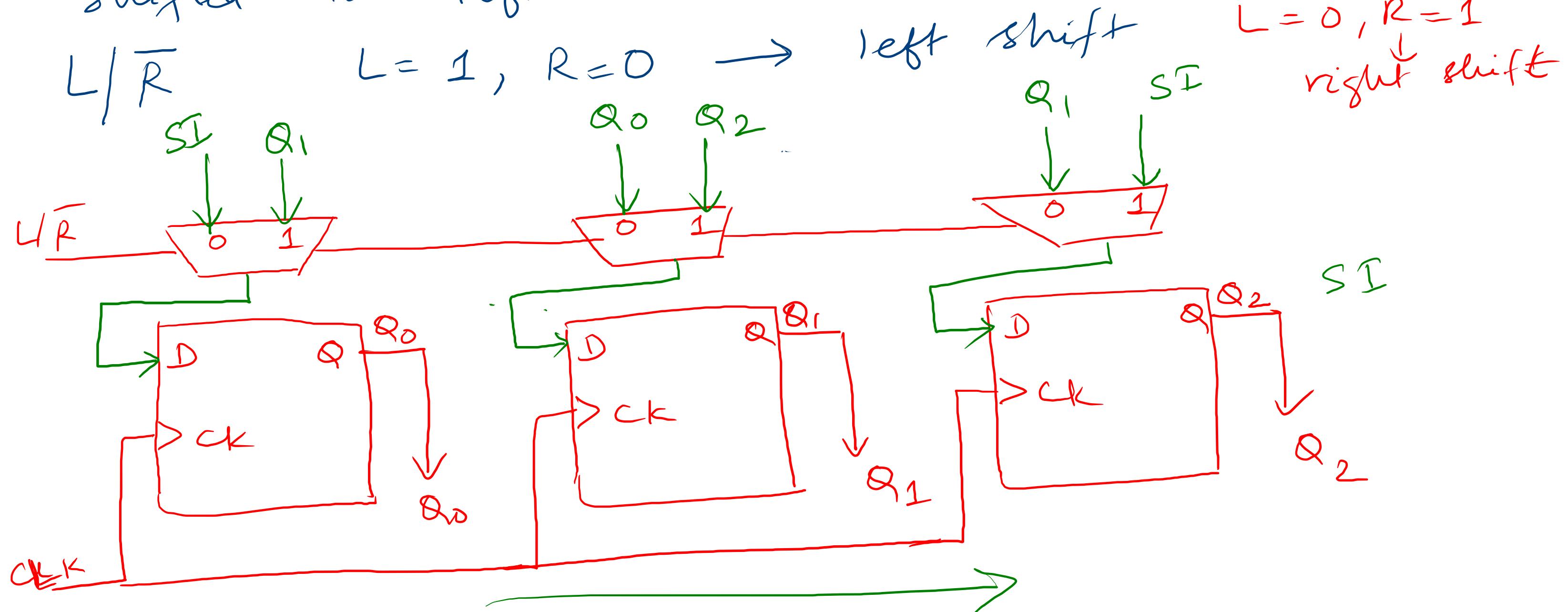
Initial state of ff





# Bidirectional shift register

Ctrl i/p which decides whether data should be shifted to left or right.



# Universal shift register

$S_1\ S_0$

Operation

0 0

Freeze (Retain content)

0 1

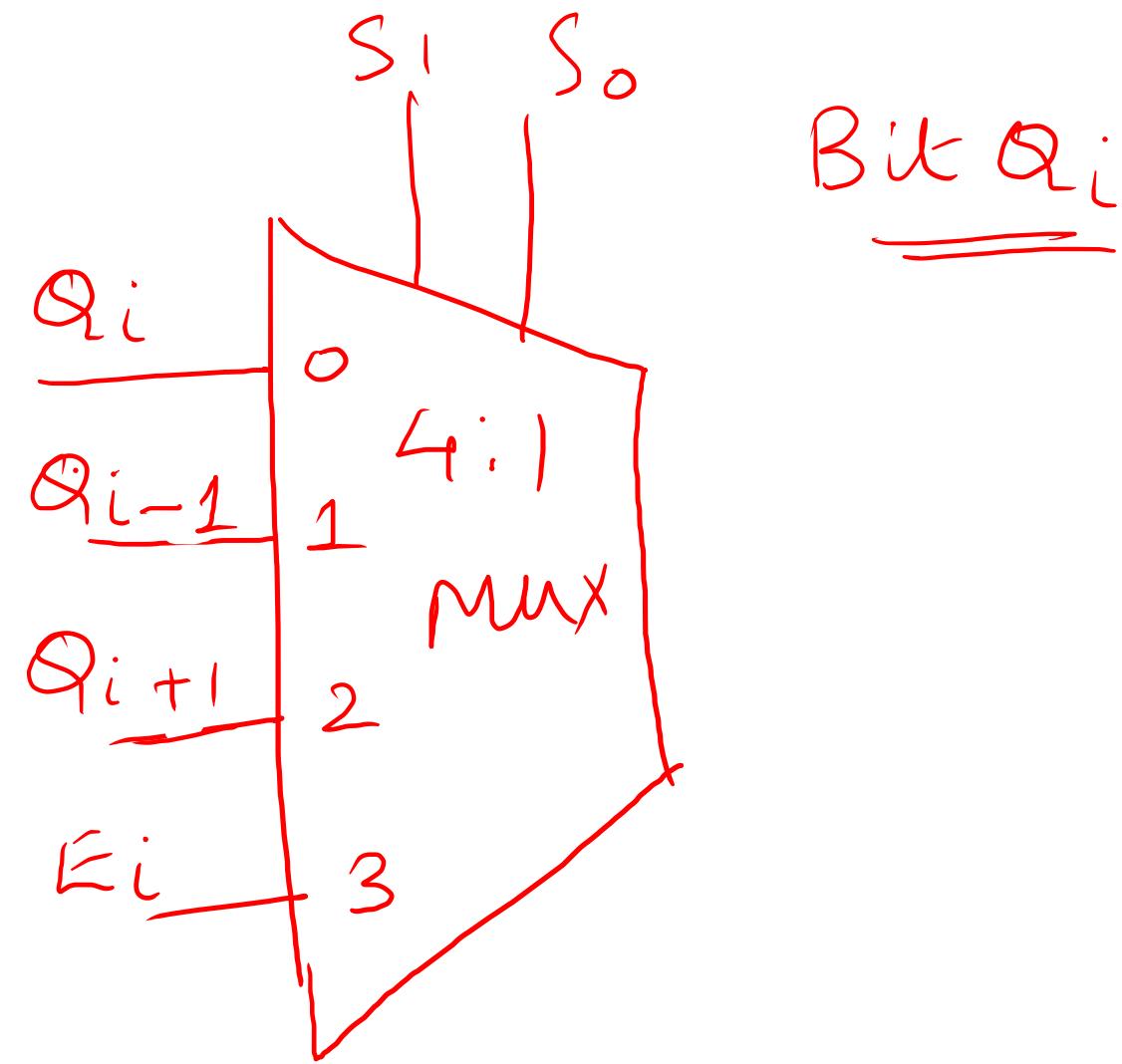
Right Shift

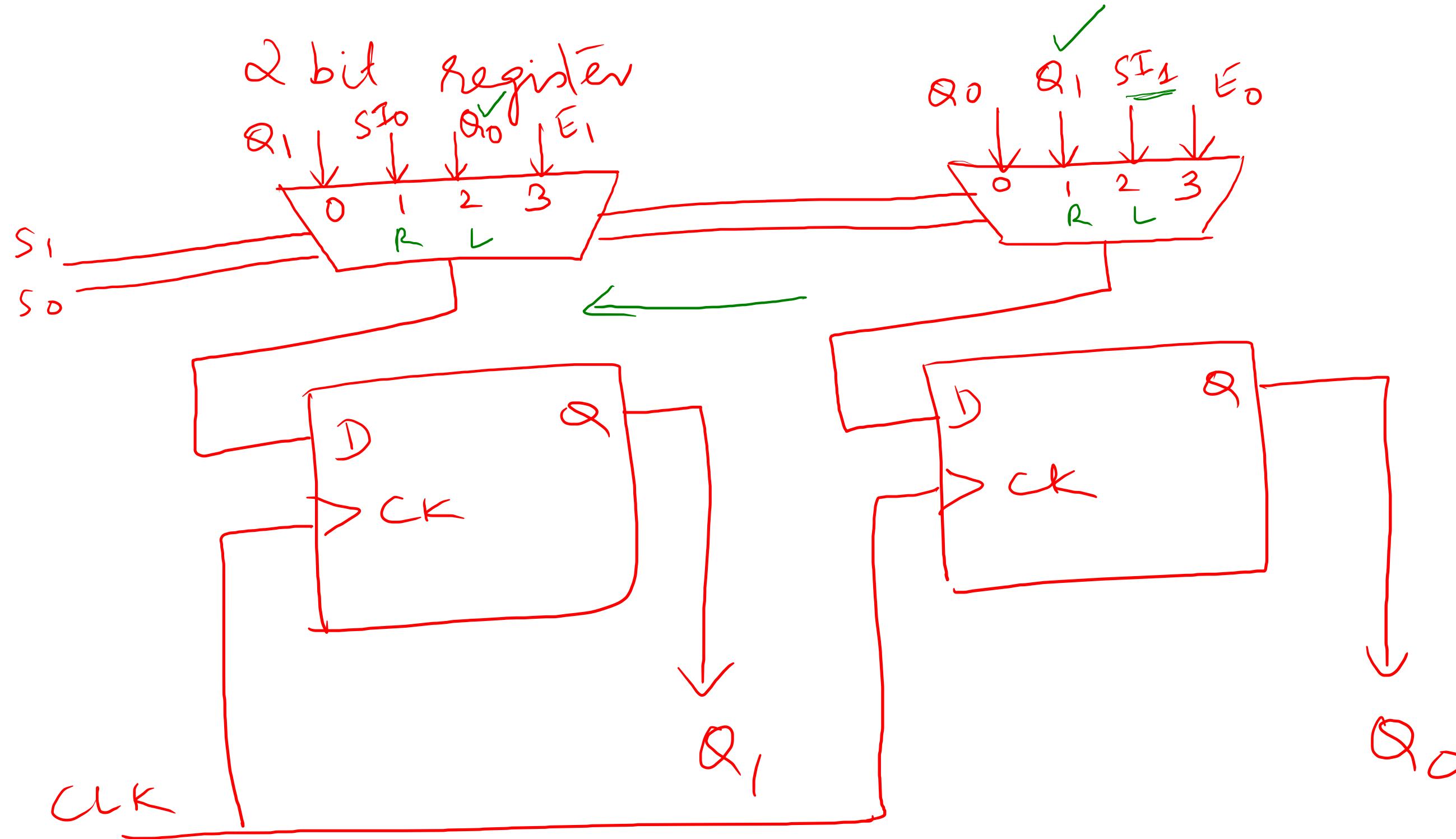
1 0

Left Shift

1 1

Parallel Load  
(External load)





## Points to remember

Logical right / left shift for an unsigned number

eg 0001  $\Rightarrow$  1

$$1000 \Rightarrow 8 = 1 \times 2^3$$

(after 3 shifts)

0000

Condition :  
a 1 should not be shifted  
out during the operation.

Signed no.

We retain the sign bit when we shift.

Right shift eg

$\begin{array}{r} -2^3 \ 2^2 \ 2^1 \ 2^0 \\ 1 \ 1 \ 0 \ 0 \end{array}$

$$= -8 + 4 = -4$$

$\begin{array}{r} 1 \ 1 \ 1 \ 0 \\ \downarrow \quad \downarrow \\ 1 \ 1 \ 1 \ 0 \end{array}$

$$= -8 + 4 + 2 = -2$$

$\begin{array}{r} 1 \ 1 \ 1 \ 1 \\ \downarrow \quad \downarrow \quad \downarrow \\ 1 \ 1 \ 1 \ 1 \end{array}$

$$= -8 + 4 + 2 + 1 = -1$$

LS

$\begin{array}{r} 1 \ 1 \ 1 \ 1 \\ \downarrow \quad \downarrow \\ 1 \ 1 \ 1 \ 0 \end{array}$

$$= -1$$

$\begin{array}{r} 1 \ 1 \ 1 \ 1 \\ \downarrow \quad \downarrow \quad \downarrow \\ 1 \ 1 \ 0 \ 0 \end{array}$

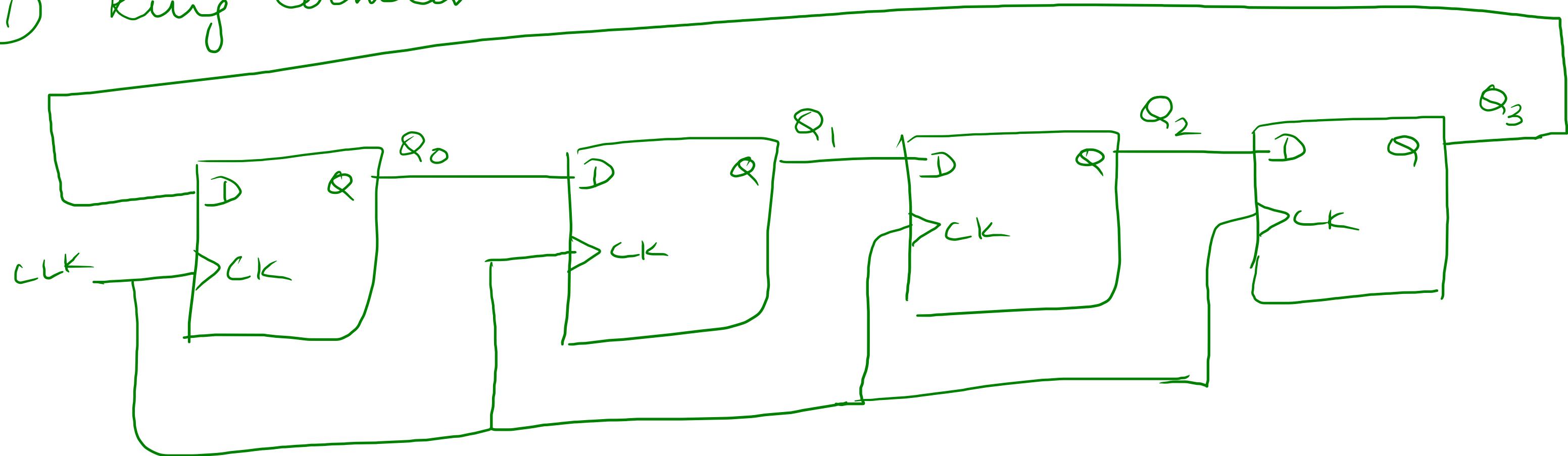
$$= -2$$

$$= -4$$

\*

## Special Registers

### ① Ring Counter



Forbidden state

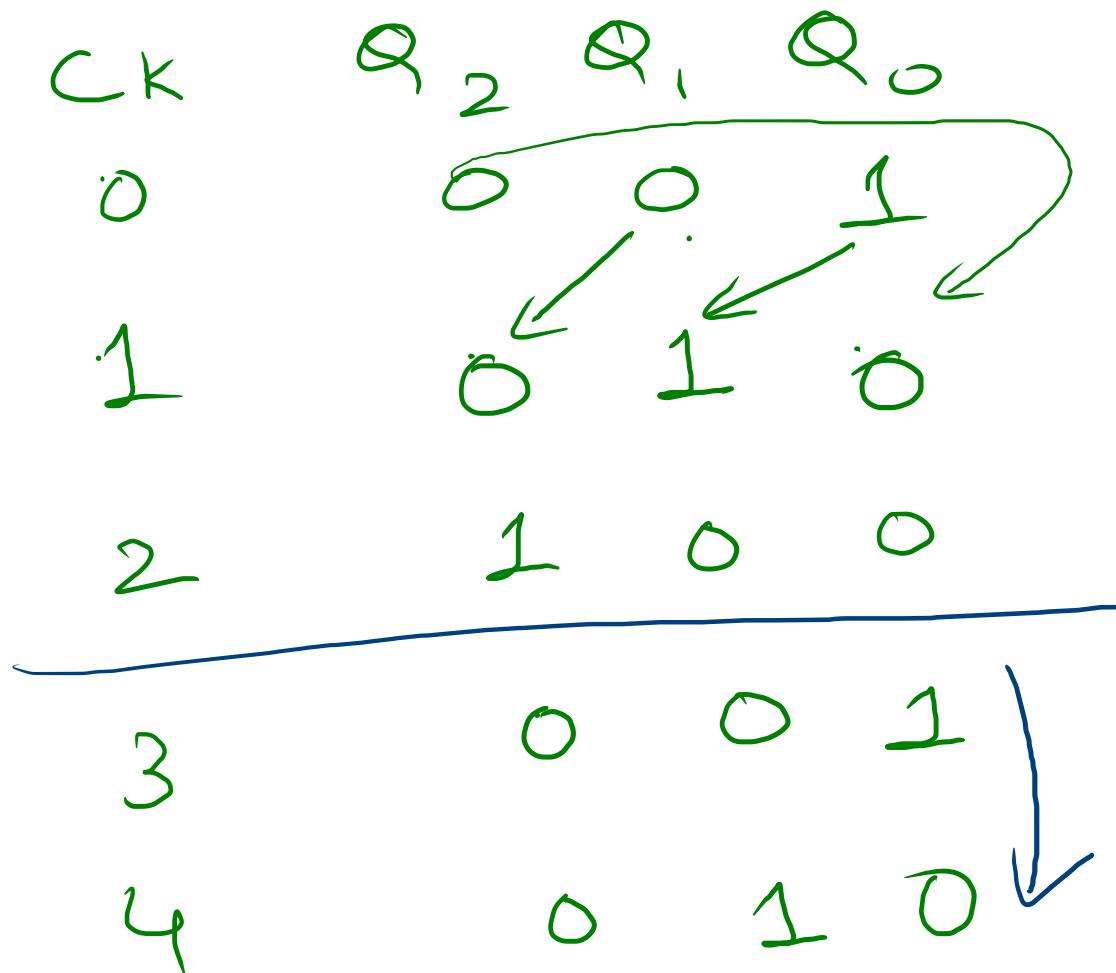
→ 0000

{

Initial condition

( 3 bit ring counter)

$$Q_0 Q_1 Q_2 = 100$$



Pattern in a 3 bit ring counter repeats after 3 clocks

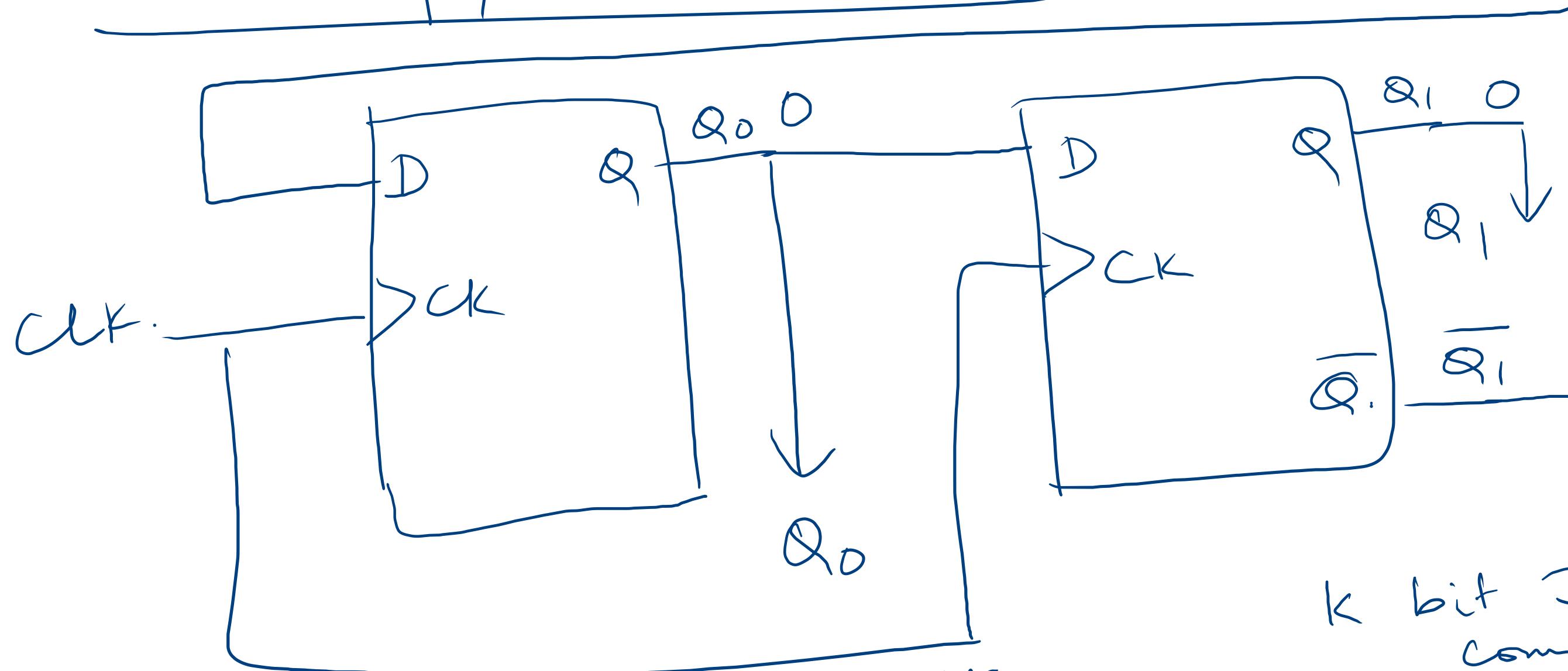
$\xrightarrow{\text{clock pulses}}$

$\xrightarrow{\text{k bit ring counter}}$

repeat K

Twisted ring / Johnson counter

3 bit



2 bit counter - 4 patterns  
3 bit counter - 6 patterns

$k$  bit Johnson counter  
 $\downarrow$   
2 $k$  unique patterns.



