PRACTICE SHEET 3

1. Using minimum number of 2:1 multiplexers, realize NOT, AND, OR, NAND, NOR, XOR and XNOR (2-input) gates with proper Boolean justification for each.

2. A circuit has eight data inputs (A = a7a6 . . . a1a0), one control input P, and an 8-bit output (Y = y7y6 . . . y1y0). Design the circuit for the following specifications most economically with respect to the number of gates utilized:
   (a) Y = −A using ones' complement representation when P = 0 and Y = A otherwise
   (b) Y = −A using ones' complement representation when P = 1 and Y = A otherwise

3. Find the values of two-valued variables A, B, C, and D by solving the following set of simultaneous equations:
   $A' + AB = 0$
   $AB = AC$
   $AB + AC' + CD = C'D$

4. (a) Show that f(A, B, C) = A′BC + AB′ + B′C′ is a universal operation.
   (b) Assuming that a constant value 1 is available, show that f(A, B) = A′B (together with the constant) is a universal operation.

5. The majority function M(x, y, z) is equal to 1 when two or three of its arguments equal 1, that is,
   M(x, y, z) = xy + xz + yz = (x + y)(x + z)(y + z)
   Show that:
   (a) Show that M(a, b, M(c, d, e)) = M(M(a, b, c), d, M(a, b, e)).
   (b) Show that M(x, y, z), the complementation operation, and the constant 0 form a functionally complete set of operations.
   (c) Find the simplest switching expression f(A, B, C, D) corresponding to the network of Fig. 1.

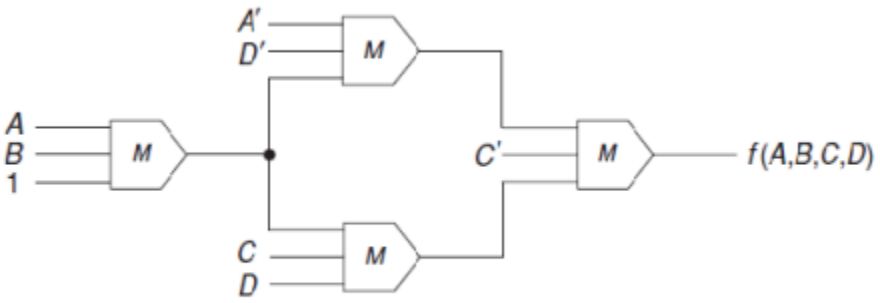

Figure 1: Majority circuit

6. You are presented with a set of requirements under which an insurance policy will be issued. The applicant must be

   1. a married female 25 years old or over, or

   2. a female under 25, or

   3. a married male under 25 who has not been involved in a car accident,

   or

   4. a married male who has been involved in a car accident, or

   5. a married male 25 years or over who has not been involved in a car accident.

   Variables w, x, y, and z assume truth value 1 in the following cases:

   w = 1 if the applicant has been involved in a car accident;

   x = 1 if the applicant is married;

   y = 1 if the applicant is a male;

   z = 1 if the applicant is under 25.

   (a) Find an algebraic expression that assumes the value 1 whenever the policy should be issued.

   (b) Simplify algebraically the above expression and suggest a simpler set of requirements.

7. Prove that for every Boolean algebra:

   (a) $a + a'b = a + b$

   (b) if $a + b = a + c$ and $a' + b = a' + c$, then $b = c$

   (c) if $a + b = a + c$ and $ab = ac$, then $b = c$

8. Given the function T(w, x, y, z) = Σm(1, 3, 4, 5, 7, 8, 9, 11, 14, 15),

   (a) use the map to obtain the set of all prime implicants and indicate specifically the essential ones

   (b) find three distinct minimal expressions for T

   (c) find the complement T directly from the map

9. A newly proposed 3-input gate T has logical properties that is defined in Fig. 2.

   (a) Prove that if the logic value 1 is given, then any switching function can be realized using only the newly proposed T gates, that is, T gates along with the logic value 1 are functionally complete.

   (b) Realize, by means of two T gates, the function f(w, x, y, z) = Σm(0, 1, 2, 4, 7, 8, 9, 10, 12, 15).

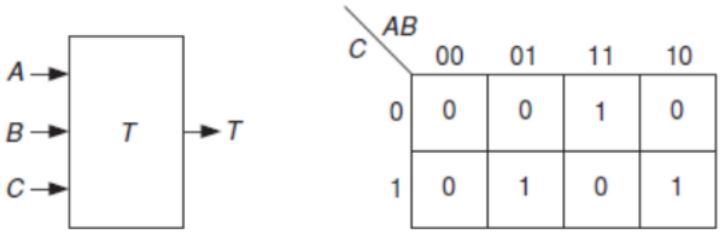

Figure 2: Gate T

10. A switching circuit has two control inputs (C1 and C2), two data inputs (X1 and X2), and one output (Z). The circuit performs one of the logic operations AND, OR, EQU (equivalence), or XOR (exclusive OR) on the two data inputs. The function performed depends on the control inputs:

$C1$	$C2$	*Function performed by the circuit*
0	0	OR
0	1	XOR
1	0	AND
1	1	EQU

   (a) Derive a truth table for Z.

(b) Use a Karnaugh map to find a minimum AND-OR gate circuit to realize Z.

11. A switching circuit has four inputs as shown in Fig. 3. A and B represent the higher and lower order bits of a binary number N1. C and D represent higher and lower order bits of a binary number N2. The output is to be 1 only if the product N1 × N2 is less than or equal to 2.

    (a) Find the minterm expansion for F and the minimal SOP form.

    (b) Find the maxterm expansion for F and the minimal POS form.

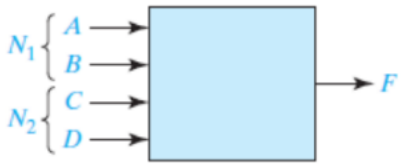

Figure 3: Switching circuit

12. Using only 2-input logic gates, design a 6-bit combined ones' complementer and two's complementer circuit most optimally, such that when the control input P = 1, circuit performs a ones' complement operation, and two's complement otherwise.

13. (a) Using only 2-input logic gates, design most optimally, a 5-bit circuit that computes Y = X + 2.

    (b) How will you re-design this circuit most optimally, by making minimal changes to the solution proposed in 13(a), to build a controlled incrementer logic that computes Y = X + 2 if P = 0 and Y = X + 1 if P = 1?

14. Using only 2-input logic gates, design a 4-bit controlled decrementer circuit which accepts a 4-bit number A and outputs a 4-bit number Y and has an additional control bit P. If P = 0, $Y = A - 1$; otherwise $Y = A$.