Addressing modes.

① Immediate addressing mode.

MVI ACC, FF → operand / number

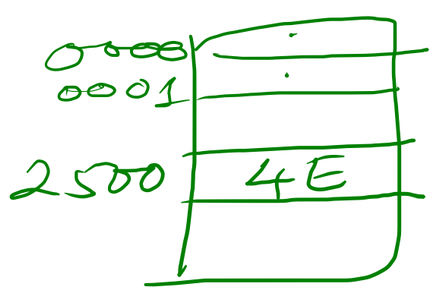
ACC ← FF

② Direct addressing mode

MOV ACC, Address of operand memory

eg MOV ACC, 2500

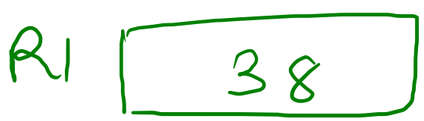
ACC ← 4E



(3) Register addressing mode

MOV ACC, R1

ACC ← 38

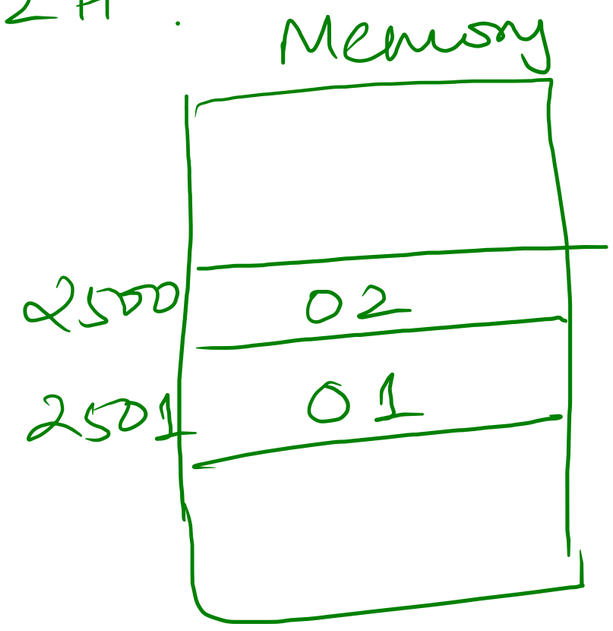


(1) WAP to store the number 49H into memory location 2501H. The number is entered by user.

```
IN   PORT A
.
STORE   2501H
```

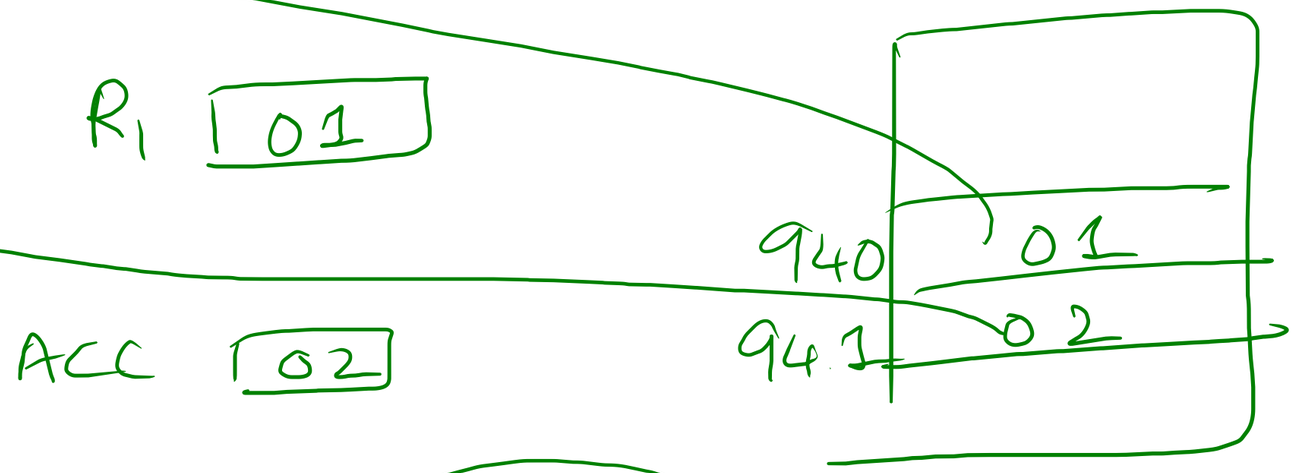
(2) Two nos are stored in memory locations 2500H and 2501H. WAP to add the numbers and store the result in 2502H.

```
LOAD    2500H
MOVE    R1, ACC
LOAD    2501H
ADD     R1
STORE   2502H
```



(3) Two nos are stored in memory location 940 H and 941 H. WAP to exchange the nos using MOVE and LOAD STORE instructions only.

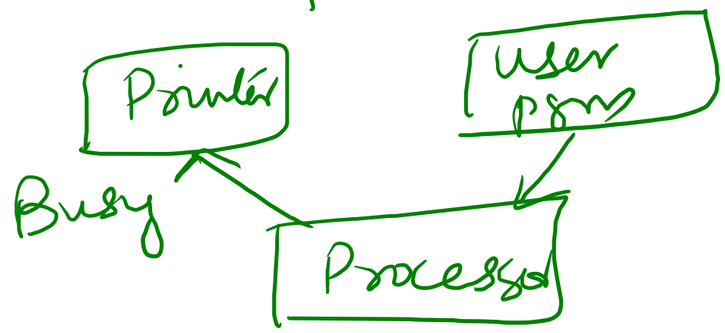
```
LOAD   940H
MOVE R1, ACC
LOAD   941H
STORE  940H
MOVE ACC, R1
STORE  941H
```



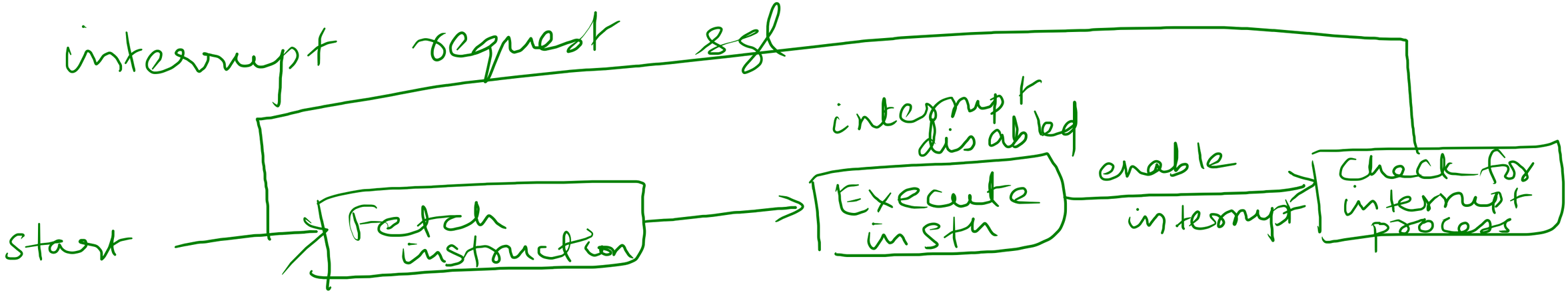
XCHG

Interrupts

All I/O or memory modules can interrupt the normal operation of the processor.



User program



2 approaches to handle multiple interrupts.

(1) Disable interrupt

ignores time critical tasks

(2) Priority list is generated

Printer	1
Flash drive	3
communication line	5

Increasing order of priority

t=0 – user pgm is executed

t=10 – printer sends interrupt request

t=15 – communication line send IR

t=20 – Flash drive sends IR

t=25 – Comm^n line instruction is complete.

t=25 – Flash drive routine executed

t=30

Mem- read
I0/M = 0
S1S0 = 10

Interrupt Service Routine

A short pgm which tells the processor how to handle the interrupt.

Basic Machine Cycles.

Opcode fetch	(4T)
Memory Read	(3T)
Mem. Write	(3T)
I/O Read	(3T)
I/O write	(3T)

T state — one clock period

Status signals.

$S_1 S_0$

00 — opcode fetch

10 — Read

01 — Write

I0/M = 1 — I/O operation

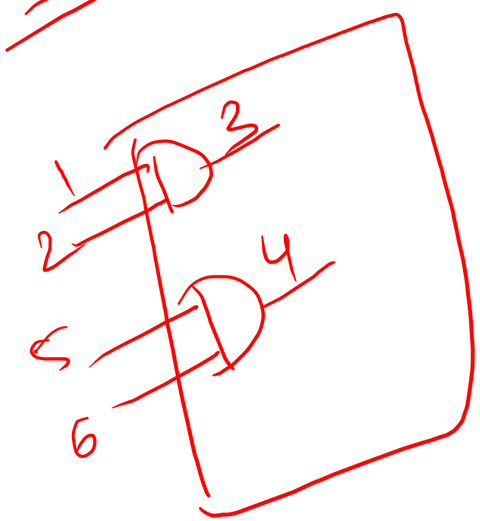
= 0 — Memory operation

Verilog -

multiplexer

decoder

assign



always

if - stmt

X assign X

case

stmts

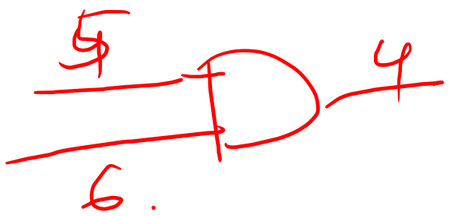
end .

&

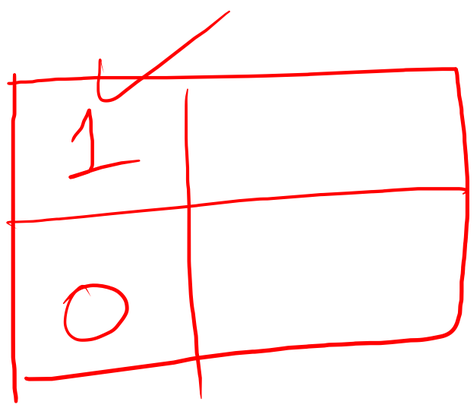
2 : 1 MUX

case (.o

if (sel = = 1)



199 .



AND gate

$0 \cdot 1 = 0$

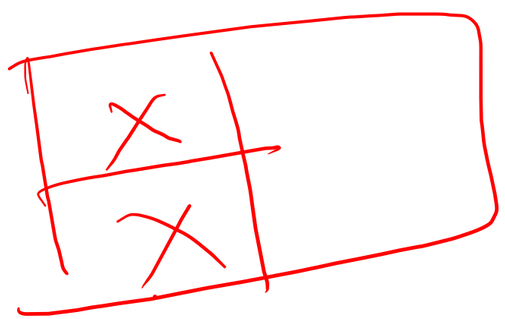
$0 \cdot 0 = 0$

$0 \cdot x = 0$

OR gate

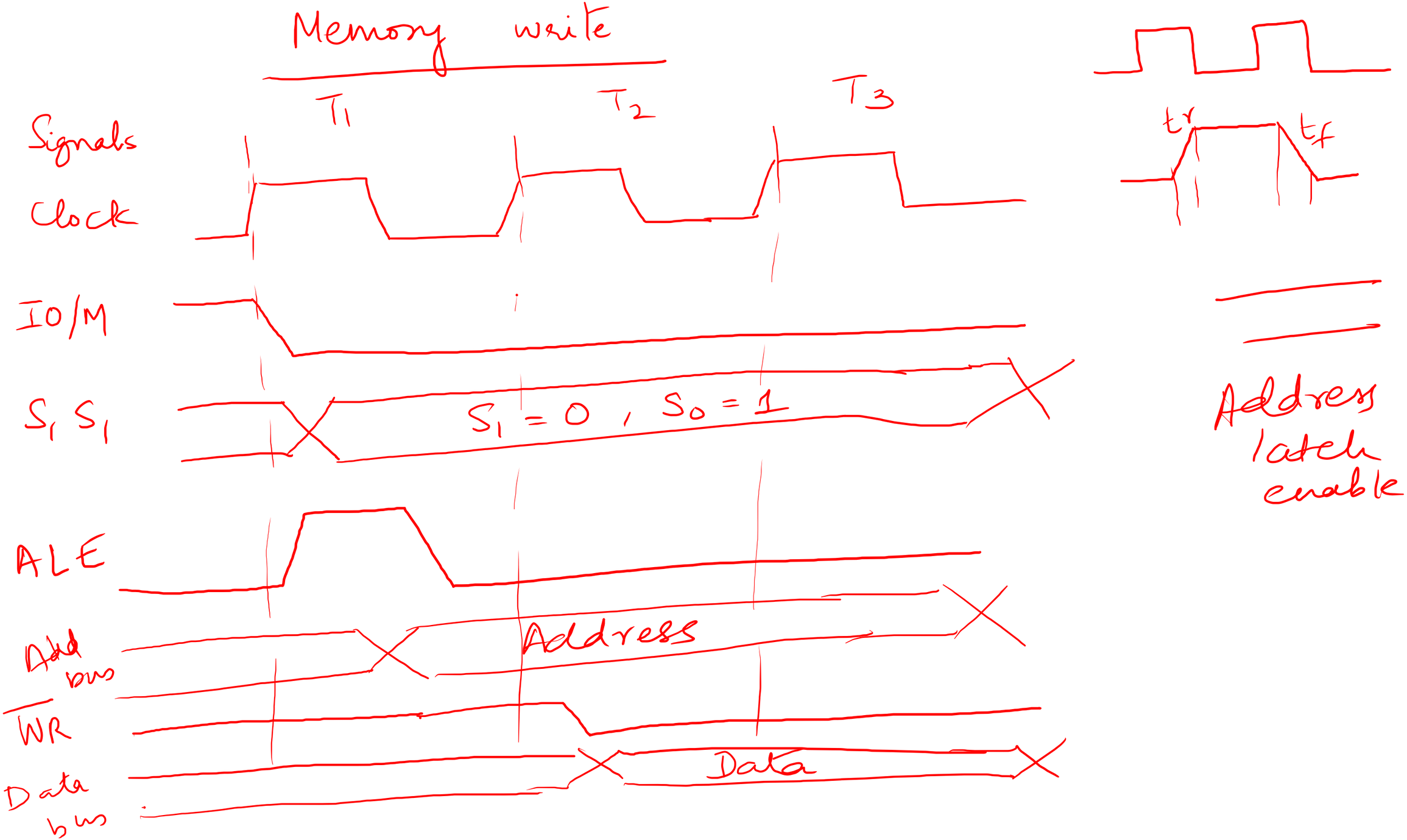
$1 + x = 1$

$0 + x = x$



$1 \cdot x = x$

Memory write



Address latch enable (ALE)