IC121: Digital Logic and Computer Organization

Group B

Practice Sheet 5

1. Implement the following set of equations using PROM, PLA and PAL:

$$X = AB'D + A'C' + BC + C'D'$$
$$Y = A'C' + AC + C'D'$$
$$Z = CD + A'C' + AB'D$$

2. Implement a full subtractor using PAL, PLA and PROM.

3. Expand the following function about the variable b.

$$F = ab'cde' + bc'd'e + a'cd'e + ac'de'$$

4. (a) Write the Boolean logic expressions that compares two 4-bit unsigned numbers A and B, and outputs three signals LT, GT and EQ.

   (b) Draw the bit-sliced design of a 4-bit unsigned comparator with outputs LT, GT and EQ.

   (c) How shall the Boolean logic expressions change or remain unaltered for LT, GT and EQ, if the same 4-bit comparator needs to handle 2's complement numbers.

5. Find the minimum and maximum number of select lines that you may have while realizing a 9:1 multiplexer.

6. Realize the Boolean expression $W \oplus X \oplus Y \oplus Z$ using a single 4:1 multiplexer, one XOR gate and one NOT gate. (*Hint: Use Shannon's expansion*)

7. (a) Design a combinatorial $MINMAX$ block that provides $min(P, Q)$ and $max(P, Q)$, where P and Q are user provided unsigned integers (assume a generalized width of N bit).

(b) Using only the $MINMAX$ blocks, design a combinatorial sorter that accepts 4 unsigned N-bit unsigned integers A, B, C, D as its input and provides sorted output H, J, K, L, where H is the highest (maximum) among the inputs and L is the lowest (minimum) of the inputs, J and K are the second largest and second smallest numbers respectively.

8. How do you realize the following structures with *minimum* hardware [Note that minimum could be zero as well]. Assume that X, M, N and R are 5 bit unsigned binary integers. [$int(R/4)$ is the integer part of the quotient after division by 4]

   (a) if (X *is odd*) then $Y = X - 1$ else $Y = X + 1$

   (b) if (X *is even*) then $X = X + 1$

   (c) if $(M > N)$ then $V = min(M, N)$ else $V = max(M, N)$

   (d) $P = 8 \times int(M/8)$

   (e) if (R *is divisible by* 4) then $S = int(R/4)$
   else $S = int(R/4) + 8 \times (R - 4 \times int(R/4))$

   (f) $S = (16 \times H) + 9$

   (g) if $(M = N)$ then $G = M$ else $G = N$

9. (a) Draw the structure of an array multiplier using half adders (HAs) and full adders (FAs) that is capable of multiplying a 6-bit unsigned binary number P with another 4-bit unsigned binary number Q.

   (b) Compute the area and delay of an $M \times N$ multiplier where M and N are the input bit-widths.

   (c) How will the area and delay estimates differ for an $N \times M$ multiplier?

   (d) Draw the structure of an array multiplier using half adders (HAs) and full adders (FAs) that is capable of multiplying a 6-bit number P with another 4-bit number Q, where P and Q are signed magnitude numbers. You may use logic gates if necessary.

10. (a) Design a combinational block as economically as possible, using only basic gates with maximum fan-in of 2, that realizes $Y = 2^N$, where N is a user provided 4-bit unsigned integer.

(b) Using the functional block computing $Y = 2^N$ (where N is a user provided 4-bit unsigned integer) as a blackbox, how do you compute $P = 2^{N+1}$, $Q = 2^{N-1}$ and $R = 2^N - 1$ most economically.

11. Implement a full adder with a decoder having active low enable outputs and NAND gates. The adder inputs are A, B, C and the outputs are S and C_o. Additionally, implement the same full adder using two 4:1 multiplexers.

12. Implement a full subtractor with a decoder having active low enable outputs and NAND gates. The subtractor inputs are A, B, C and the outputs are D and B_o. Additionally, implement the same full subtractor using two 4:1 multiplexers.

13. Implement a 2:1 multiplexer functionality using transistors following the CMOS logic style. How many transistors are required to implement the same? Assume that only inputs A, B and S are made available.

14. Implement a two-input XOR gate, a two-input XNOR gate and a half adder using transistors following the CMOS logic style. Comment on the number of transistors required for each of the implementations. Assume that only inputs A and B are made available.

15. Simplify the Boolean expression $F = (V + W + X)(V + X + Y)(V + Z)$ in a way such that it requires minimum number of transistors using CMOS style for realization. Show the realization as well.

16. Given that $f(a, b, c, d) = \Sigma_m(1, 3, 5, 7, 10, 11, 14, 15)$, realize $f(.)$ using the CMOS logic style.

17. Show the complete PMOS and NMOS transistor based realization of an active high and active low enabled tri-stated inverter. Explain the operation for each of the circuits in a few sentences and using a formal truth-table.

18. Find the minimized POS expression for $T(w, x, y, z) = \prod_M(0, 1, 8, 9, 13, 15)$. Represent this minimized POS expression using transistors following the CMOS logic style, assuming both complemented and uncomplemented variables are available as inputs. Comment on the number of transistors required.

19. Write the truth table of a 2-to-4-line decoder having an active low enable signal G. Construct a 5-to-32-line decoder with four 3-to-8-line decoders and a 2-to-4-line decoder, along with additional hardware if at all necessary, with each decoder unit having the active low enable signal.

20. Identify and design a circuit that accepts an 8-bit unsigned integer N and computes $\lfloor log_2 N \rfloor$. Assume that all zero input combination never occurs.

21. Implement a 3-to-8 active high enabled decoder using:

    (a) minimum number of 1-to-2 active high enabled decoders *ONLY*

    (b) one 1-to-2 active high enabled decoder and two 2-to-4 active high enabled decoders

22. If X and Y are the inputs and outputs respectively of a given functional block, express the first two least significant bits y_0 and y_1 of the output as a Boolean function of the input bits (x_0, x_1, etc.) for the following functional blocks:

    (a) Decrementer ($Y = X - 1$)

    (b) Divide by 4 ($Y = \lfloor X/4 \rfloor$)

    (c) Squarer ($Y = X^2$)

    (d) Remainder on division by 8 ($Y = X \ mod \ 8$)

    (e) Doubler ($Y = 2X$)

    (f) Ones' complementer

    (g) Two's complementer