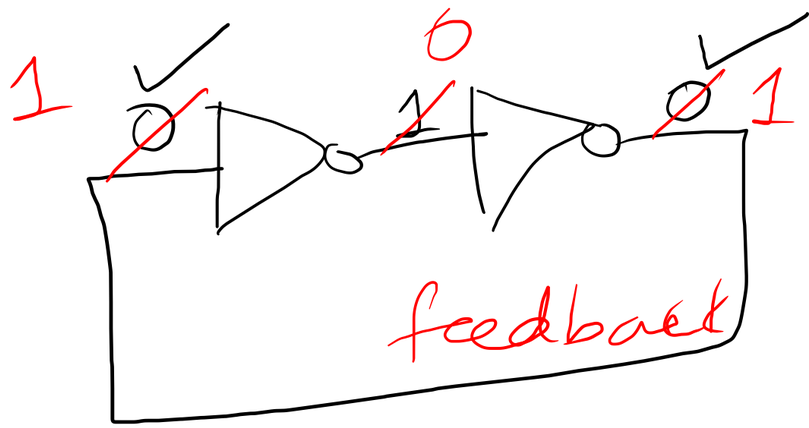
Latches

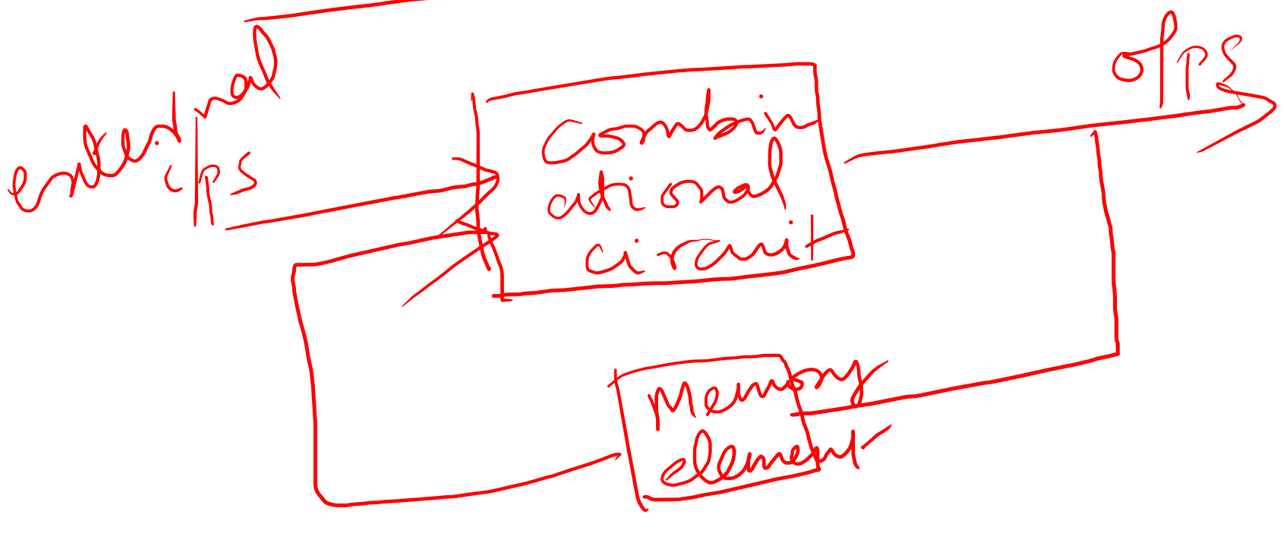
Sequential — memory

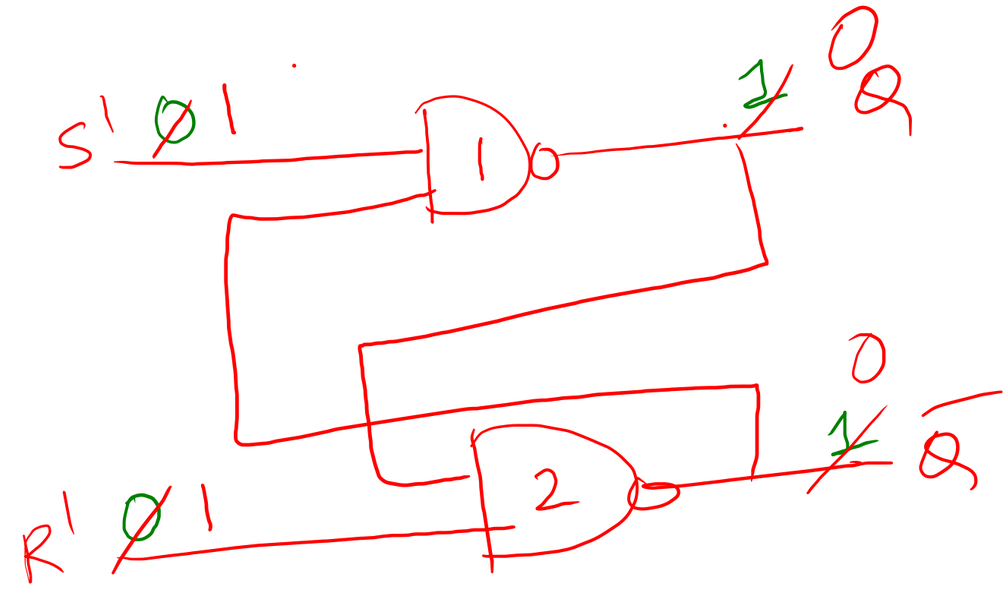


store 0 or 1

NAND / NOR

SR latch.





T	T	Q
S	R	
0	0	i
0	1	1
1	0	1
1	1	0

$S=0, R=1, Q=0, \bar{Q}=1$

$S=0, R=0, Q=0, \bar{Q}=1$

NC

$S=1, R=0, Q=1, \bar{Q}=0$

$S=0, R=0, Q=1, \bar{Q}=0$

NC

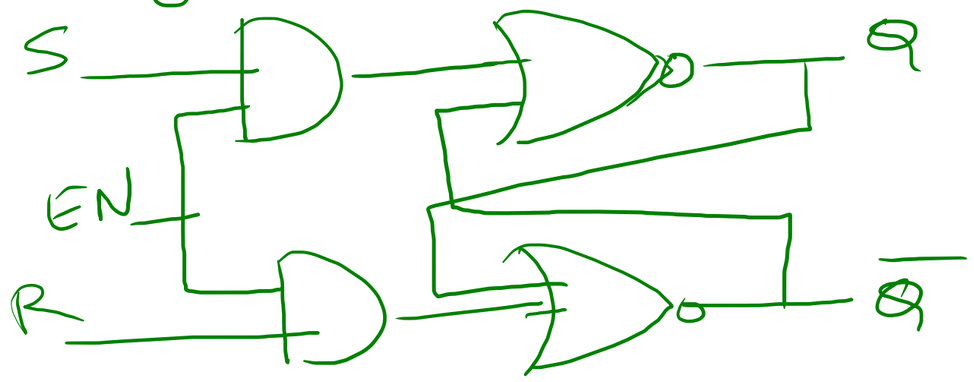
$S=1, R=1, Q=1, \bar{Q}=0$

$S=0, R=0, Q=0, \bar{Q}=1$

EN	S	R	Q	$\overline{Q}$
0	X	X	NC	NC
1	0	0	NC	NC
1	0	1	0	1
1	1	0	1	0
1	1	1	?	? invalid

State table

Gated SR latch



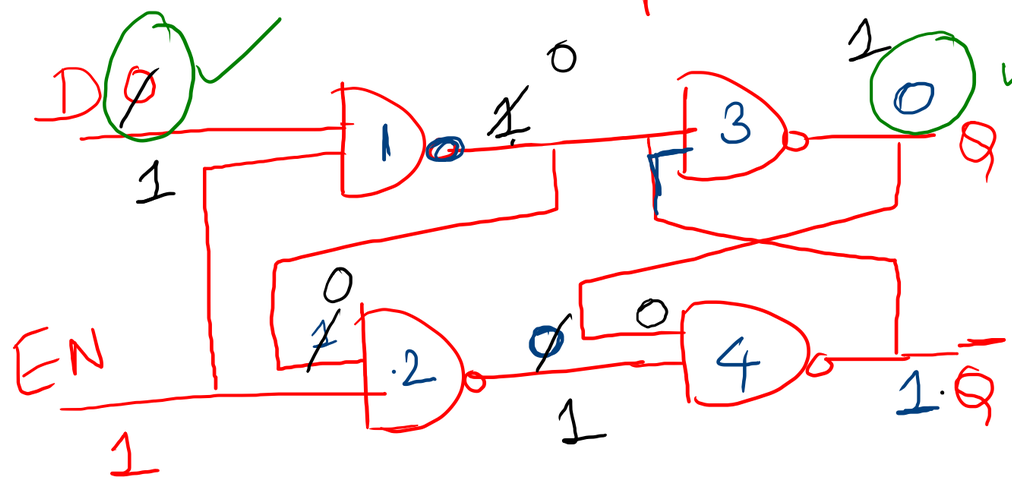
D latch.

1 i/p – D, 2 o/ps Q & $\overline{Q}$

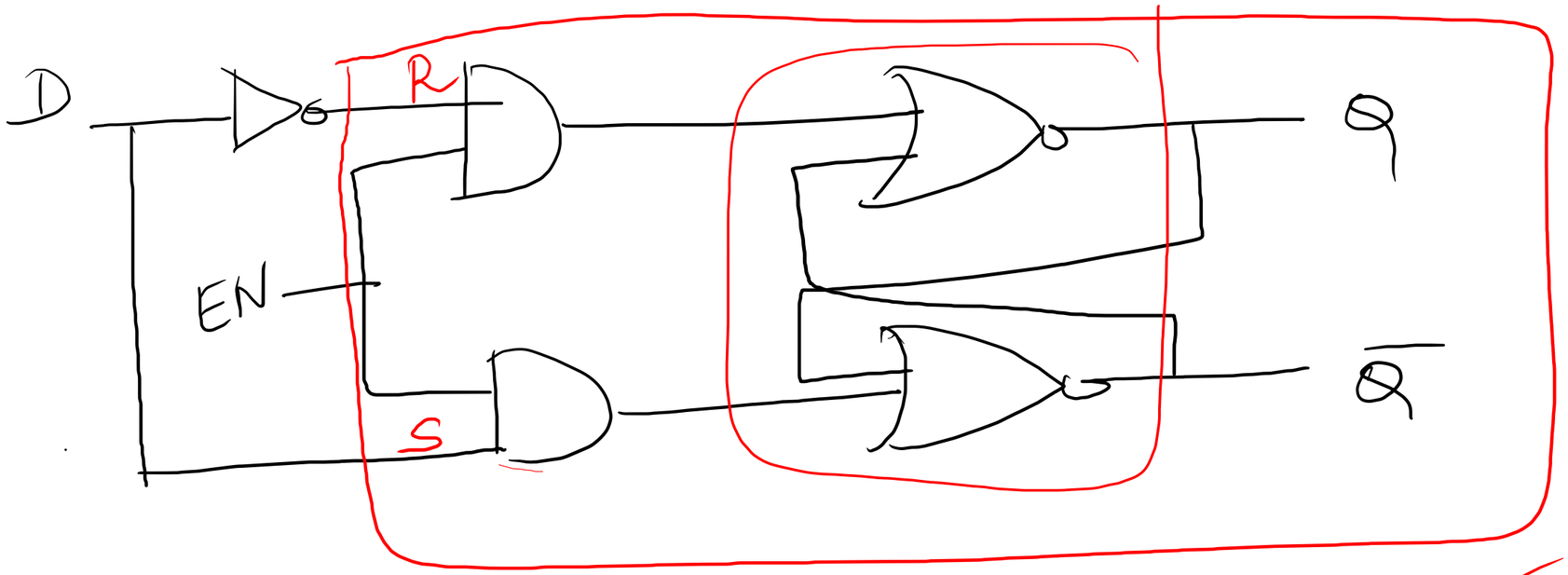
EN	D	Q	$\overline{Q}$
0	X	NC	NC
1	0	0	1
1	1	1	0

Gated D latch

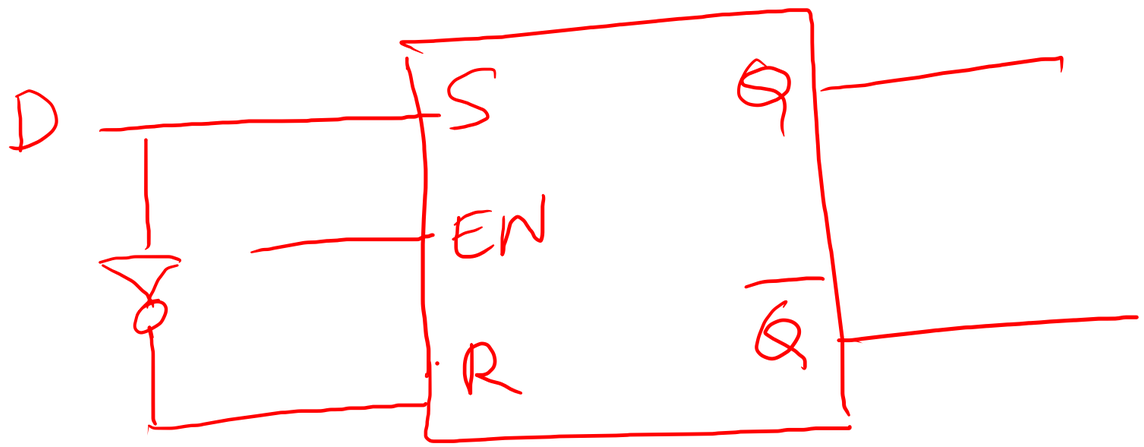
NAND implementation



NOR implementation of D latch

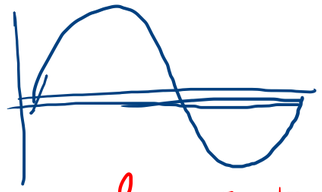


SR latch

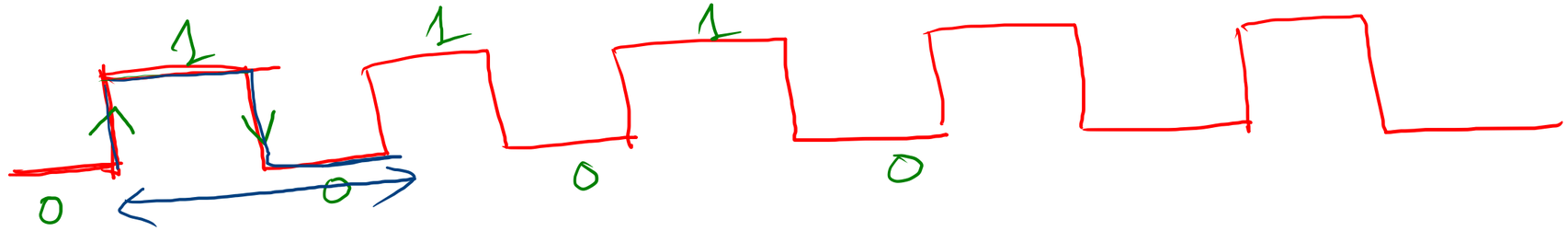


gated D latch using gated SR latch.

Clock



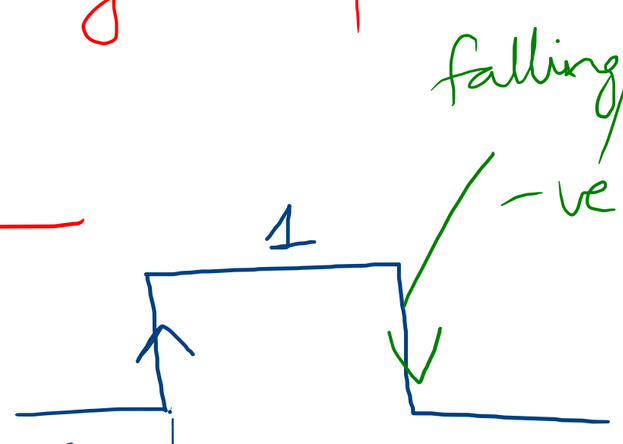
Periodic (Repetitive) train of rectangular pulses.



2 events

① sgl going from low to high

② sgl going from high to low



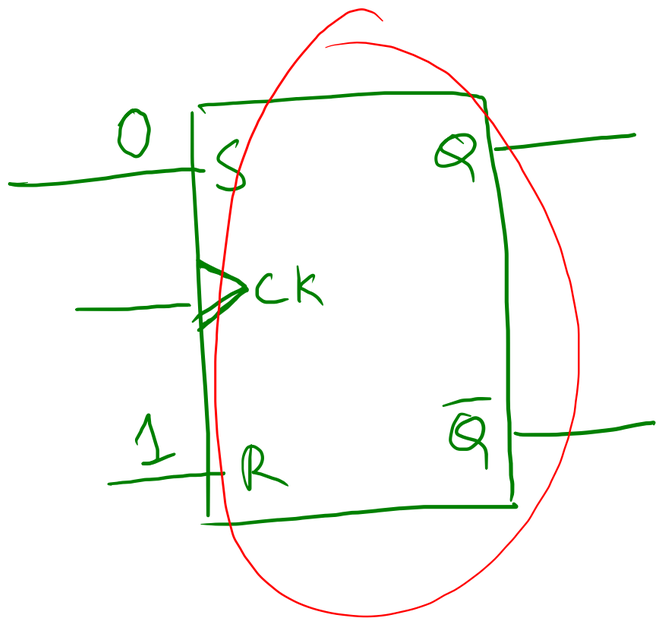
Flip flop

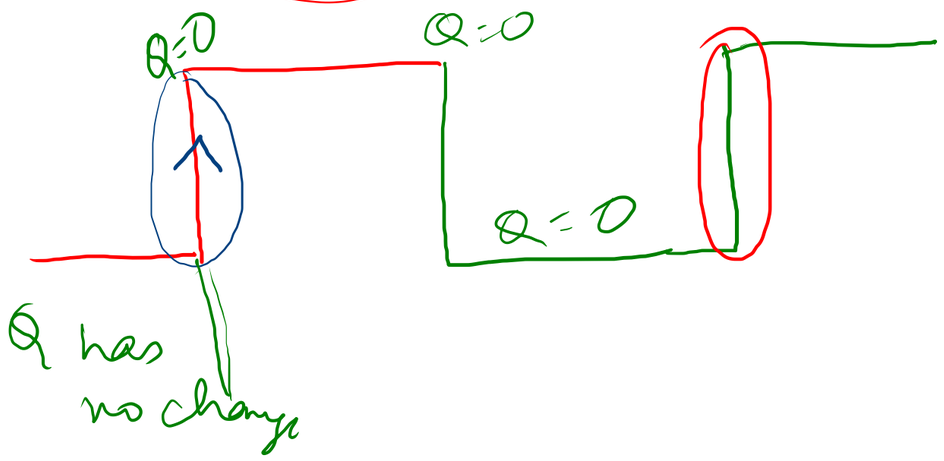
Inputs & a clock sgl

Flip flops are clock triggered → o/p will change only for a certain event on the clock pulse

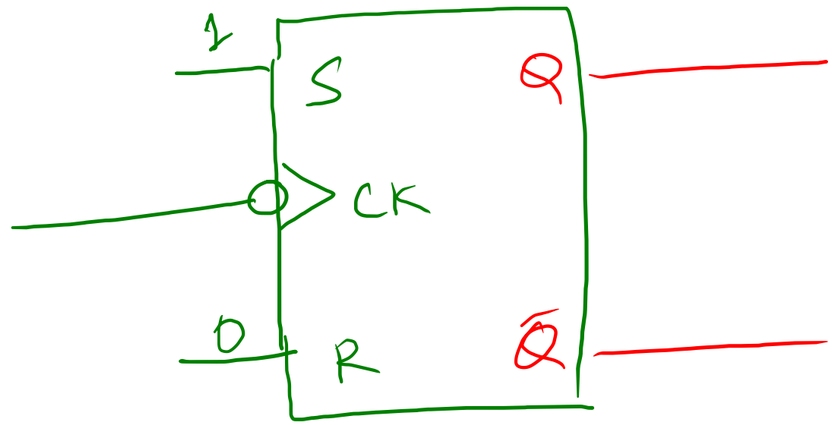
Sequential circuits can be +ve edge triggered or -ve edge triggered.

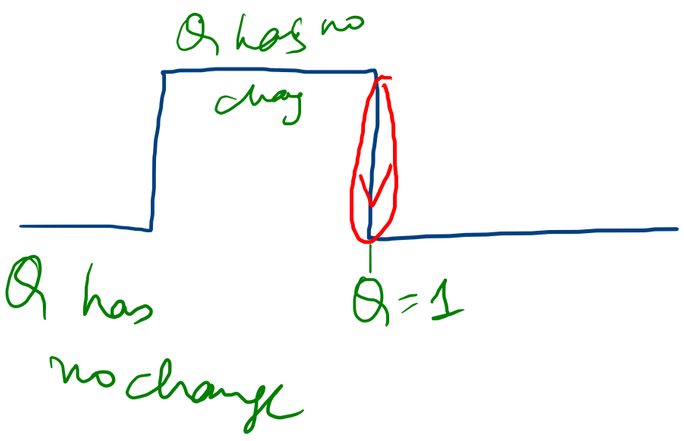
tve edge triggered SR ff.



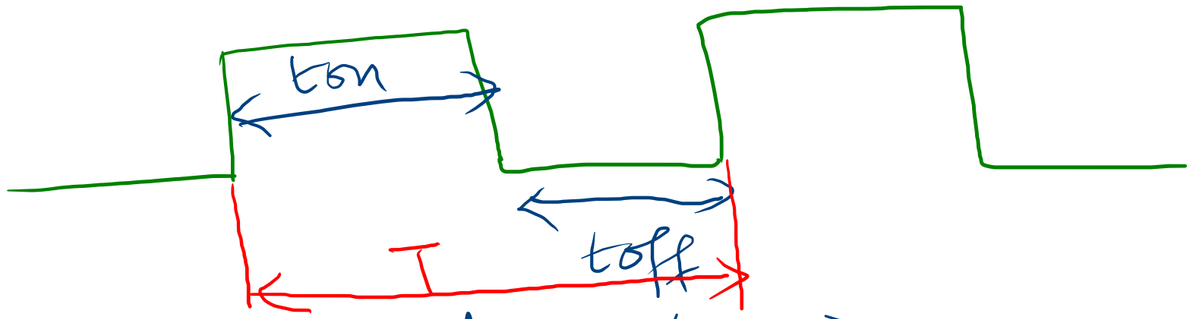


-ve edge triggered SR ff





A clock pulse



① on period (t_{on})

② off period (t_{off})

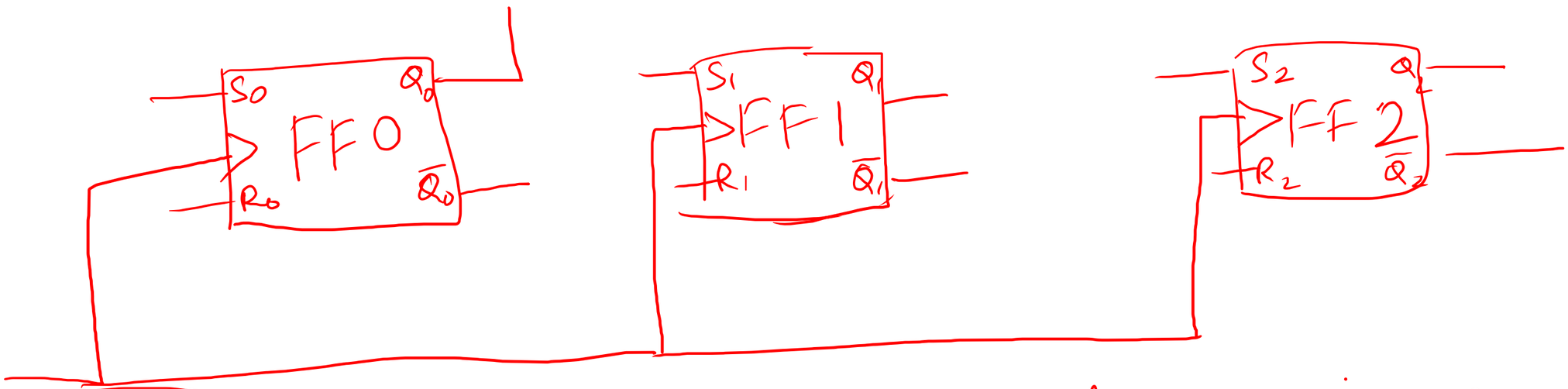
③ Time period (T)

$f = 1/T$

$T = 1\,ms$

$f = \frac{1}{10^{-3}} = 10^{3}\,Hz$

$= 1\,kHz$



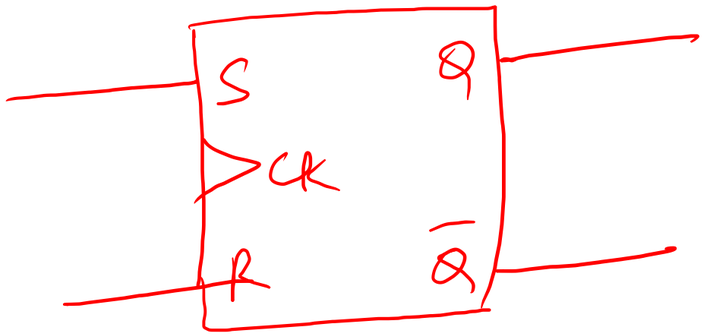
Clock generated

master clock

Synchronization in sequential circuits is possible using clock.

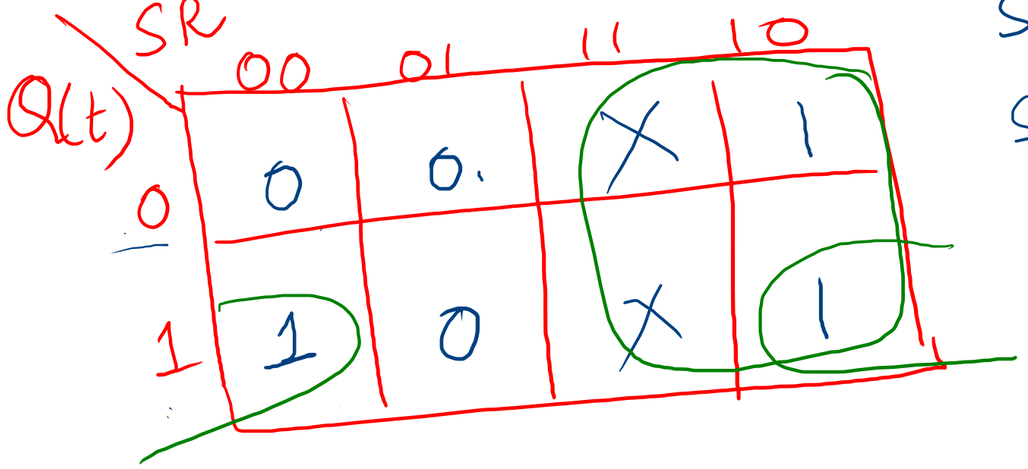
Synchronous circuits

Positive Edge triggered SR ff.



State table

CK	S	R	Q	$\bar{Q}$
0/1	x	x	NC	NC
↑	0	0	NC	NC
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	?	?



S=0, R=0

S=0, R=1

Q = 0

S=1, R=0

Q = 1

$Q_{(t+1)} = Q_{(t)}\bar{R} + S$ → Characteristic equation for SR ff

$R \cdot S = 0$

previous present state Q(t) – ~~present~~ state

present ~~next~~ state Q(t+1) –

Excitation table for SR ff

Circuit changes		Required value	
From $Q(t)$	To $Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$S = 0, R = 1$

$S = 0, R = 0$

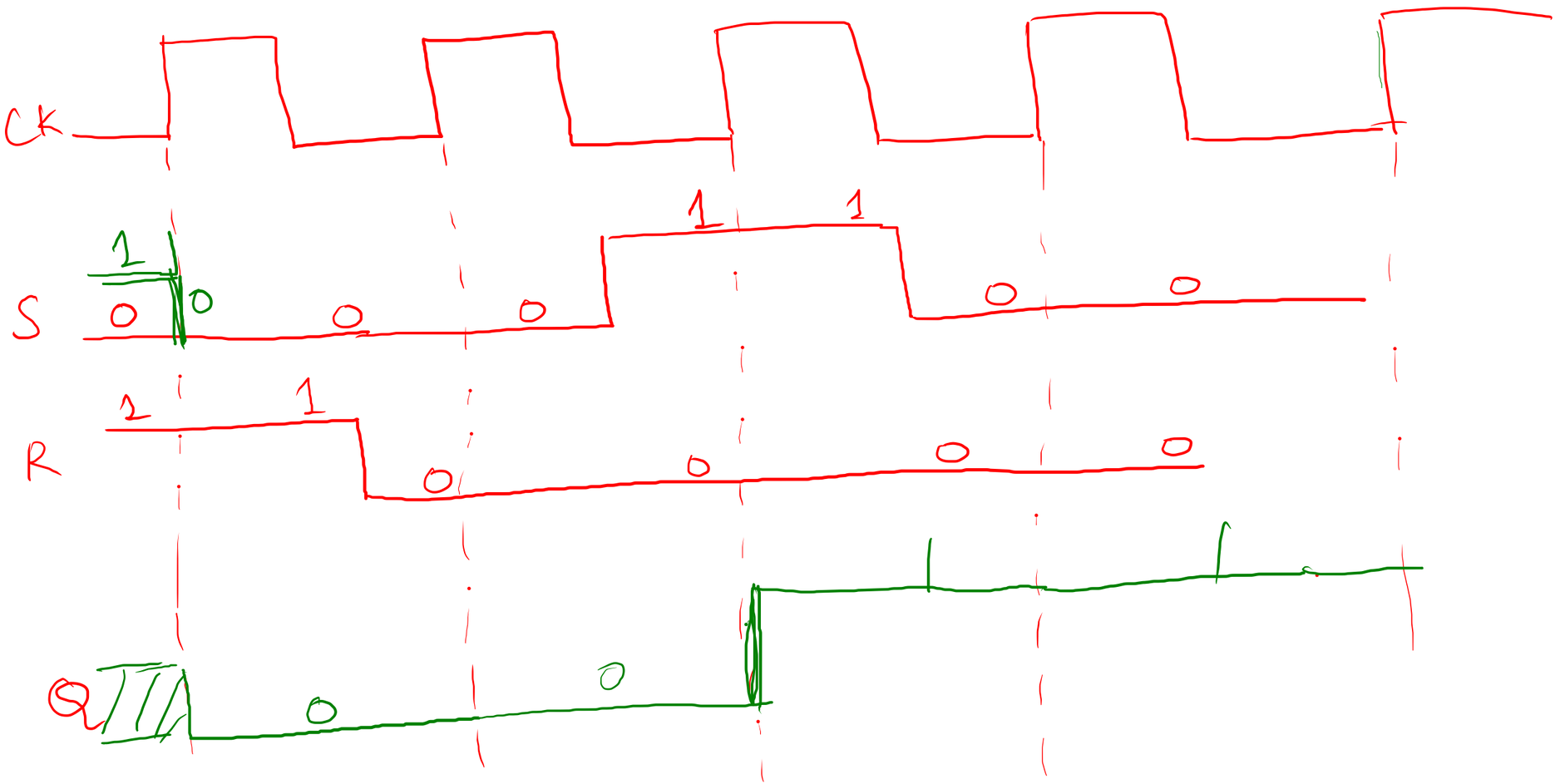
$S = 1, R = 0$

$S = 0, R = 1$

$S = 1, R = 0$

$S = 0, R = 0$

Timing diagram for SR ff. (+ve edge triggered)



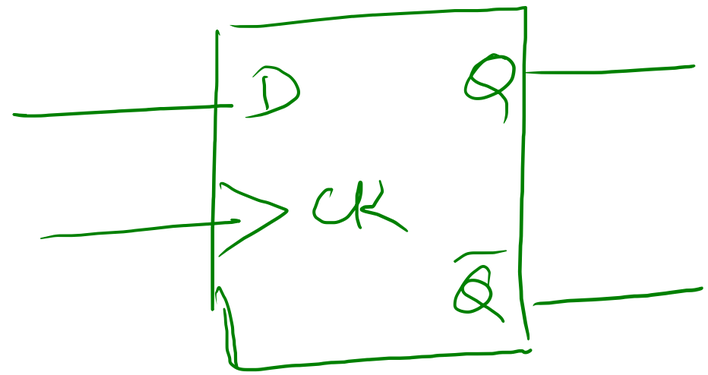
Edge triggered D ff.

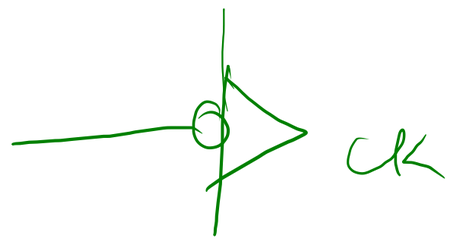
State diagram.

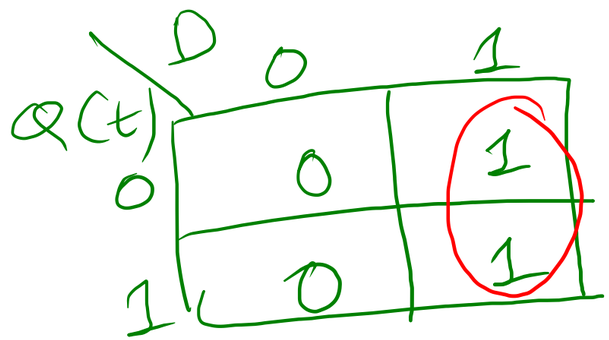
Ck	D	Q	$\overline{Q}$
0/1	X	NC	NC
↑	0	0	1
↑	1	1	0

Characteristic equation

$Q_{(t+1)} = D$







Timing Diagram for -ve edge triggered D ff