

Opcode fetch

Instruction decode

Execute

2 cycles

Fetch cycle

Execute cycle

e.g. The instruction code 0100 1111 ($4F_H$) is stored in memory location 2005_H .

- ① Program counter places the address 2005_H on the address bus.
- ② Control unit sends Memory Read (\overline{MEMR}) signal to enable the op buffer of the memory.

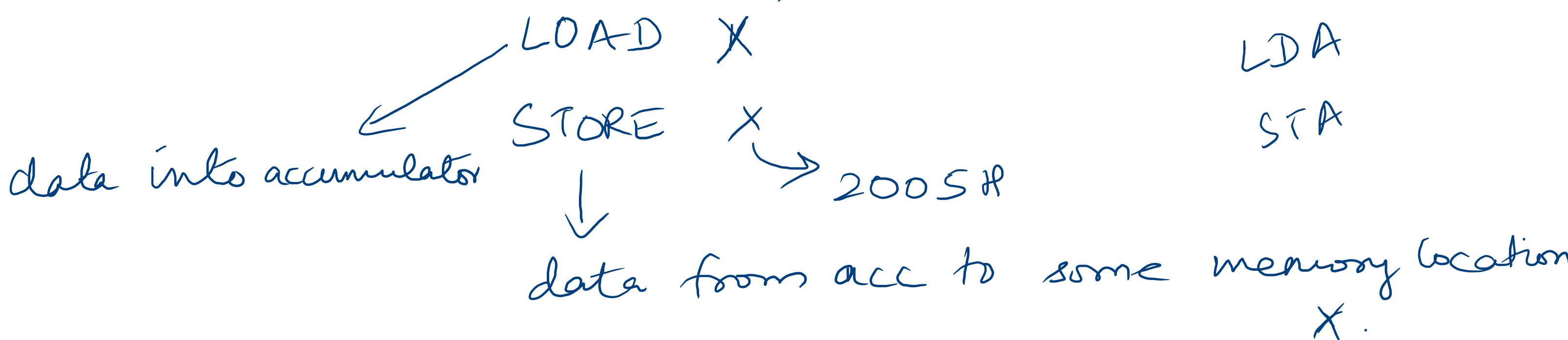
③ The instruction $4F_H$ stored in memory location 2005_H is placed on the data bus & copied to the instruction register (IR) .

④ Instruction will be decoded & executed accordingly

}

Diff types of instructions

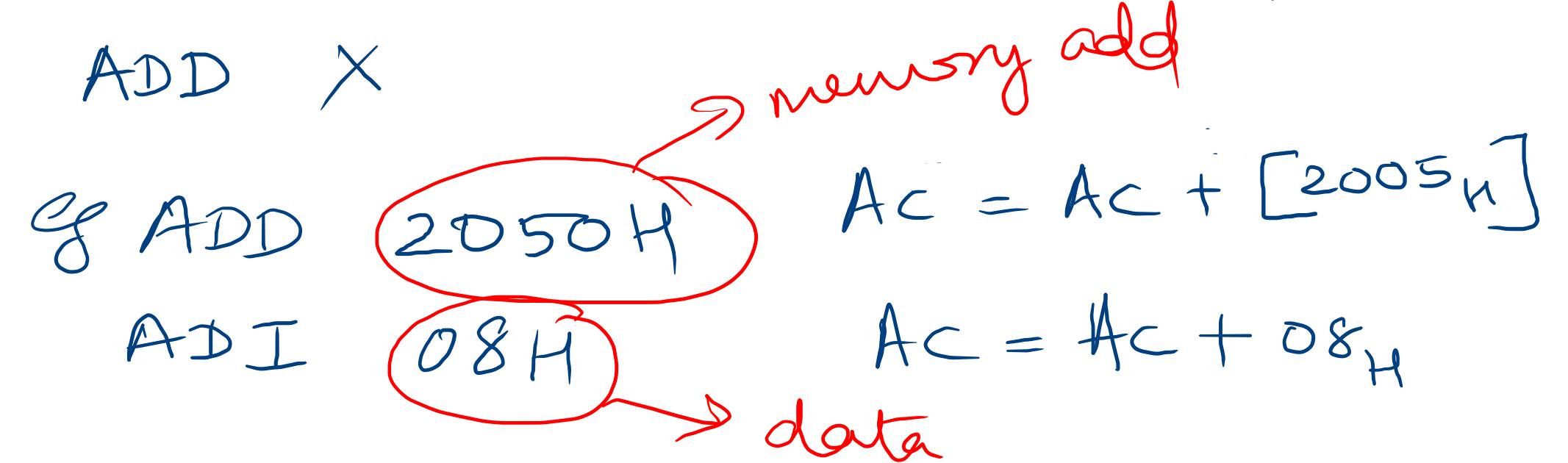
① Data Transfer



② Arithmetic operation

SUB

MUL



③ Logical instruction

AND X
OR X → X - memory location
 $Acc = Acc \& [X]$

④ Program Control instructions

Jump
JZ memory location
JC Jump on Zero
Jump on carry

⑤ I/O instructions

IN Port A
OUT Port B

Bus.

A set of physical wires that connect components.

Dedicated bus — single source & single destination

Shared bus — multiple sources & destinations.

If a reg is 16 bit long, it can be connected to the bus if the bus has the same width (16 bits)

Address bus — unidirectional

Data bus — bidirectional

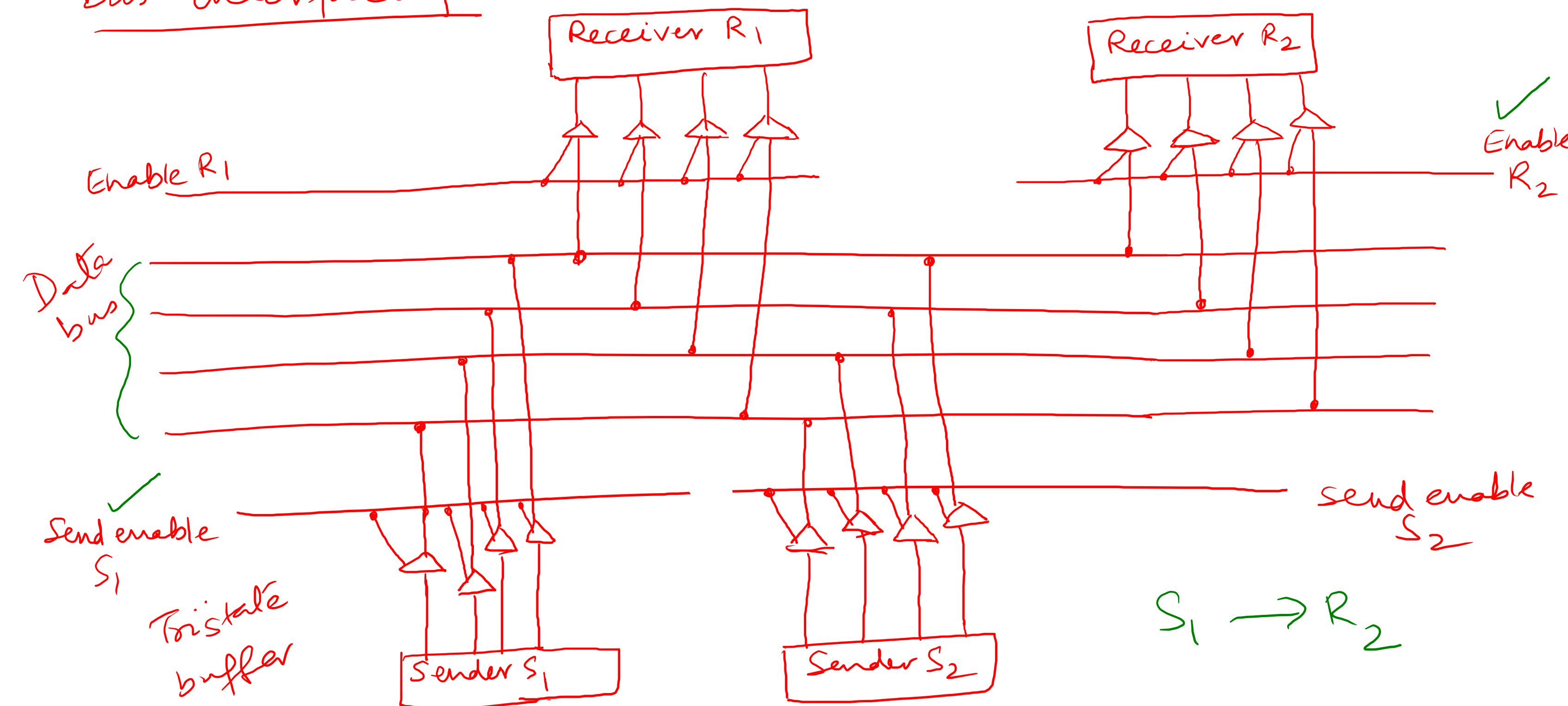
→ multiplexed ✓

(16 bits) → dedicated

(8 bit) → $A_0 - A_{15}$

→ $AD_0 - AD_7$

Bus interfacing



Main memory



(Address)

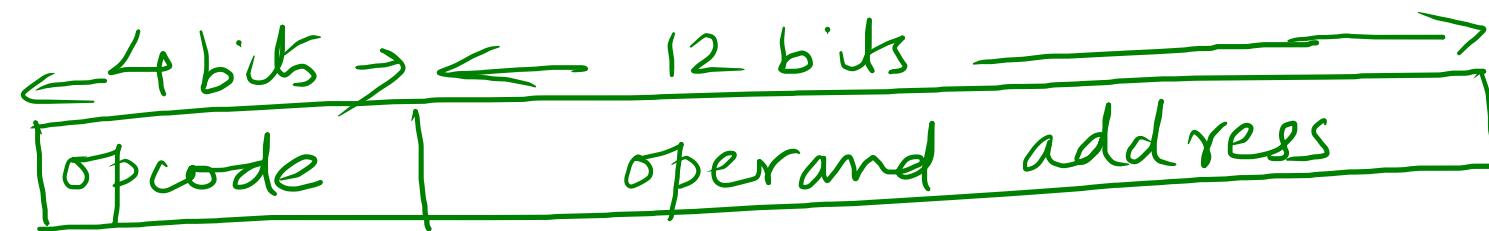
0
1
2
3

n - 3
n - 2
n - 1

Memory is segmented
Instruction segment
Data segment
Stack segment

Instruction

Format of an instruction in the memory



Memory word is 16 bit long.

ADD

2005H

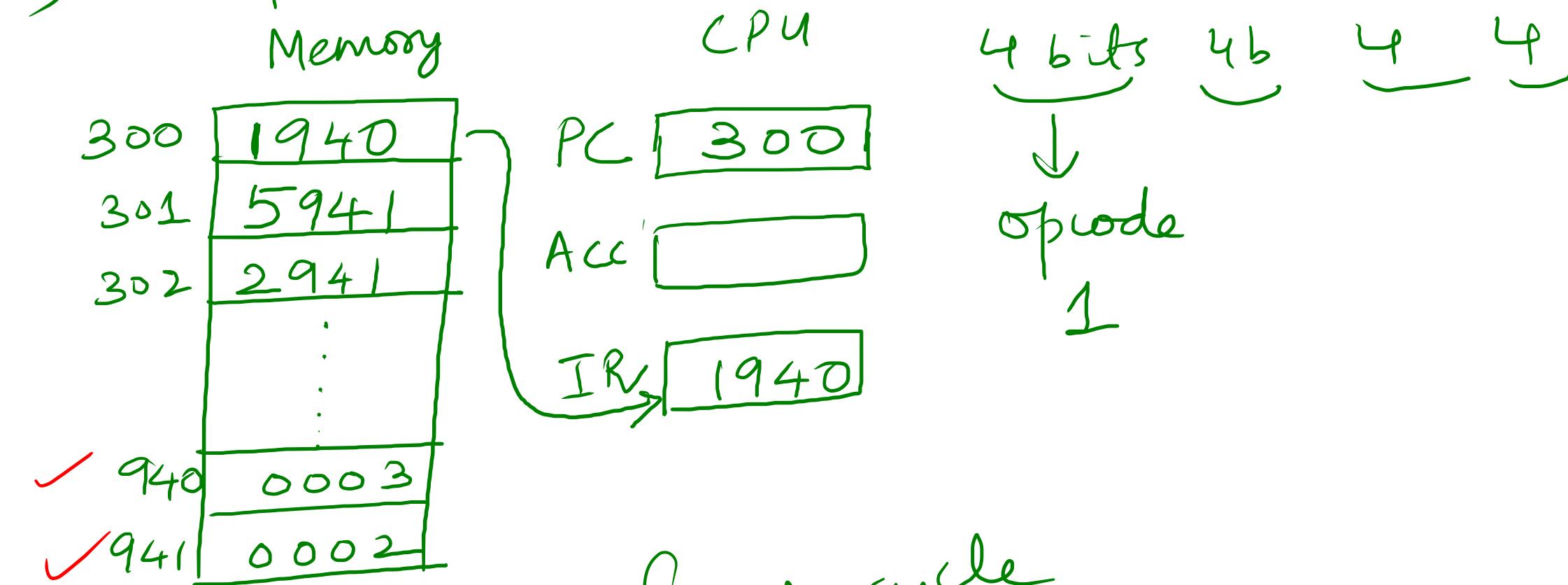
↓
eg 01 - opcode

Add the contents of memory location 940 with contents of memory location 941 and store the result in 941. (opcode 1) Step 1 16 bit.

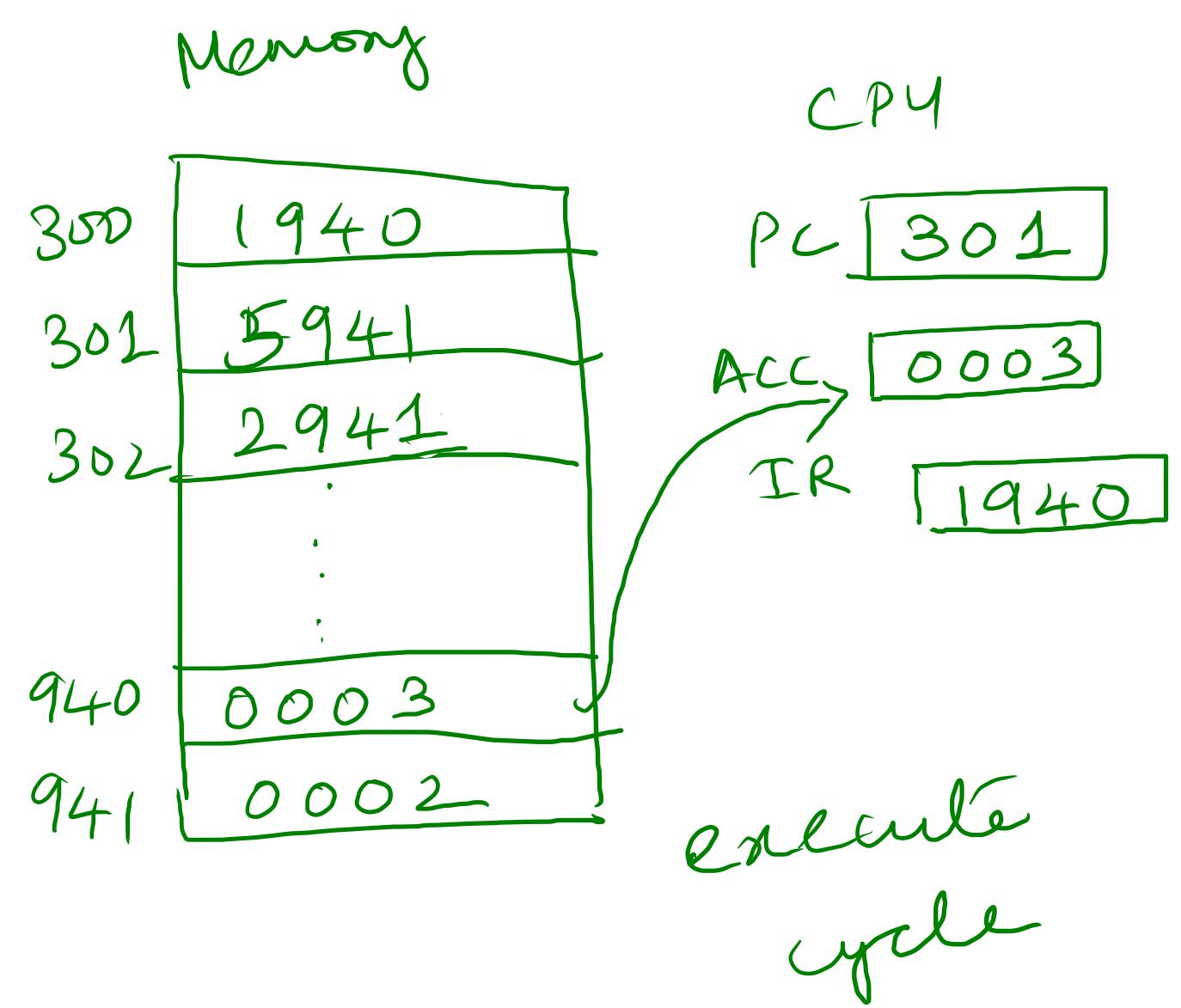
LOAD 940

ADD 941 (5)

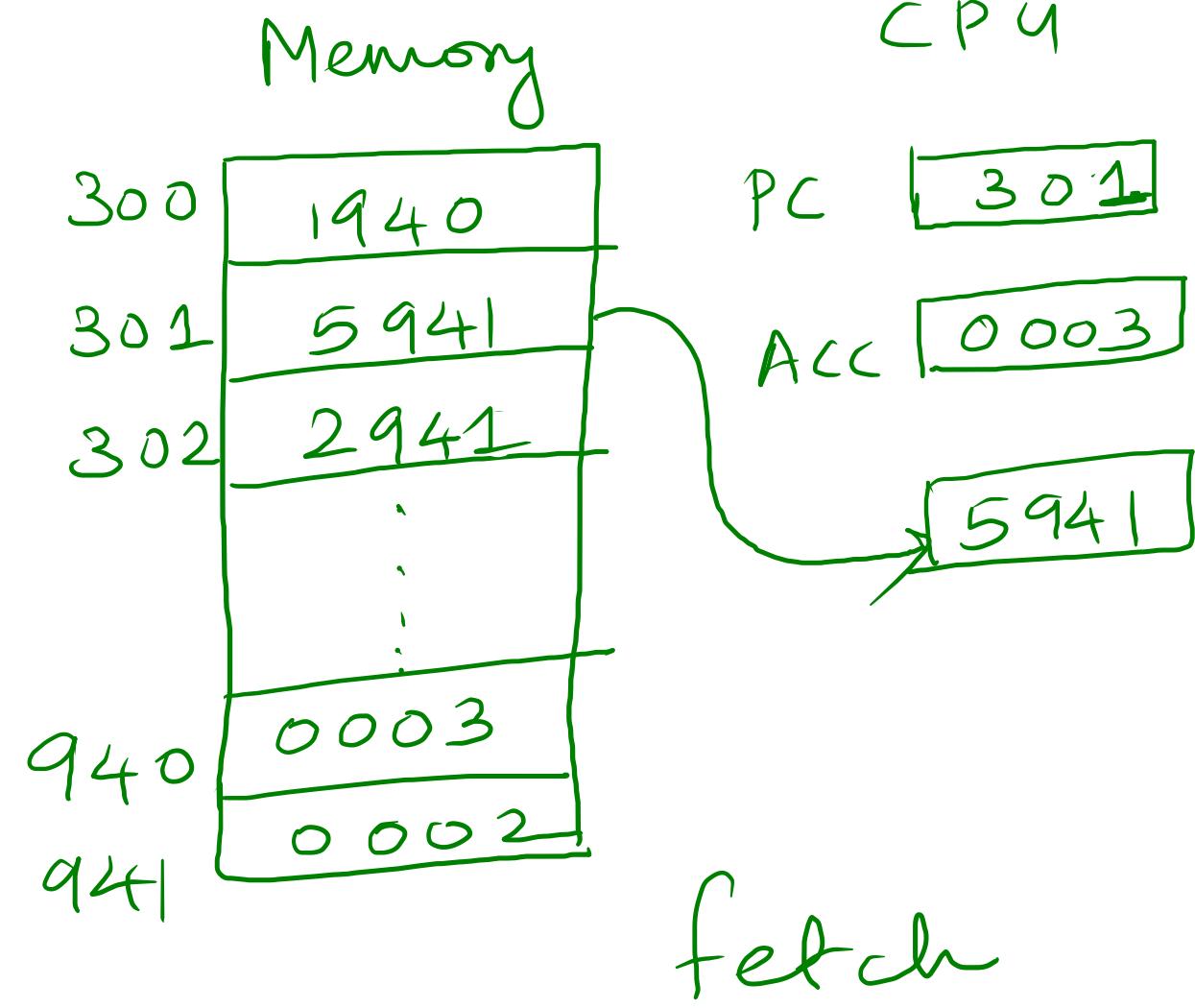
STORE 941 (2)



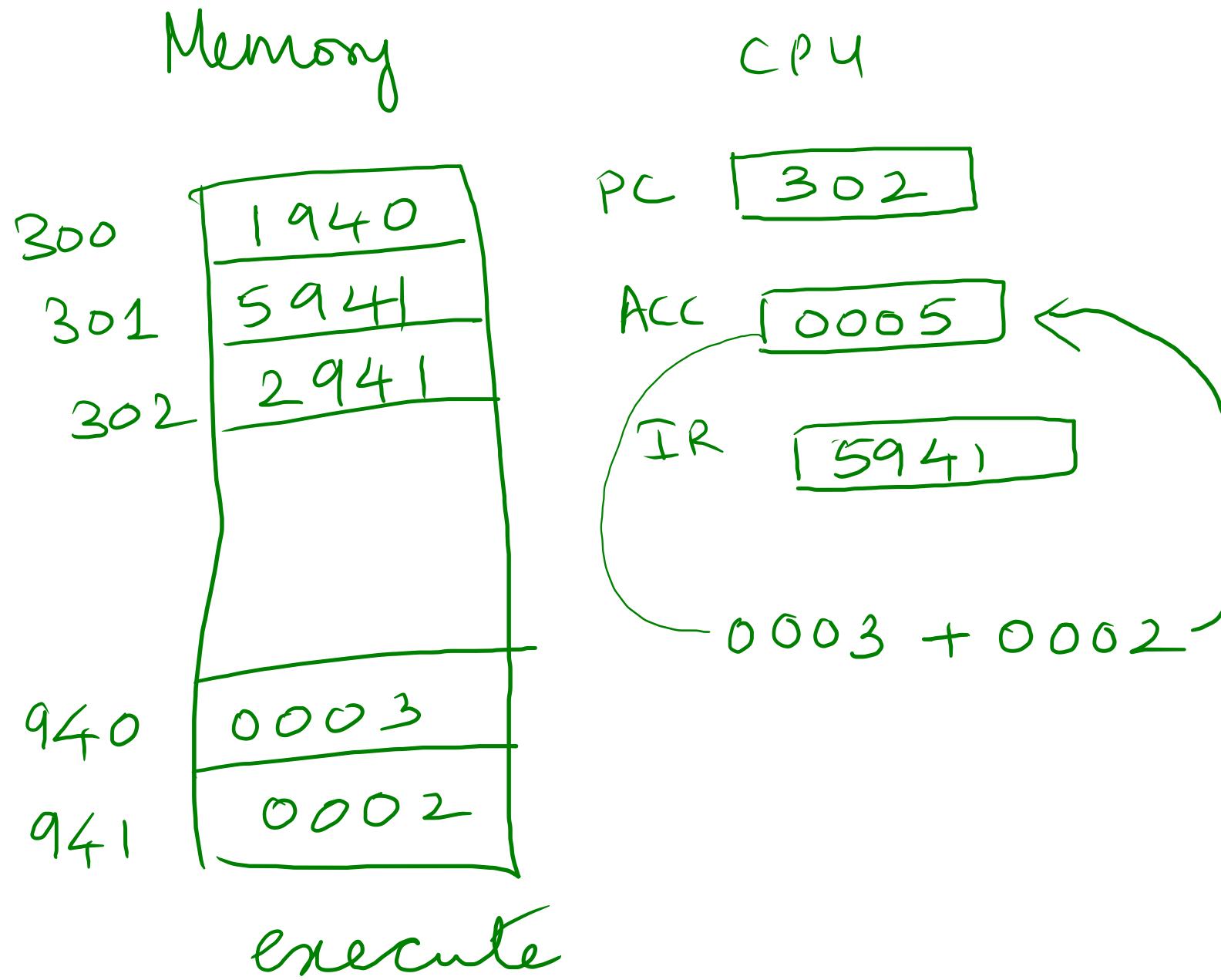
Step 2



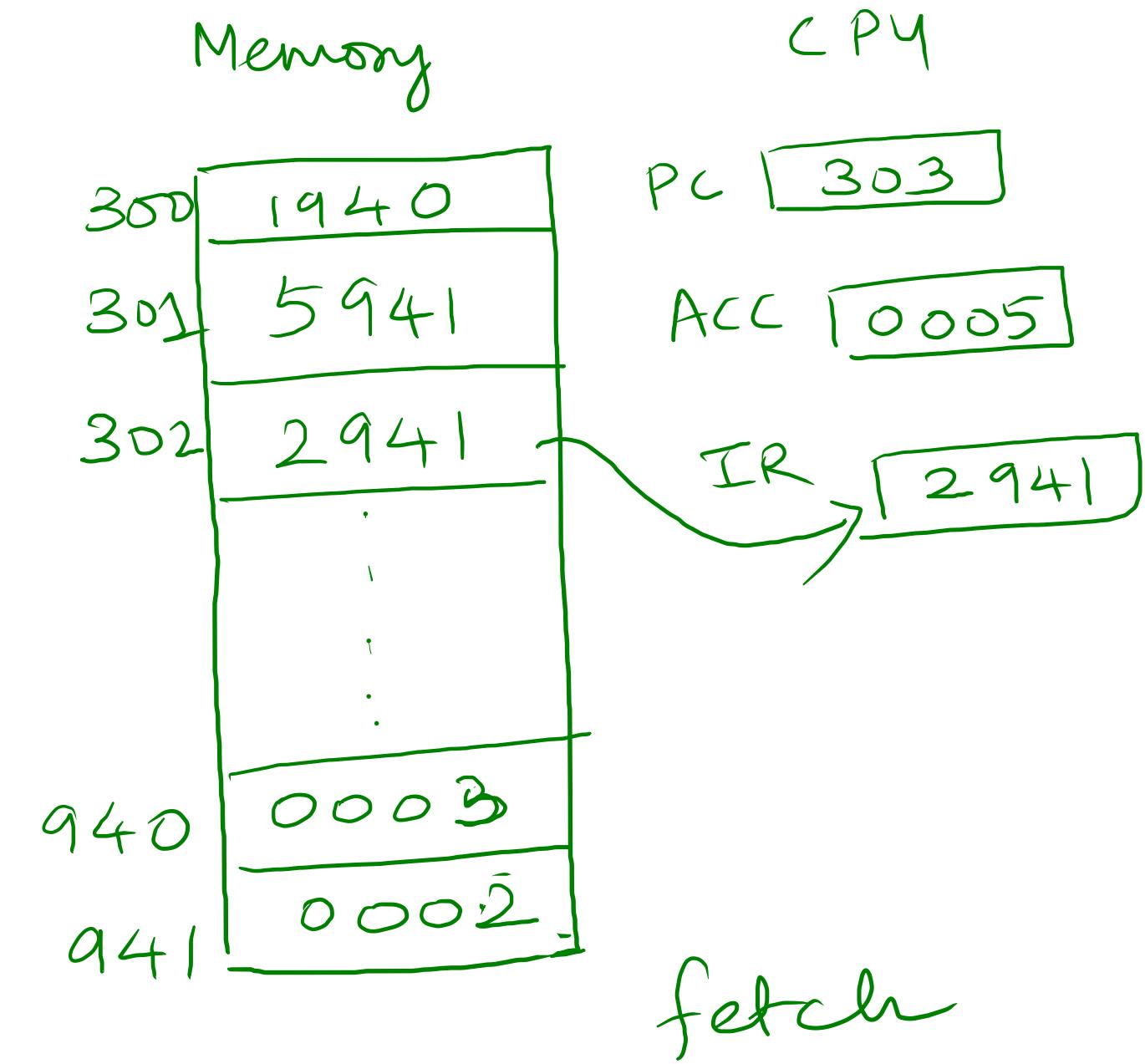
Step 3



Step 4



Step 5



Step 6

