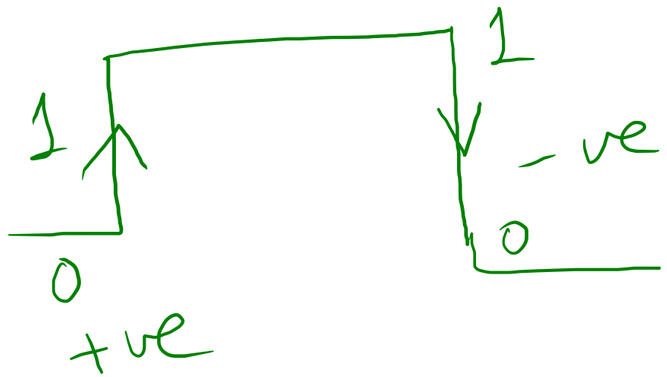
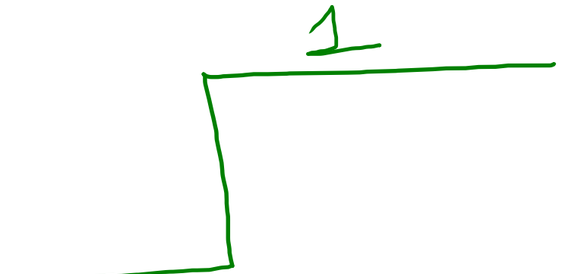
Edge triggered

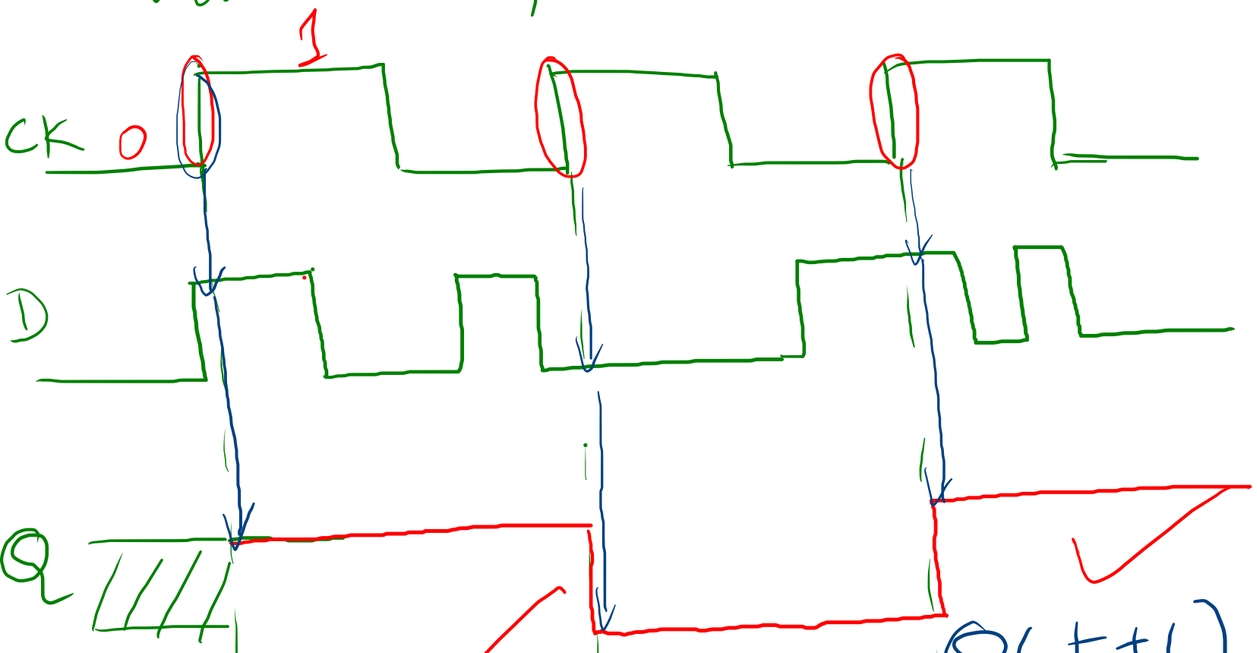


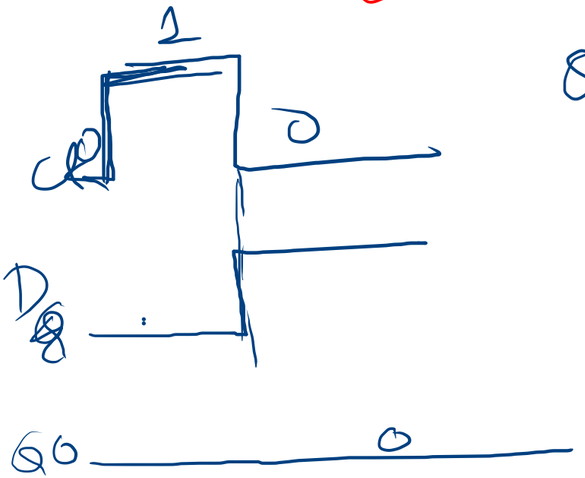
latch

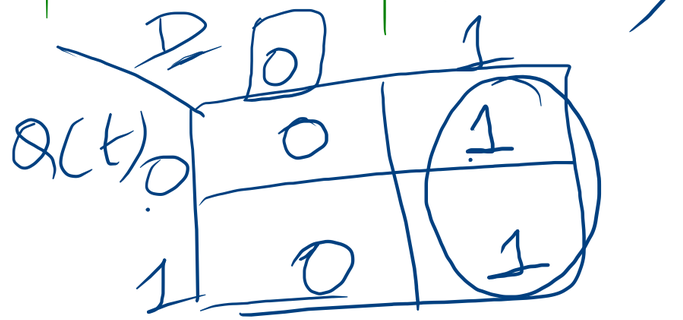
level sensetive



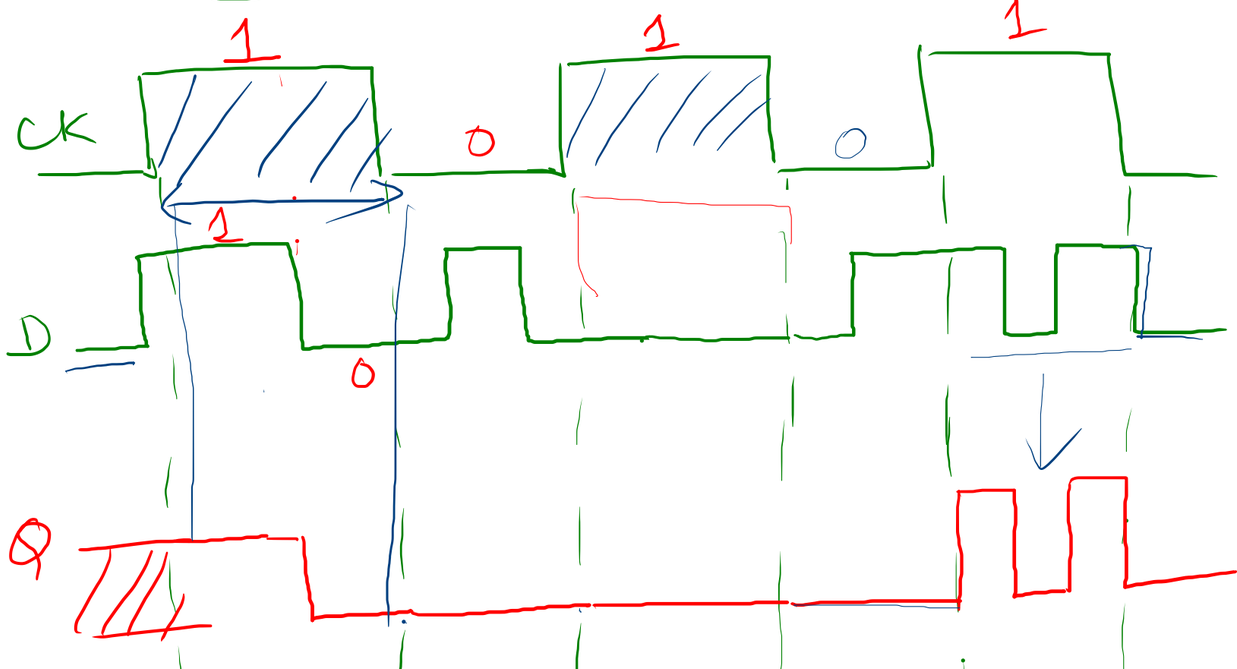
+ve edge triggered D ff







D latch



D ff

CK	D	Q	$\bar{Q}$
↑	0	0	1
↑	1	1 ✓	0

SR latch

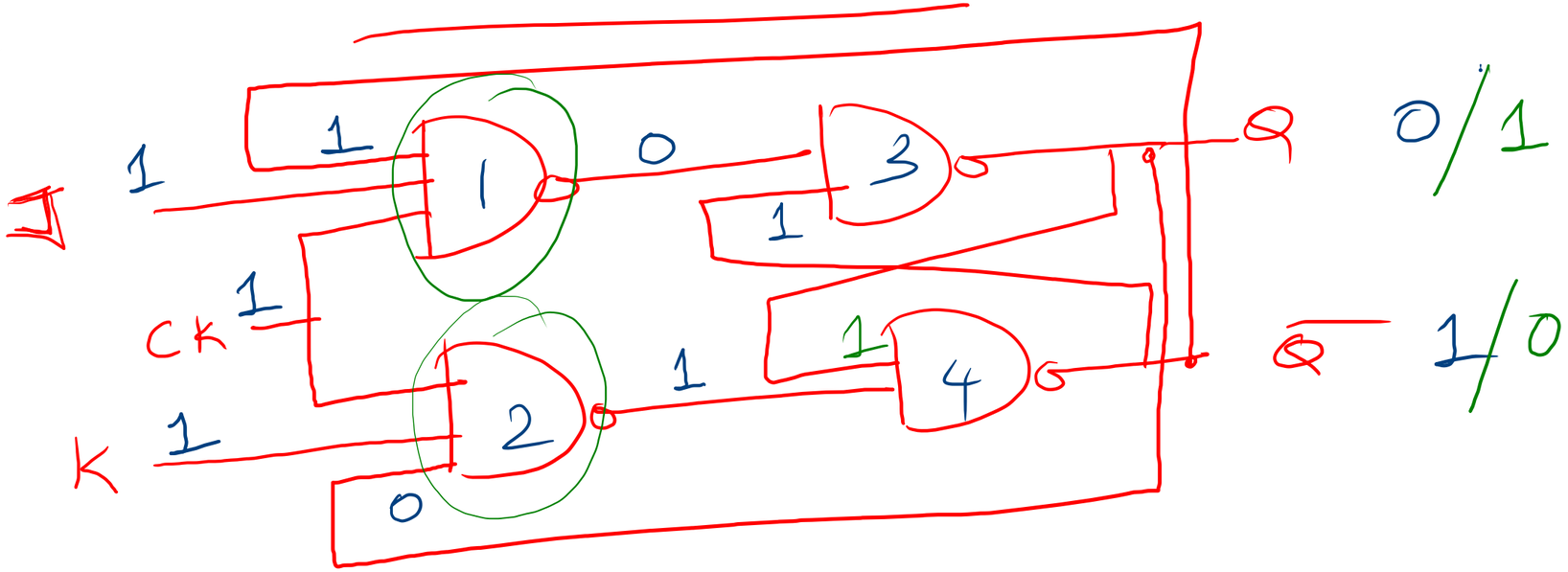
invalid

We introduce a feedback

Assume $Q = 0$, $\bar{Q} = 1$

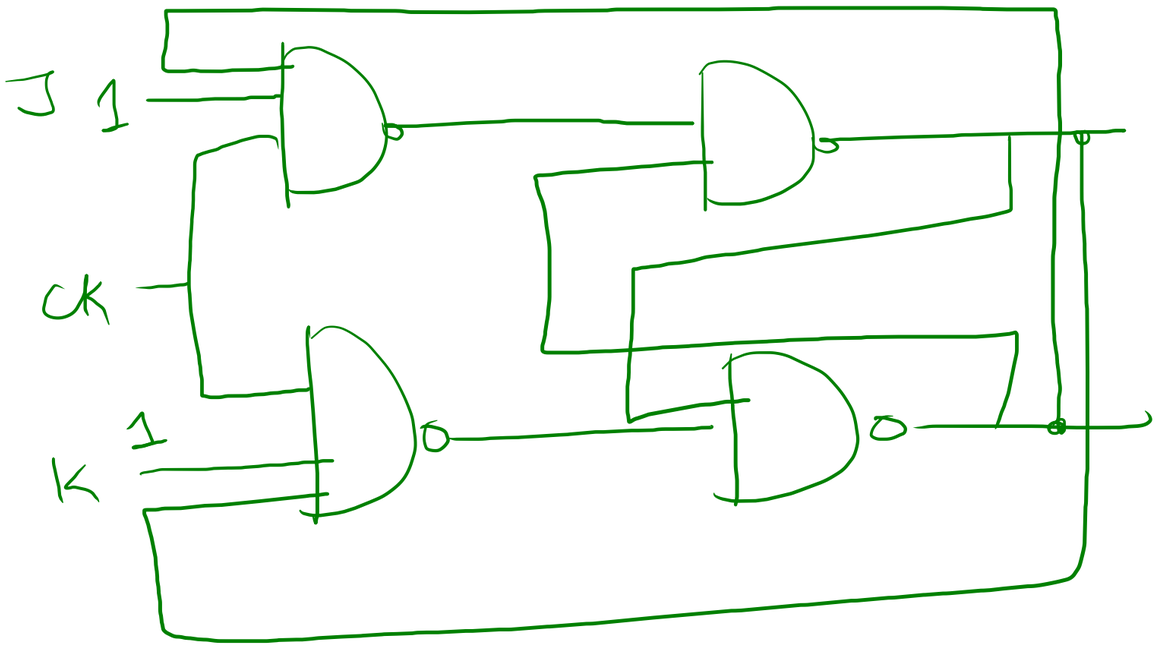
$J = 0$, $Q = 0$
$\bar{Q} = 1$
$K = 1$

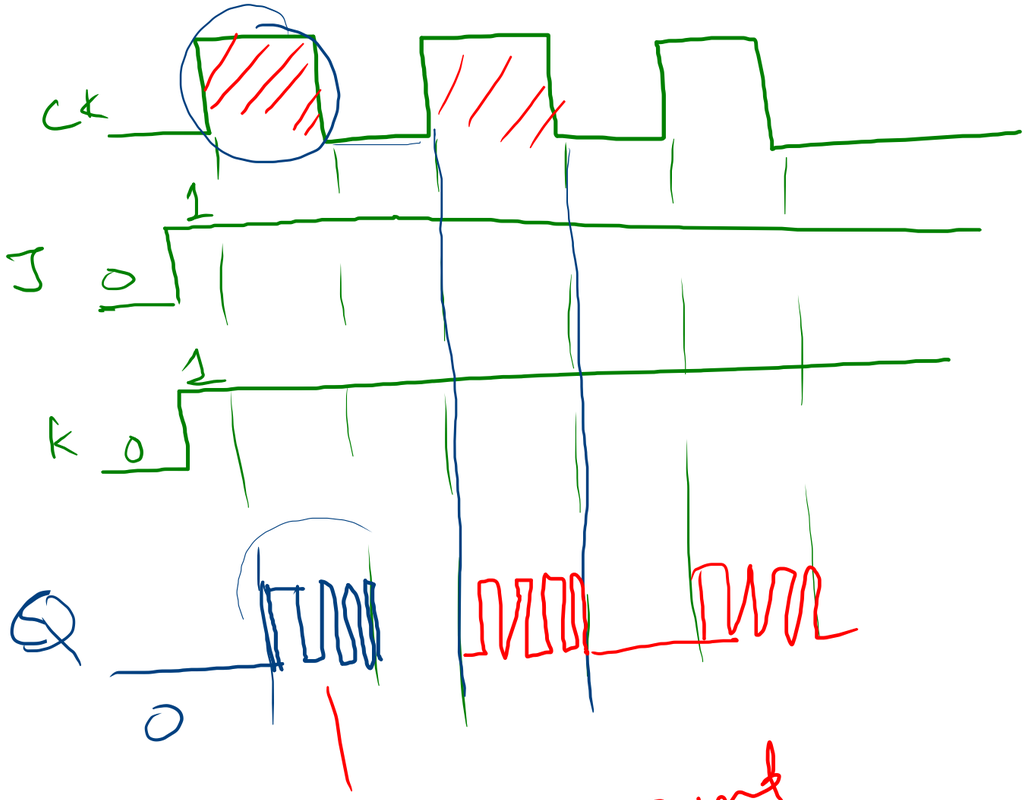
JK latch



S	R	Q	$\bar{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	~~1~~	~~1~~

1 1 $\bar{Q}$ Q



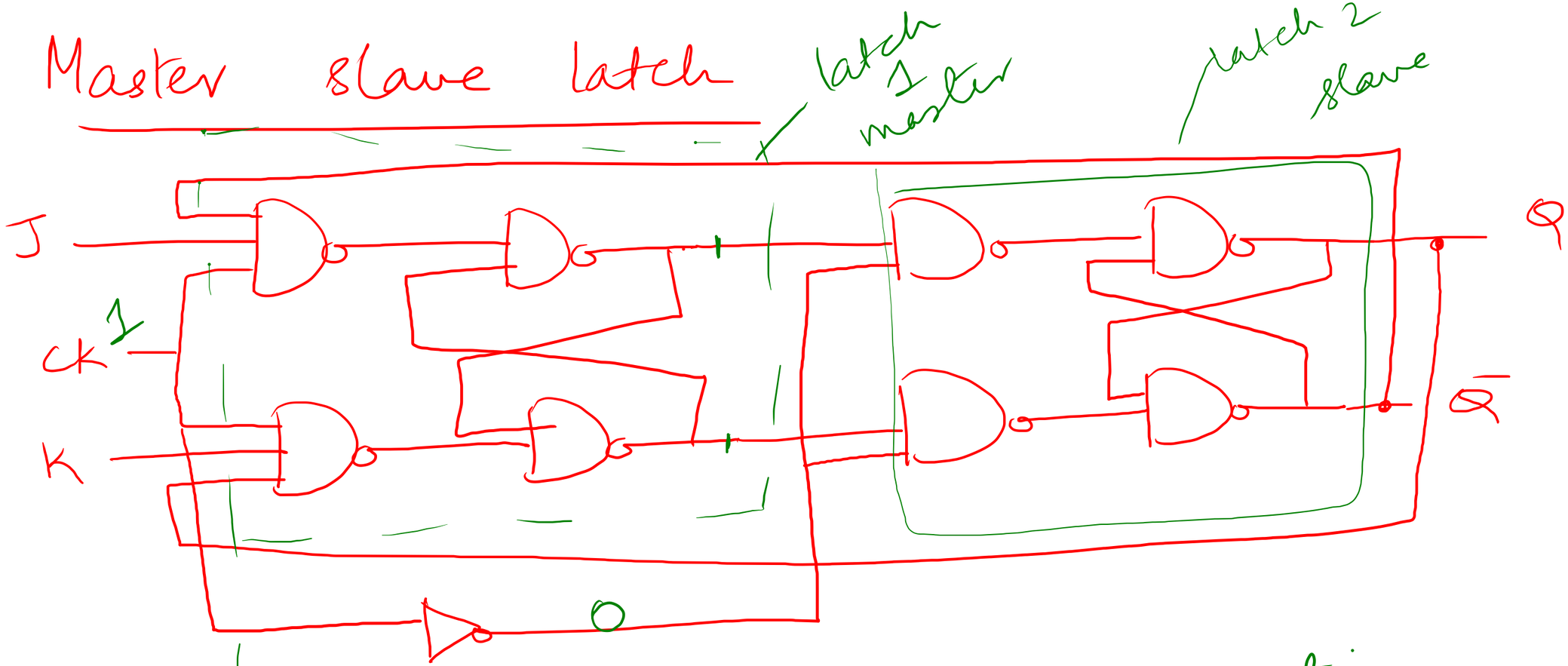


$Q_t = 0$, $Q_{t+1} = 1$

When $J = K = 1$

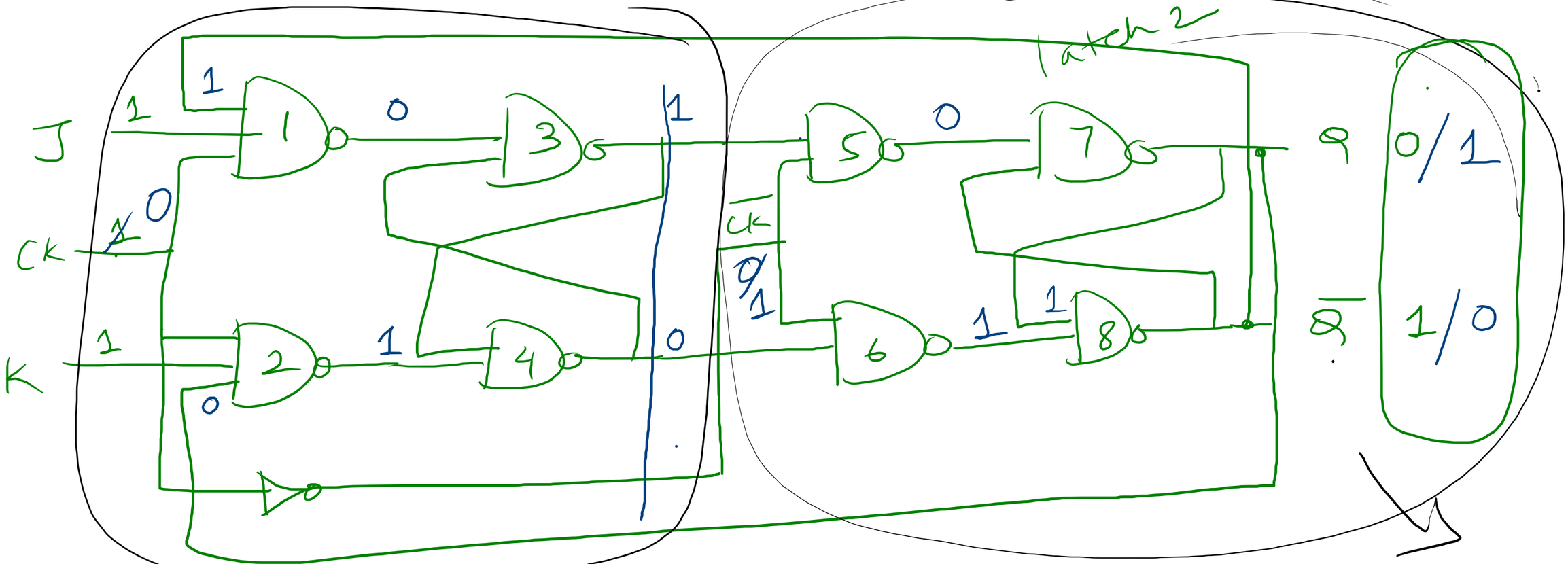
CK = high $Q_{t+2} = 0$,

Master slave latch



When ck = 1 , master / latch 1 is active
latch 2 is inactive → memory

When ck = 0 , latch 1 is inactive (memory)
latch 2 be active

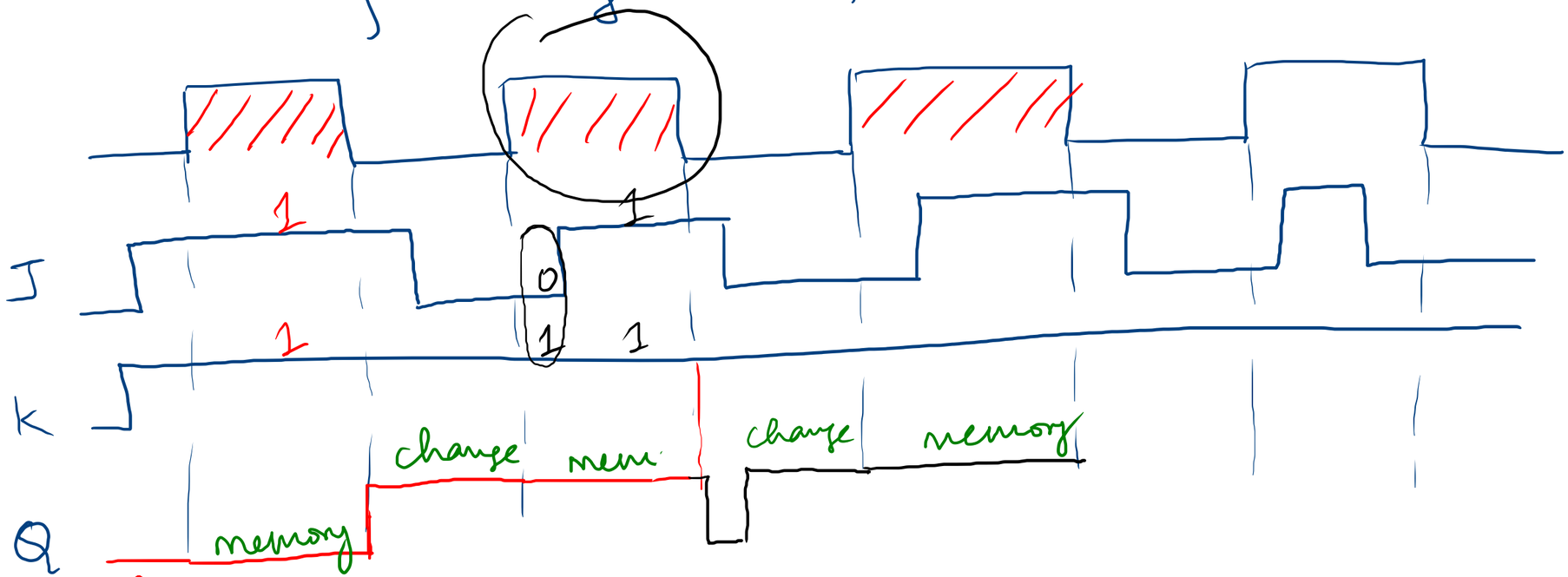


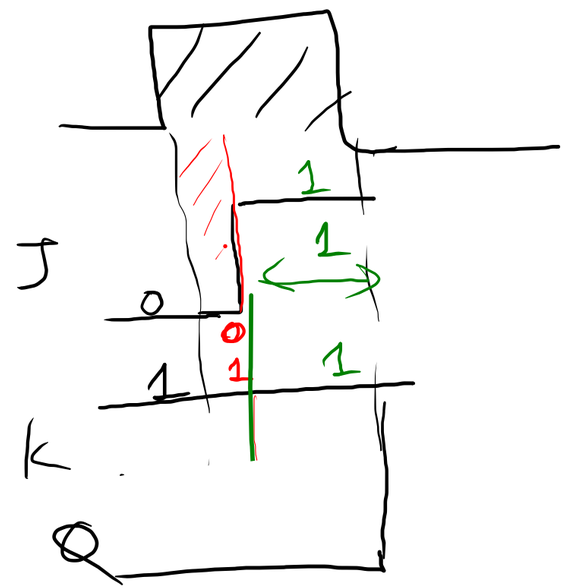
Assume $Q = 0$, $\overline{Q} = 1$ (initial value)

$CK = 1$ $J = 1$, $K = 1$, $Q = 0$, $\overline{Q} = 1$ ($CK = 1$ memory state

$CK = 0$, $J = 1$, $K = 1$, $Q = 1$, $\overline{Q} = 0$ $CK = 0$ output changes)

Timing Diagrams for JK master slave latch





Assume

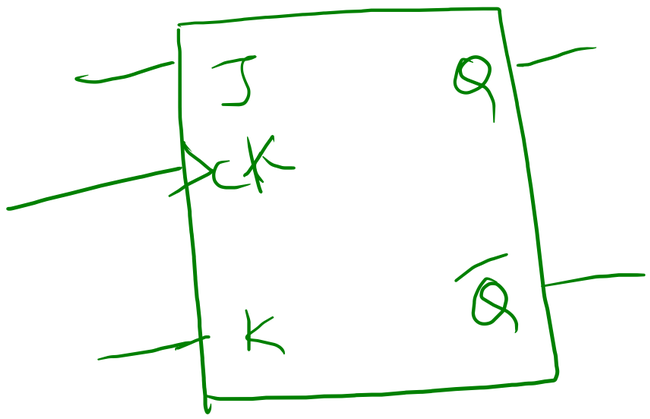
$Q_t = 0$

$\overline{Q}_t = 1$

$J = 0 \quad K = 1 \;, Q = 0$

$J = 1 \;, \quad K = 1 \;, Q = 1$

+ve Edge Triggered J-K ff.

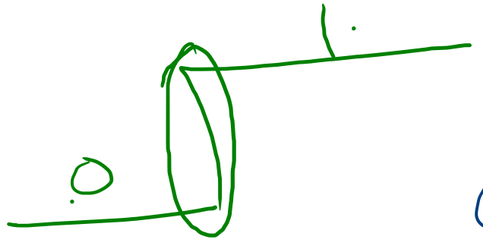


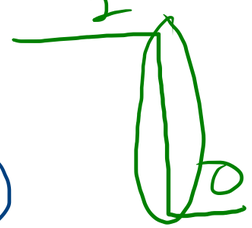
State table

CK	J	K	Q_{t+1}	$\overline{Q}_{t+1}$	
0/1	X	X	Q_t	$\overline{Q}_t$	→ memory
↓ ↑	0	0	Q_t	$\overline{Q}_t$	→ memory
↓	0	1	0	1	
↑	1	0	1	0	
↑	1	1	$\overline{Q}_t$	Q_t	

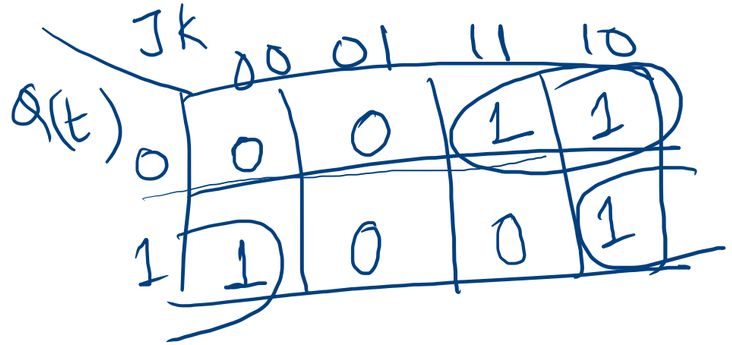
present ~~previous~~ state – Q_t

next state – Q_{t+1}





$Q_{(t+1)}$



$$Q_{(t+1)} = \overline{Q}_t J + Q_t \overline{K}$$

Excitation table for D ff

Circuit changes		Required Value
From	To	D
0	0	0
0	1	1
1	0	0
1	1	1

whatever value we need at the o/p, the same value should be applied to D i/p.