

Group 1 — Thursday 11:30 am  
9th June extra session  
LT 1

# Edge triggered JK flipflop

State table

CK	J K	$Q_t$	$\bar{Q}_t$	
0/1	X X	$Q_t$	$\bar{Q}_t$	$\bar{Q}_{t+1}$
↑	0 0	$Q_t$	$\bar{Q}_t$	$\bar{Q}_{t+1}$
↑	0 1	0	1	→ memory
↑	1 0	1	0	1 → reset
↑	1 1	$\bar{Q}_t$	$Q_t$	0 → set

$Q_t = 0 \rightarrow Q_{t+1} = 1$

$Q_t = 1 \rightarrow Q_{t+1} = 0$

## Excitation table

Circuit changes

Required values

Q <sub>t</sub>	From		To	Required values	
	0	1		Q <sub>t+1</sub>	J
0	0		0	0	X
0	1		1	1	X
1		0	0	X	1
1		1	1	X	0

J K  
 0 0  
 0 1

0 X

A 0  
 1 1

1 X

J K  
 0 1  
 1 1

11

JK

1 0  
 0 0

Q<sub>t+1</sub>

→ 1  
 → 1

11

unused

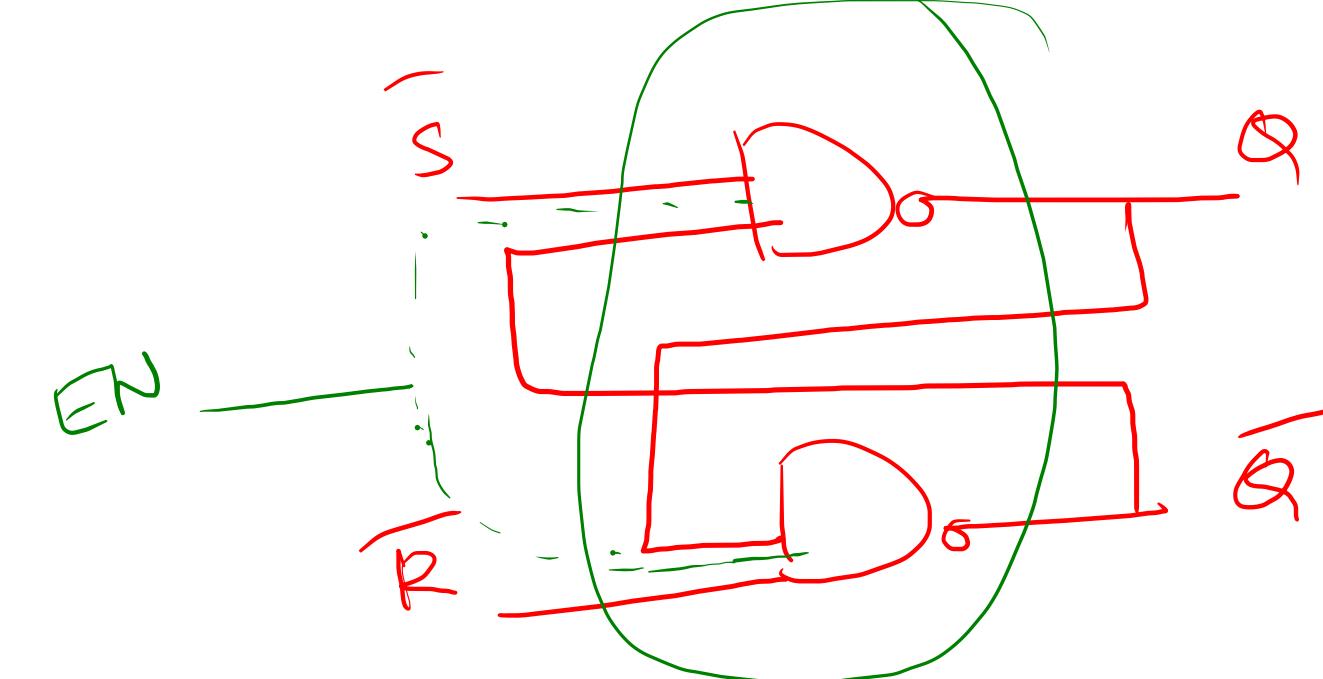
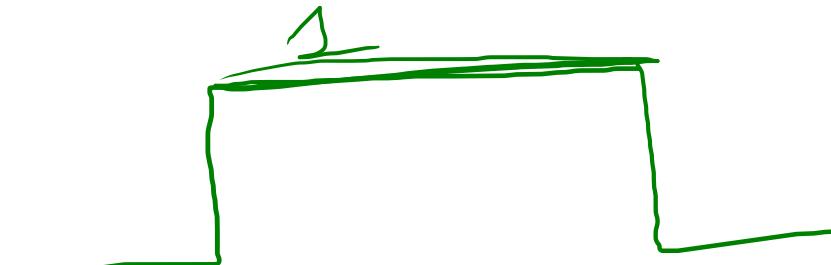
Solution

J K latch

$J = 1, K = 1, \text{ output toggles/complements}$

$$Q_t = 0, Q_{t+1} = 1$$

$$\text{or } Q_t = 1, Q_{t+1} = 0$$

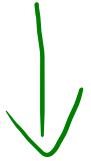


cross coupled  
NAND  
gates

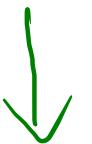


Solution to race around

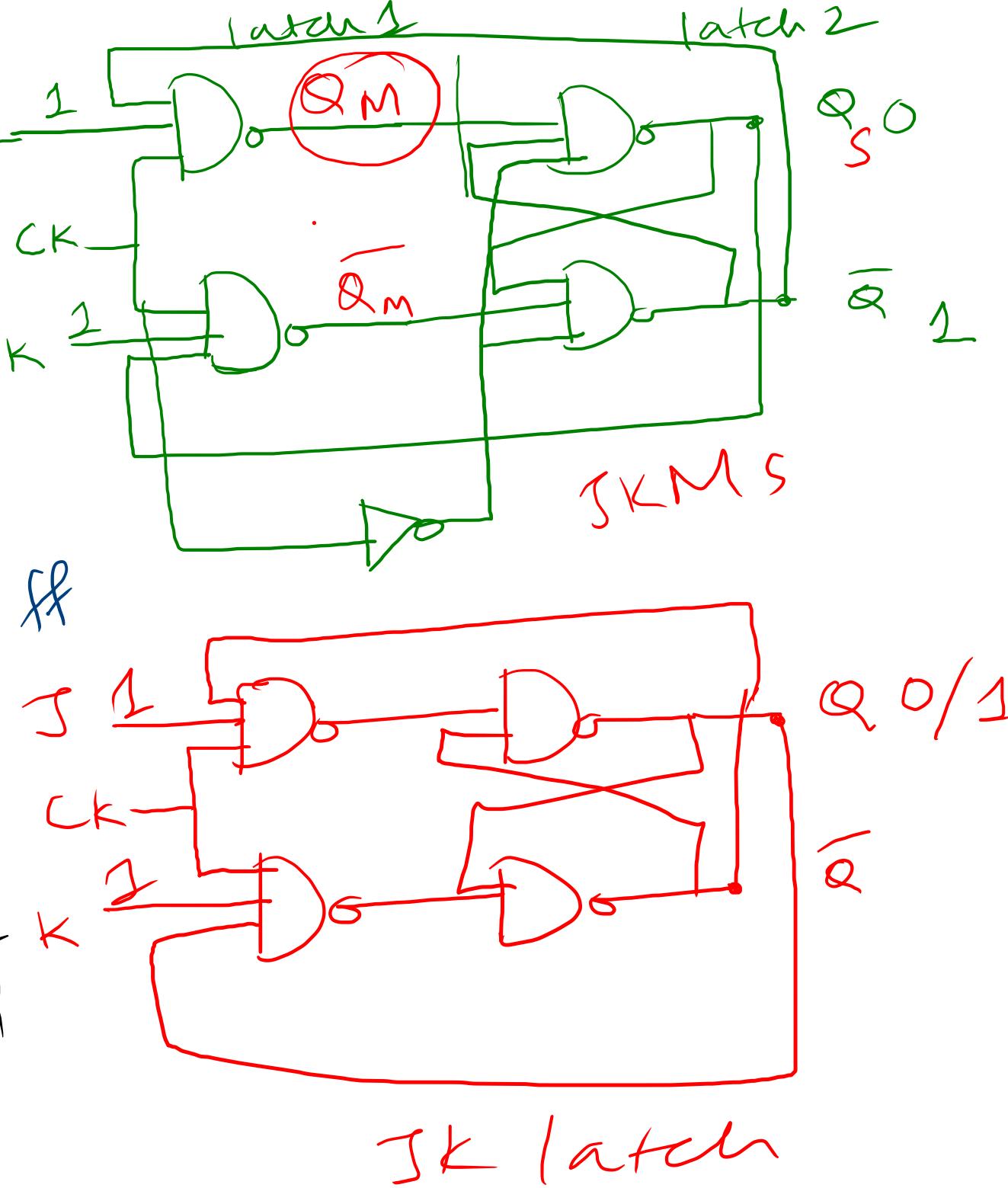
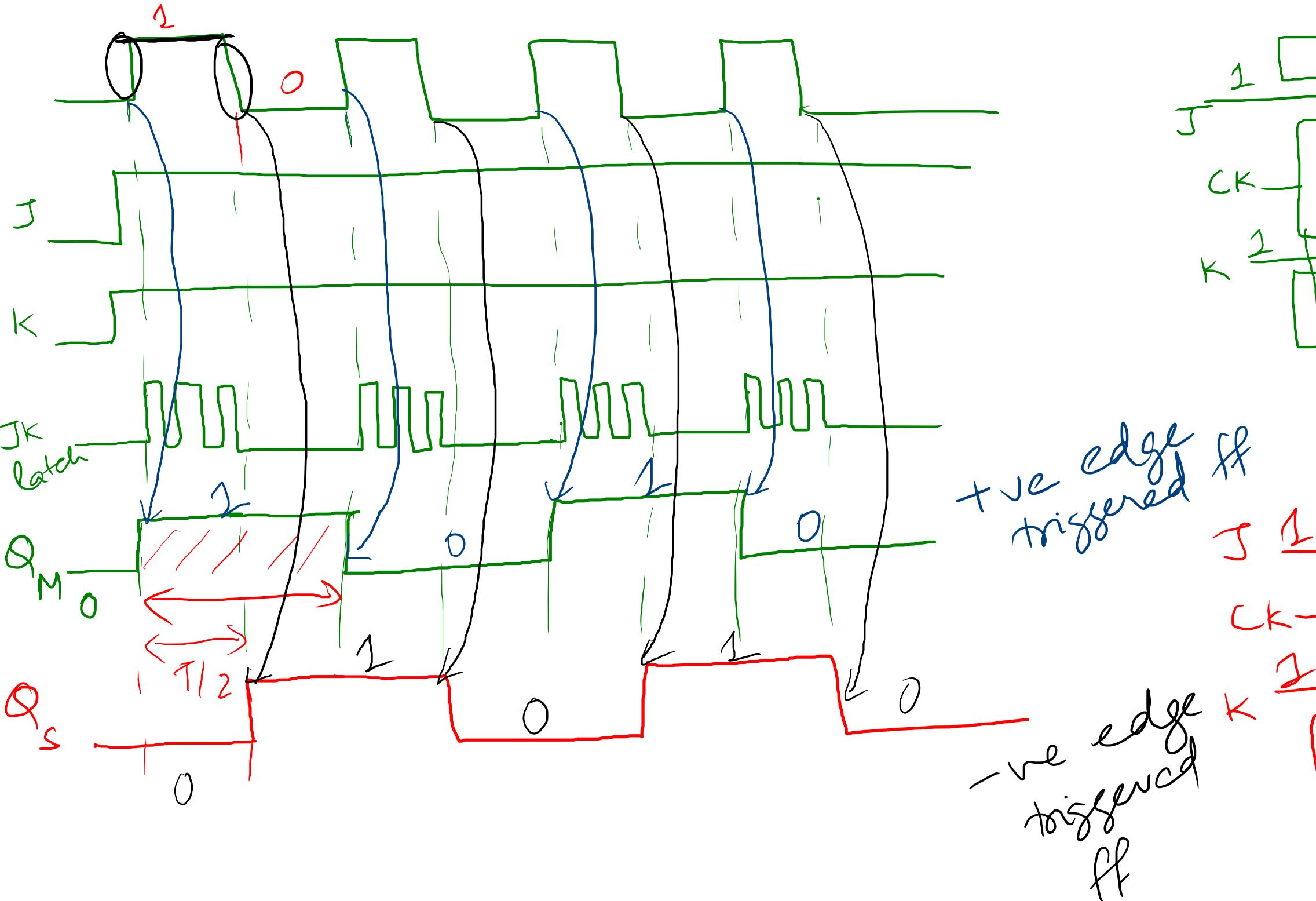
Master slave



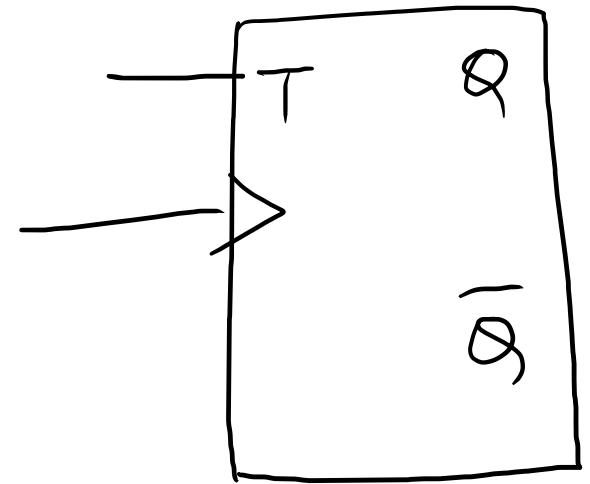
latch 1



latch 1



+ve edge triggered T ff.

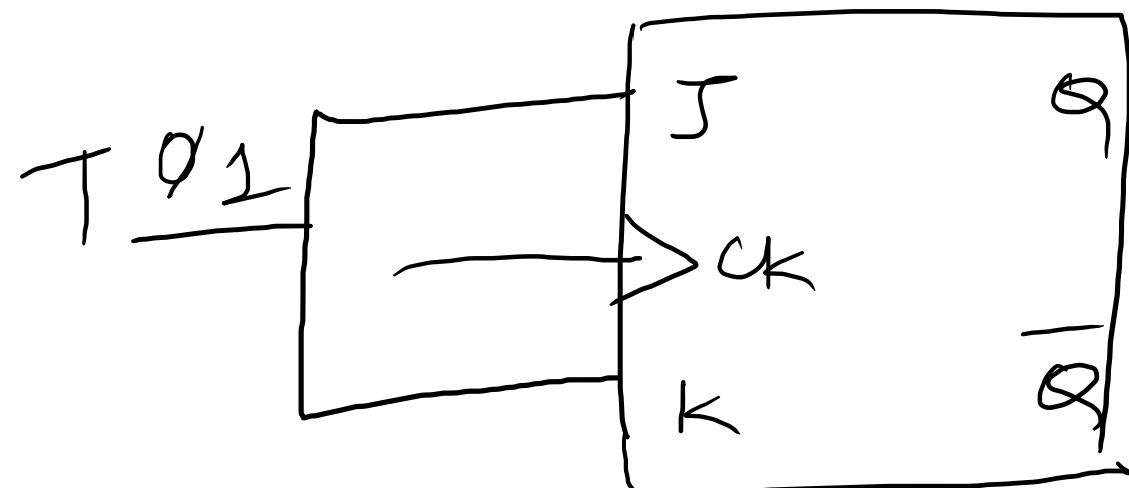


State table

CK	T	$Q_{t+1}$	$\bar{Q}_{t+1}$
0	1	$Q_t$	$\bar{Q}_t$
↑	0	$Q_t$	$\bar{Q}_t$
↑	1	$\bar{Q}_t$	$Q_t$

Memory      Toggle

Special case of JK flip flop.



with inputs J & K tied together.

$Q_t$	J	$Q_{t+1}$
0	0	1
1	1	0

$$Q_{t+1} = T \bar{Q}_t + \bar{T} Q_t$$

$$= T \oplus Q_t$$

# Excitation table

Circuit changes		Required value
From	To	T
0	0	0
0	1	1
1	0	1
1	1	0

## Flipflops with asynchronous preset & clear

X — unknown state

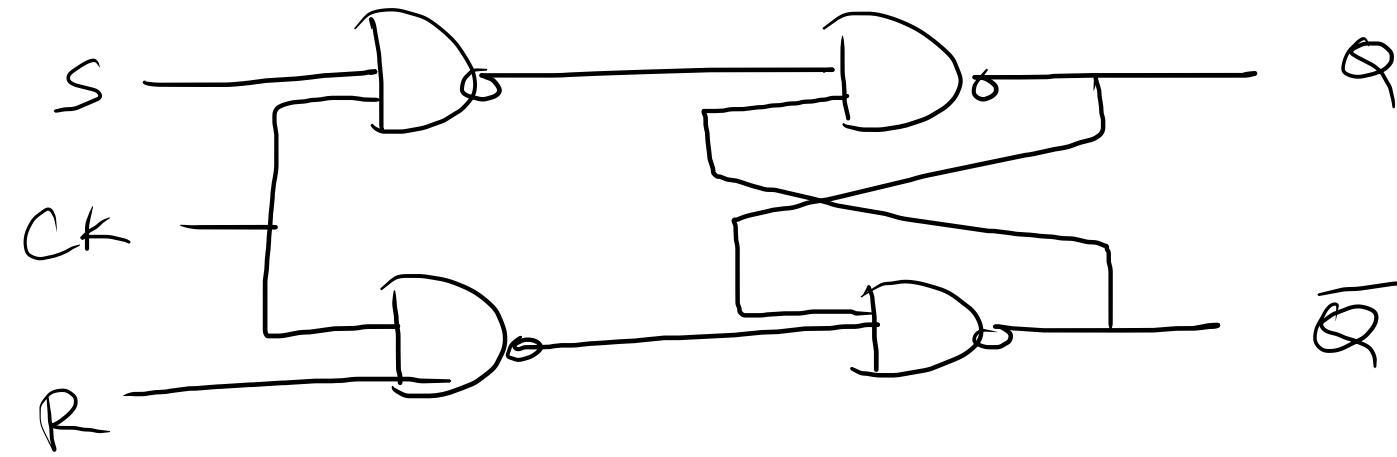
i/p →  $\overline{\text{Preset}}$  } active low sigs  
 $\overline{\text{Clear}}$

Initially  
set (1)  
or  
resetting (0)  
ff

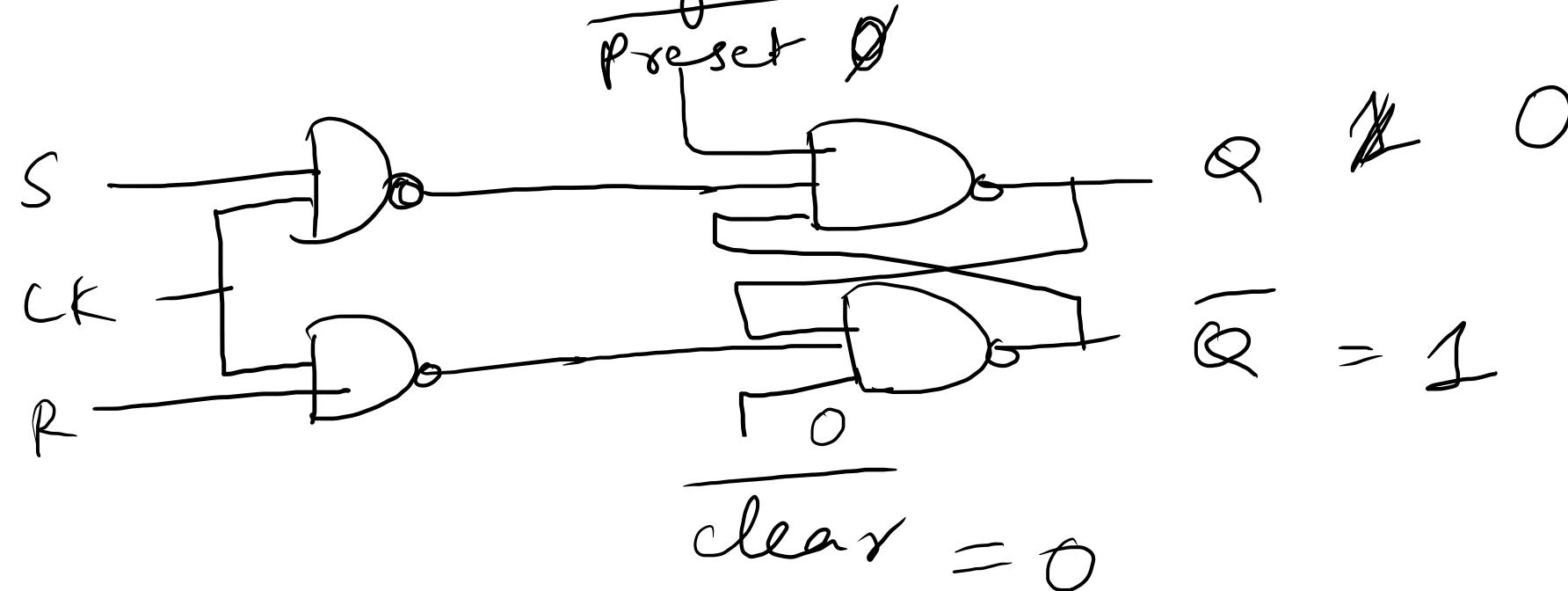
$$\overline{\text{Preset}} = 0, \quad Q = 1$$

$$\overline{\text{Clear}} = 0, \quad Q = 0 \quad (\text{pin})$$

SR ff

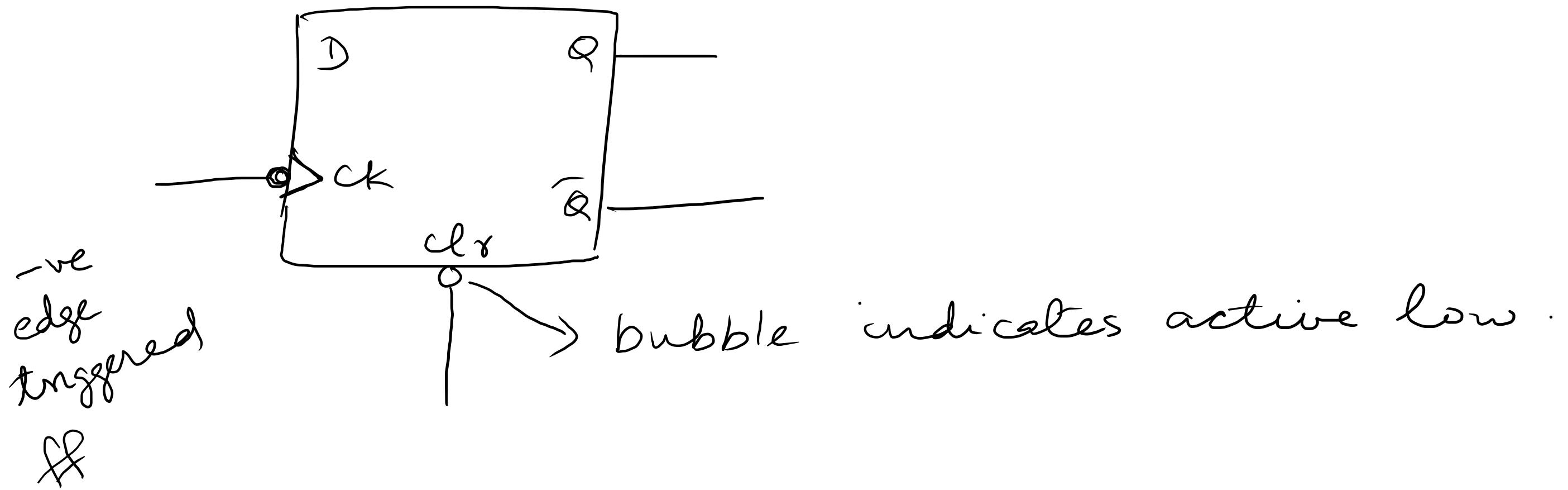


SR ff with asynchronous preset & clear i/p's

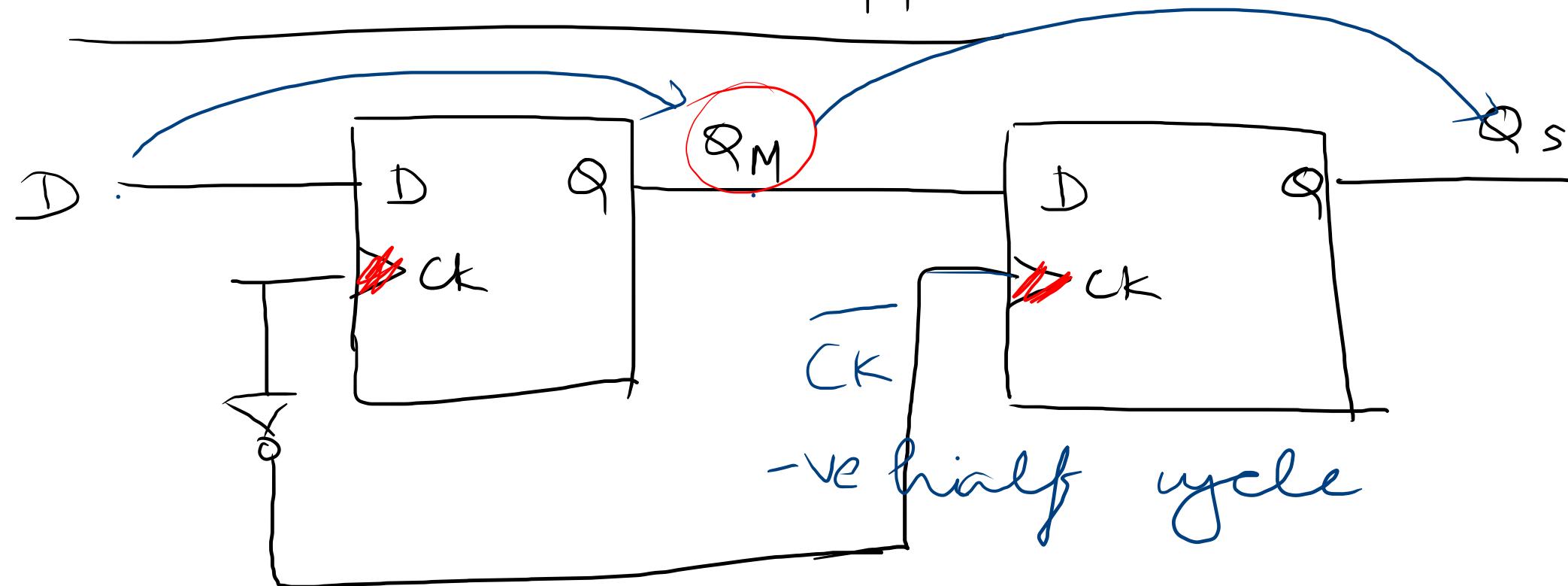


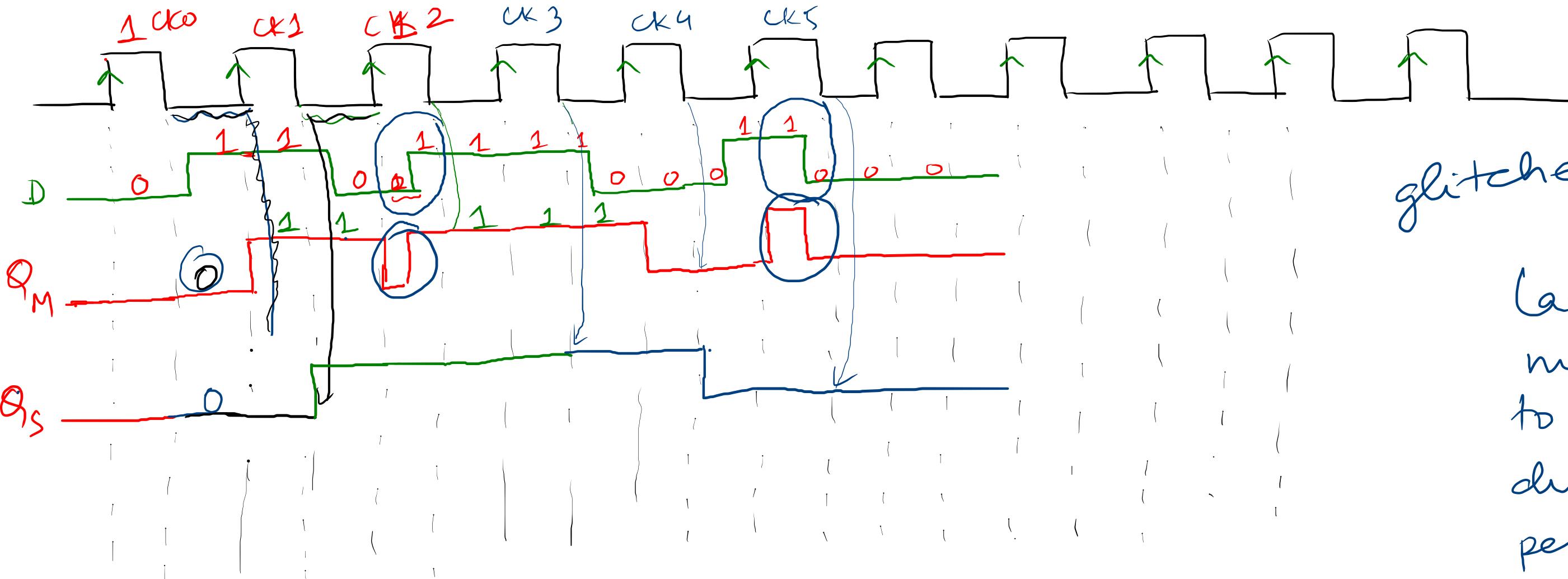
For normal operation  
of ff  
preset & clear  
should be high(1)

D ff with clear i/p



D master slave ff





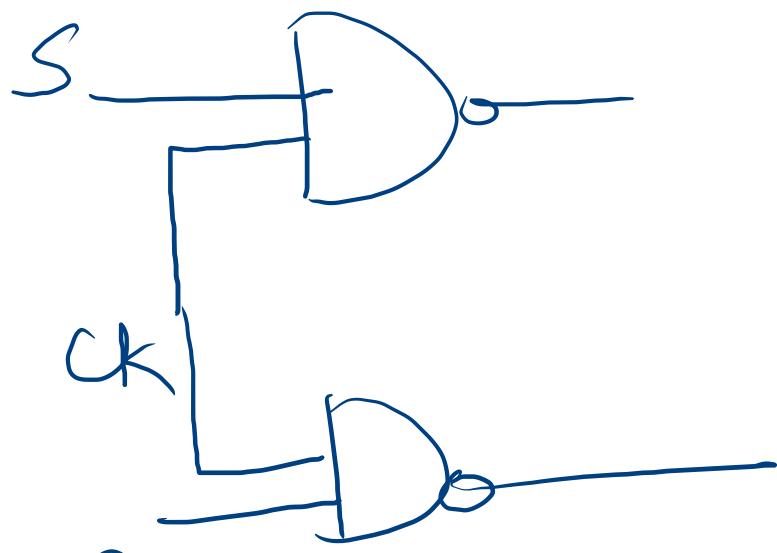
glitches

Latches are more sensitive to input changes during clock period (0 or 1)

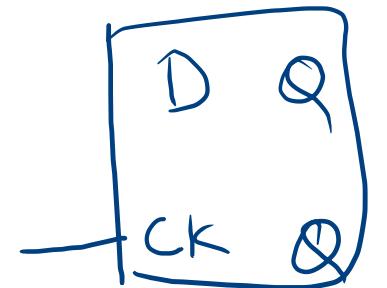
If can generate stable output

for an entire clock period.

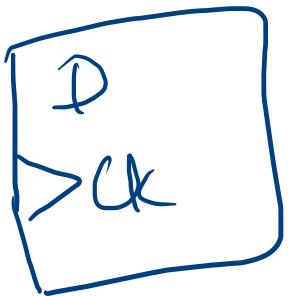
How is edge trigger implemented



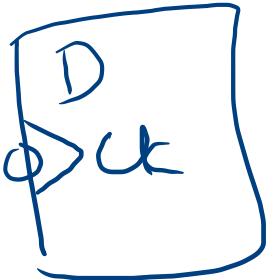
~~EN~~ - is 1 for a long period



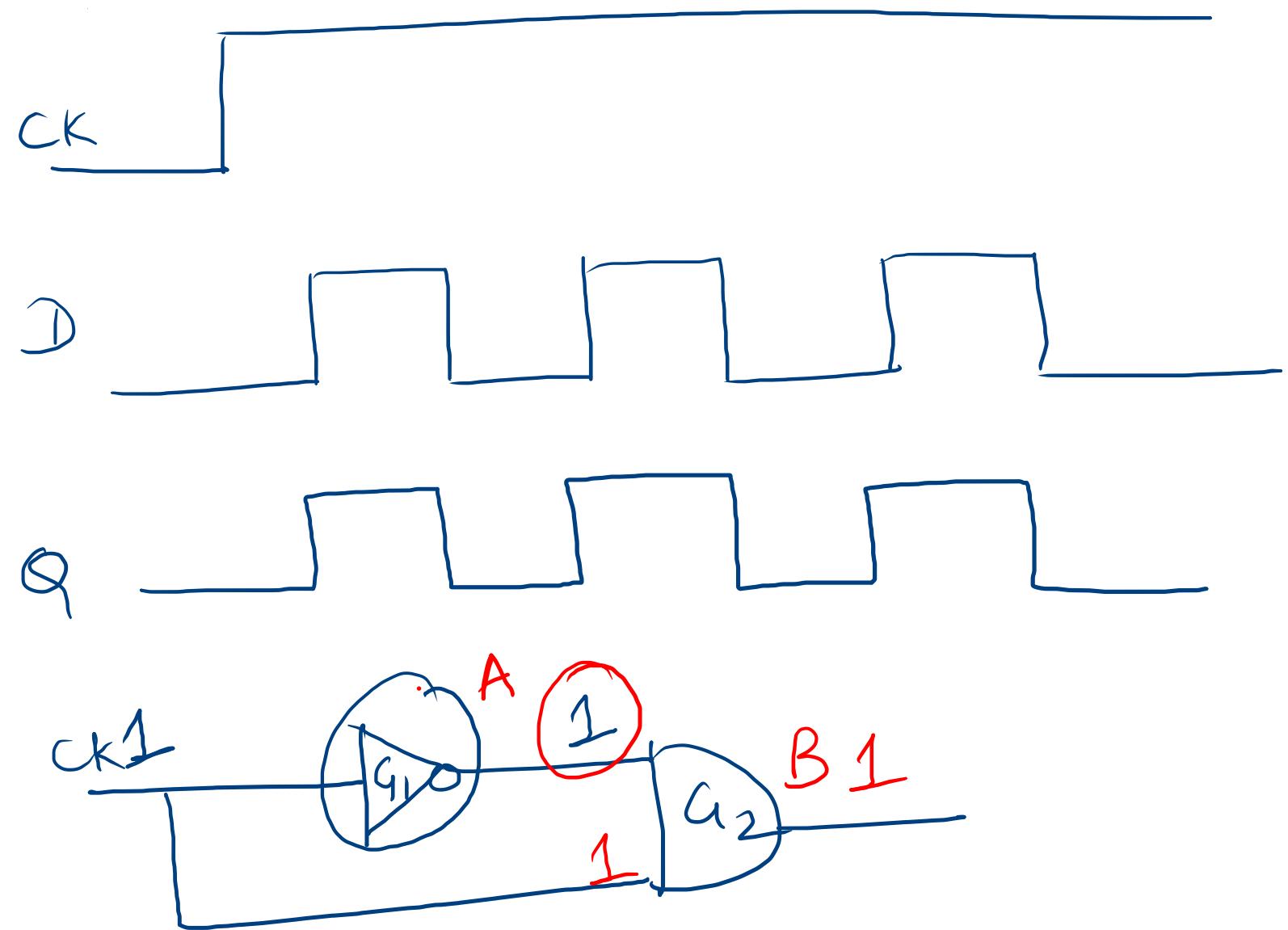
latch



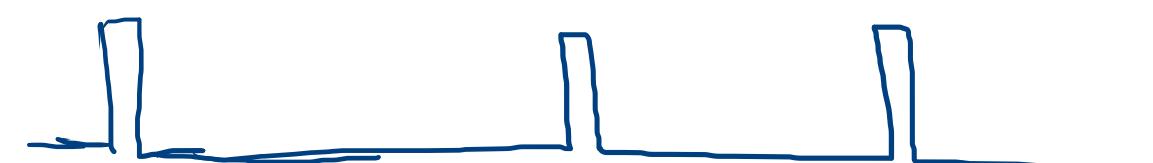
+ve  
edge triggered  
ff



-ve  
edge triggered  
ff.



CK width to a very short pulse  
Edge triggered

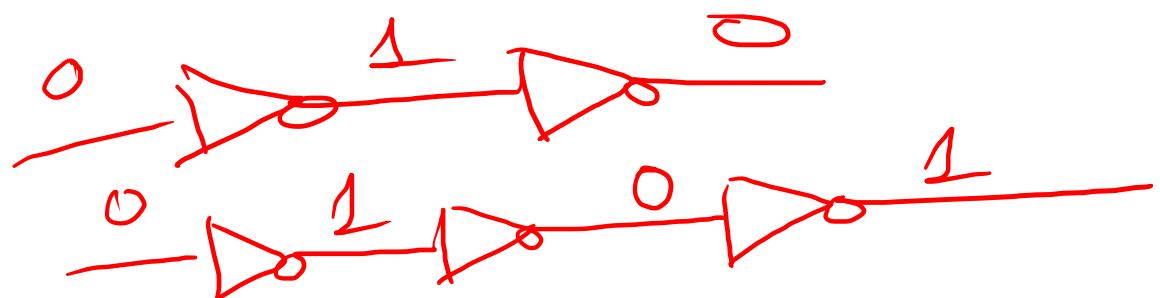


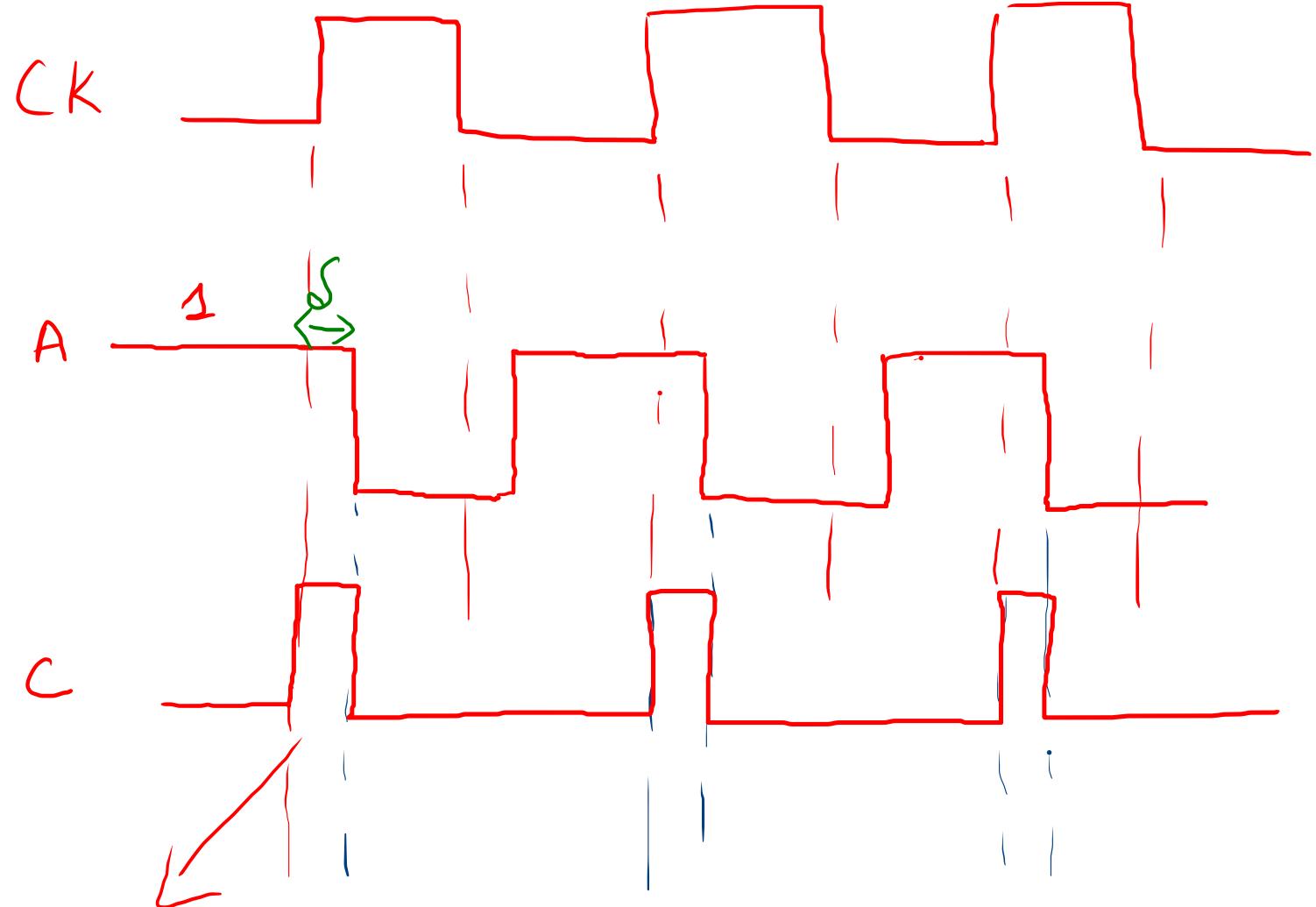
We try to generate a very narrow pulse

$G_1$  - has a propagation delay  
op of  $G_1$  will become 0 after  
(the delay

Initially  $CK = 0$ , op of  $G_1$  is set to 1

odd no of inverters





edge  
triggering

Value of A changes  
after  $\delta$  'time'.