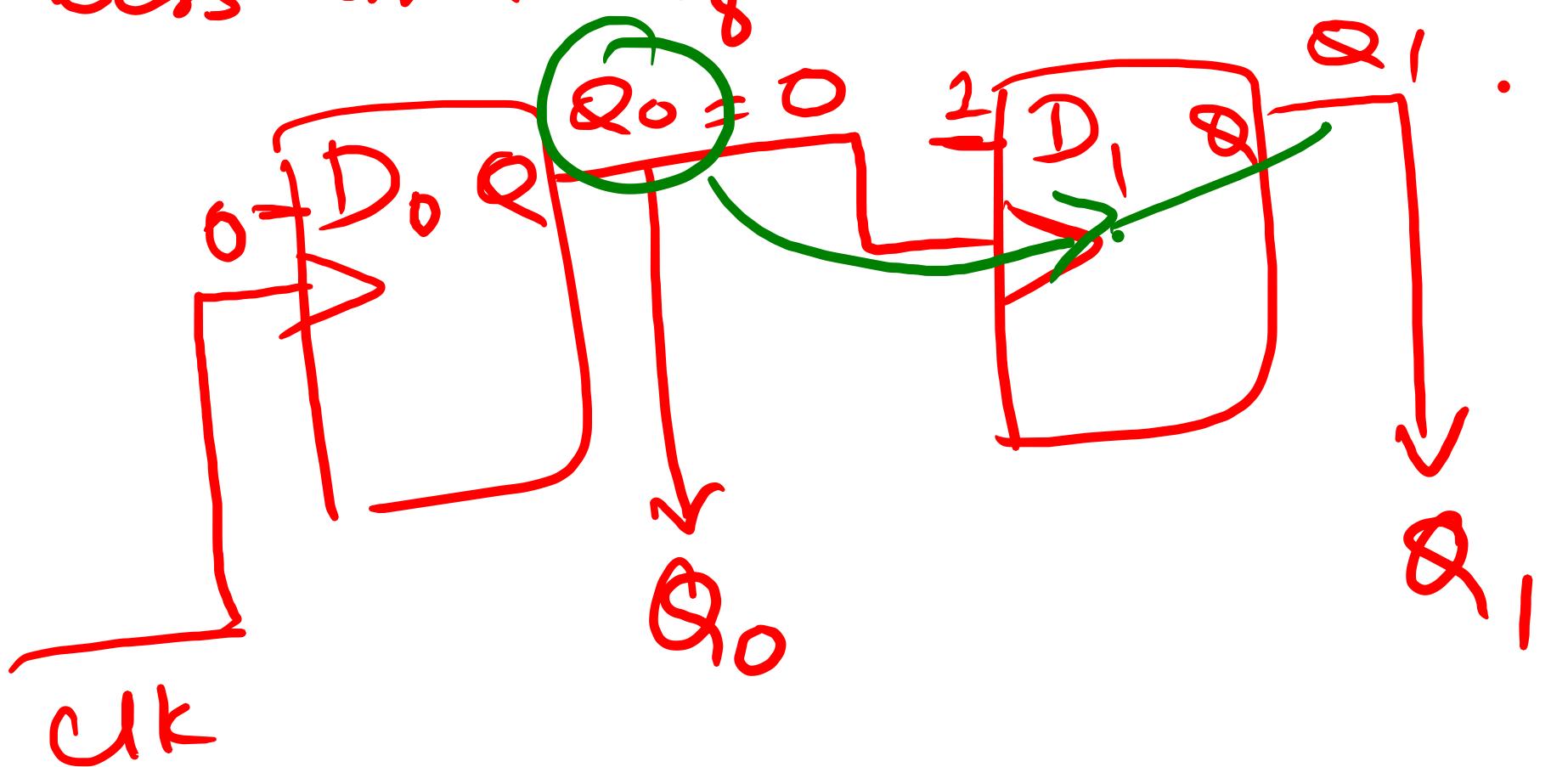


Asynchronous Counters (Ripple counters)

easy to design

less amt of hardware



Asyn. becuz flip-flops are not driven by same clock & hence they do not change state simultaneously.

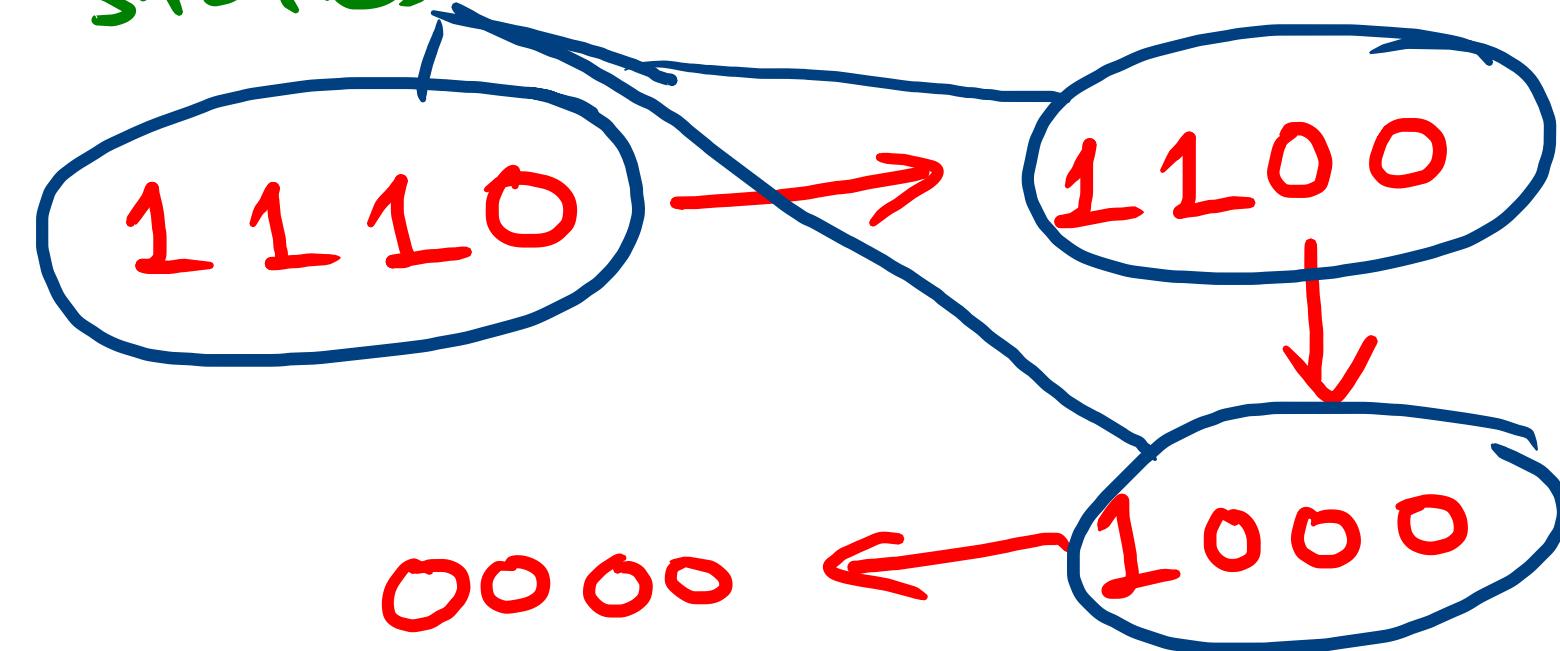
$$\overline{1111} \rightarrow \overline{0000}$$

$$Q_3 Q_2 Q_1 Q_0 \quad Q_3^+ Q_2^+ Q_1^+ Q_0^+$$

$$1111 \longrightarrow 0000$$

intermediate states

$$1111 \longrightarrow$$

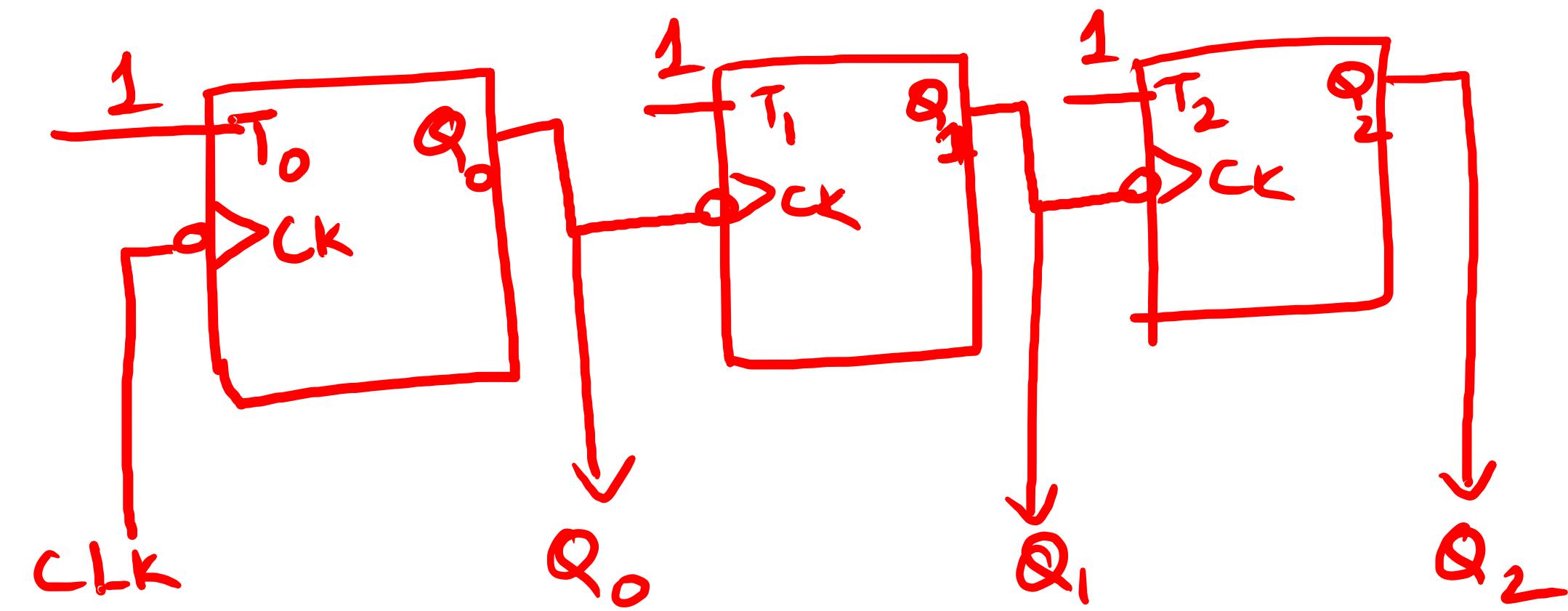


Design of 3 bit ripple counter

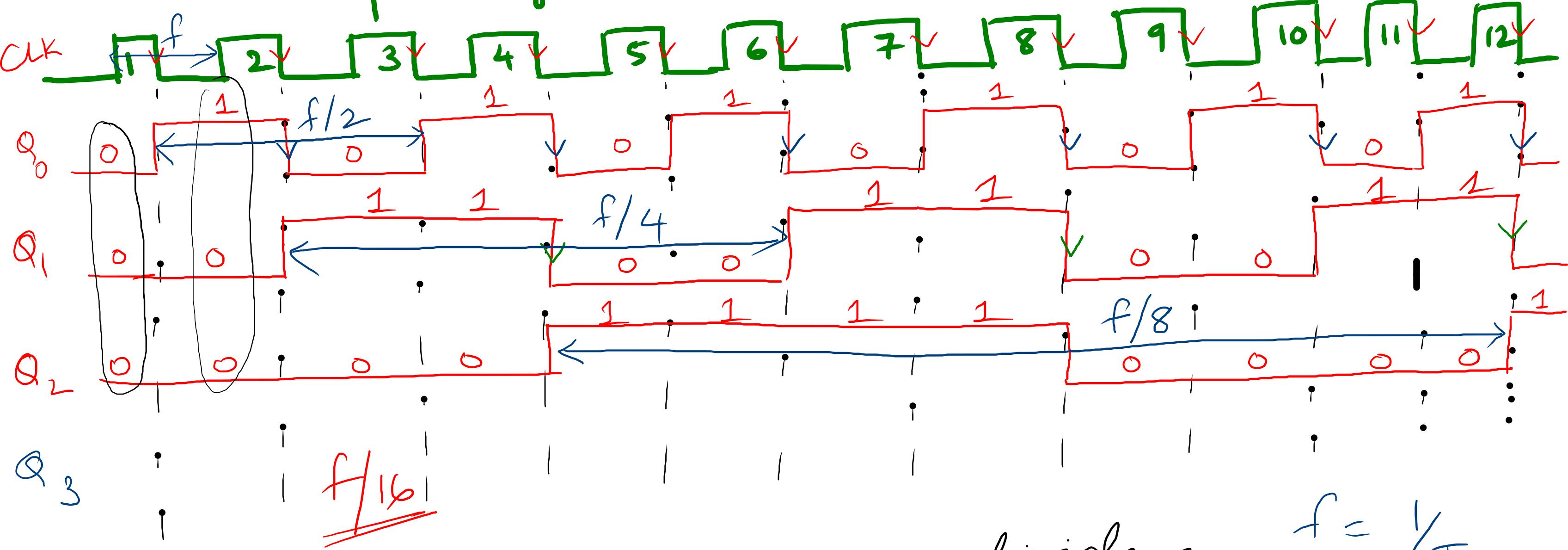
ck	Q_2	Q_1	Q_0
0	0	0	0
1	1	0	1
2	0	1	1
3	0	1	0
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Initial state

$$Q_2 Q_1 Q_0 = 000$$



Timing diagram



frequency divider
circuit

$Q_3 Q_2 Q_1 Q_0 \text{ mod } 16$
 $0 - 15$

freq of MSB $f/16$

$$f = \frac{1}{T}$$

M

freq of
MSB f/M

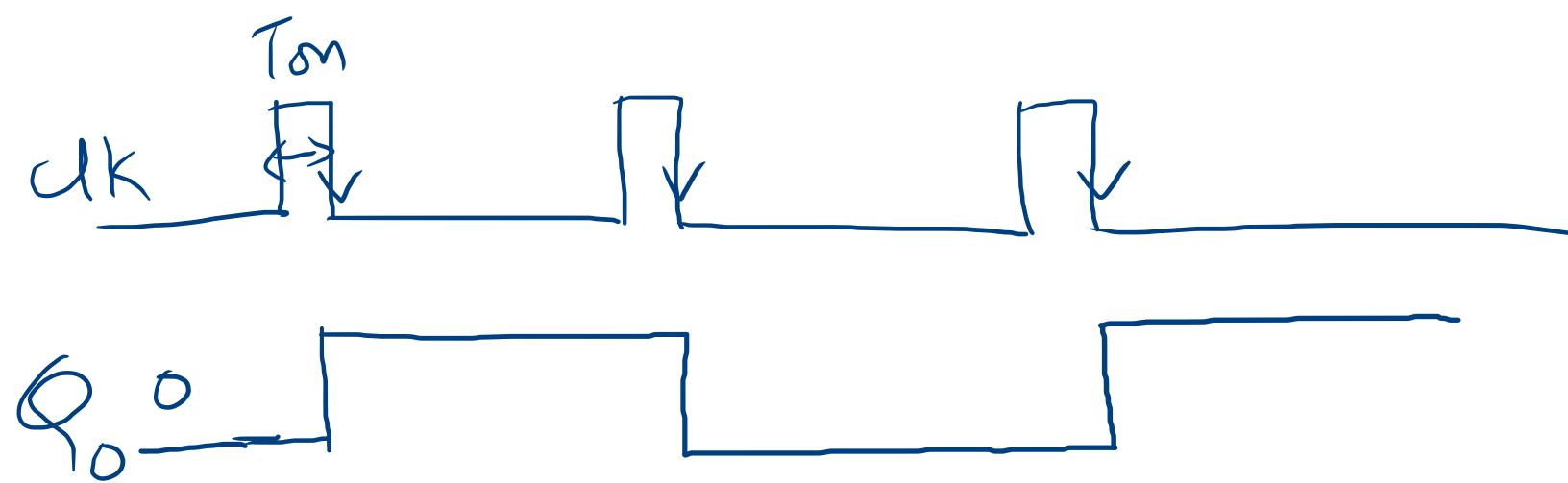
Sum of clock freq of ip clk = f

frequency of pulse train at $Q_0 = f/2$

frequency of pulse train at ~~at~~ $Q_1 = f/4$

frequency of pulse train at $Q_2 = f/8$

An n bit counter is called a modulo 2^n counter
or divide by 2^n counter.

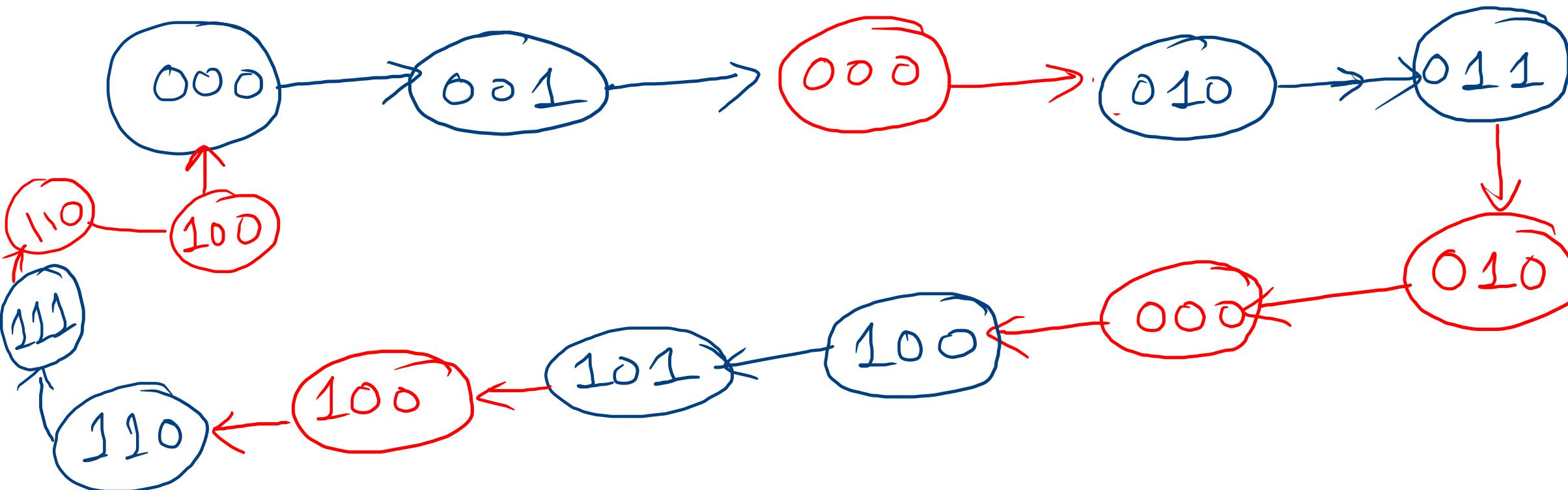


The sigs from the op of the counter will be
square waves

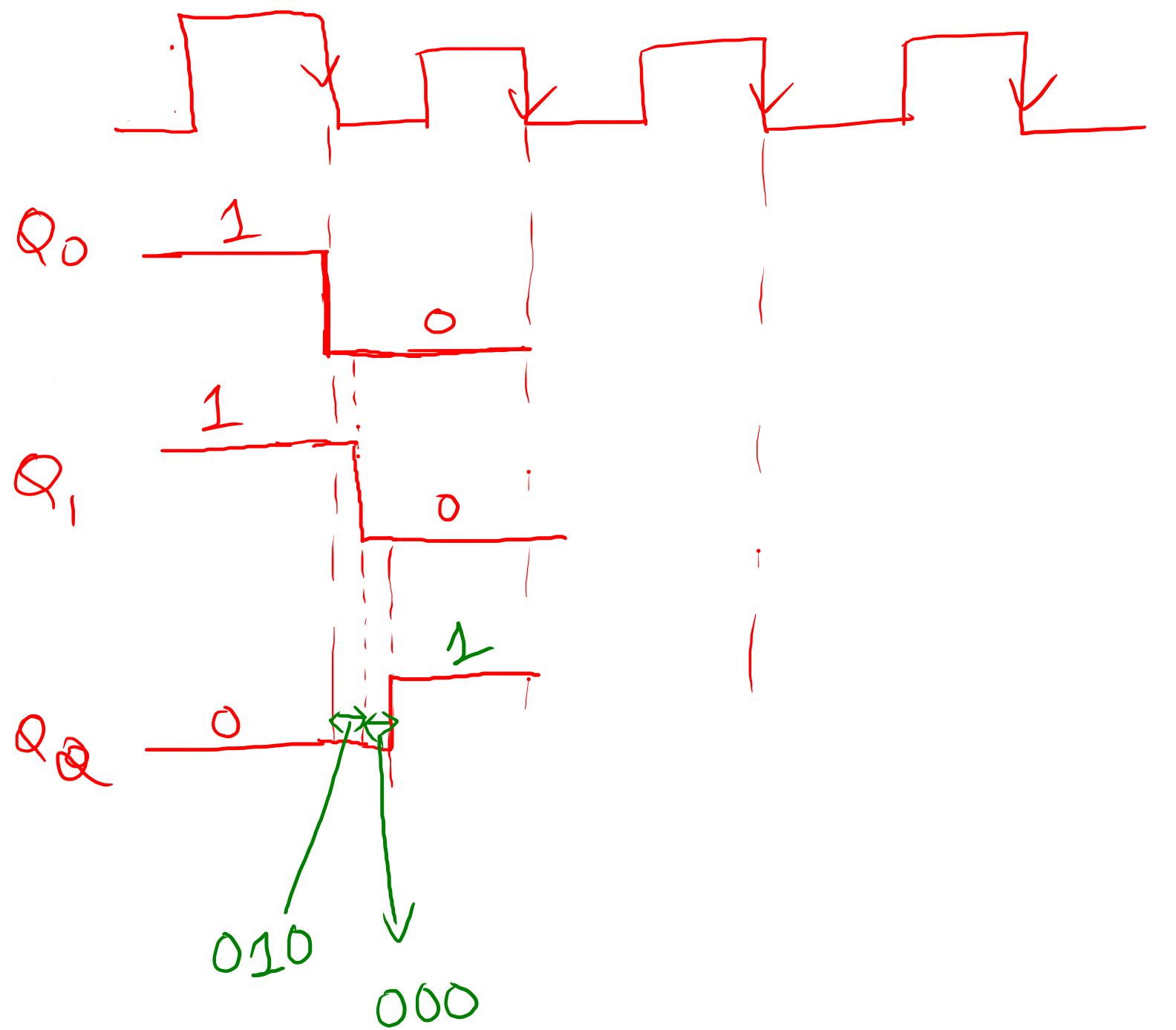
Transient states during counting

3 bit counter

LSB will change state first



001
010
011
100
101
110
111
000
100



$011 - 100$
 011
 010

$Q_2 \ Q_1 \ Q_0$
1 1 1

1 1 0
↓
1 0 1

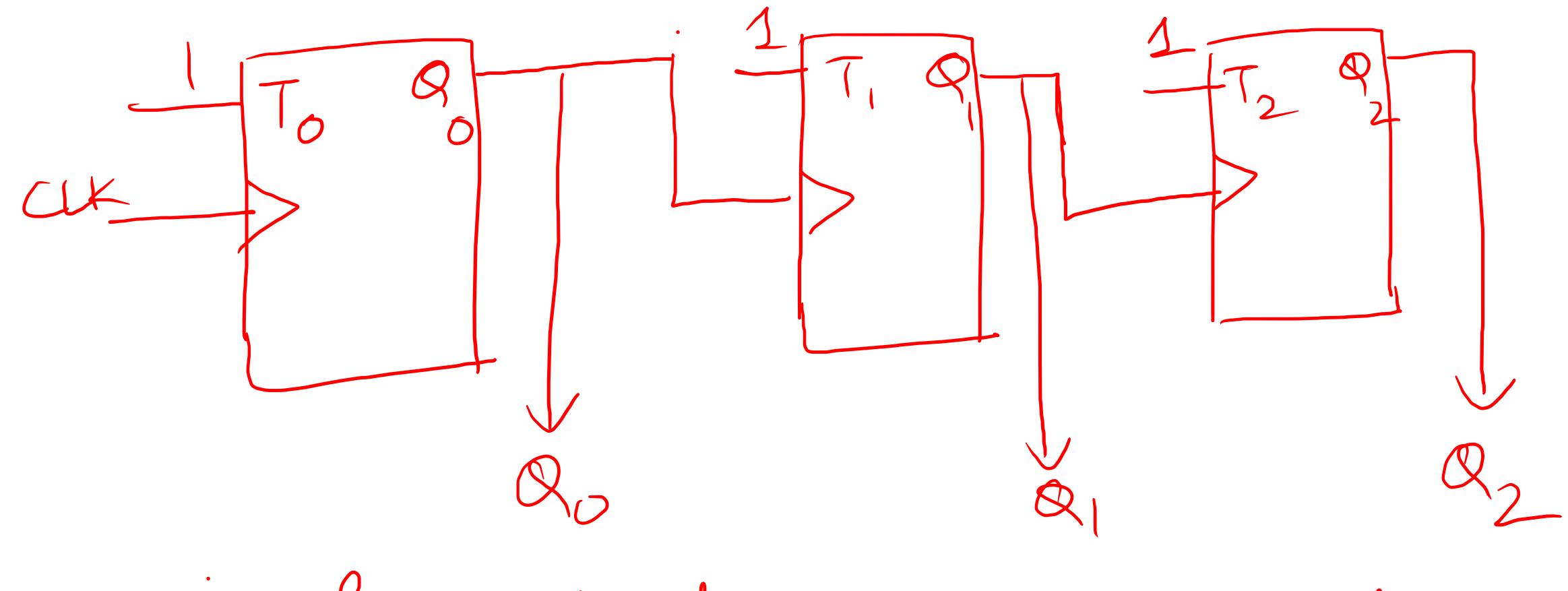
1 0 0
↓
0 1 1

0 1 0

0 0 1

0 0 0

Down counter



implemented using +ve edge triggered ff.

Design of binary ripple counter of any arbitrary modulus.

Modulo M counter

Count from $0 \rightarrow M-1$

$$M = 6$$

$$0 \rightarrow 5$$

no of bits/stages

$$= \log_2 M$$

Gating circuit

1 0 1 3 bits

- max count

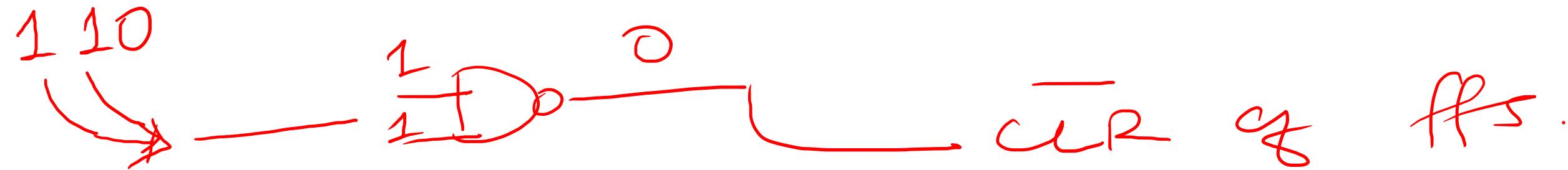
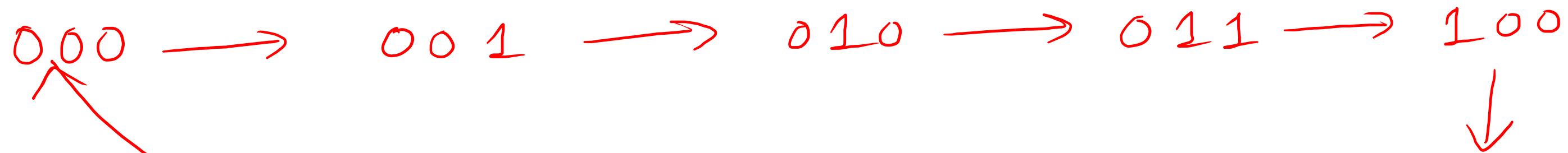
1 1 1

↓
forcibly reset the op's to 0.

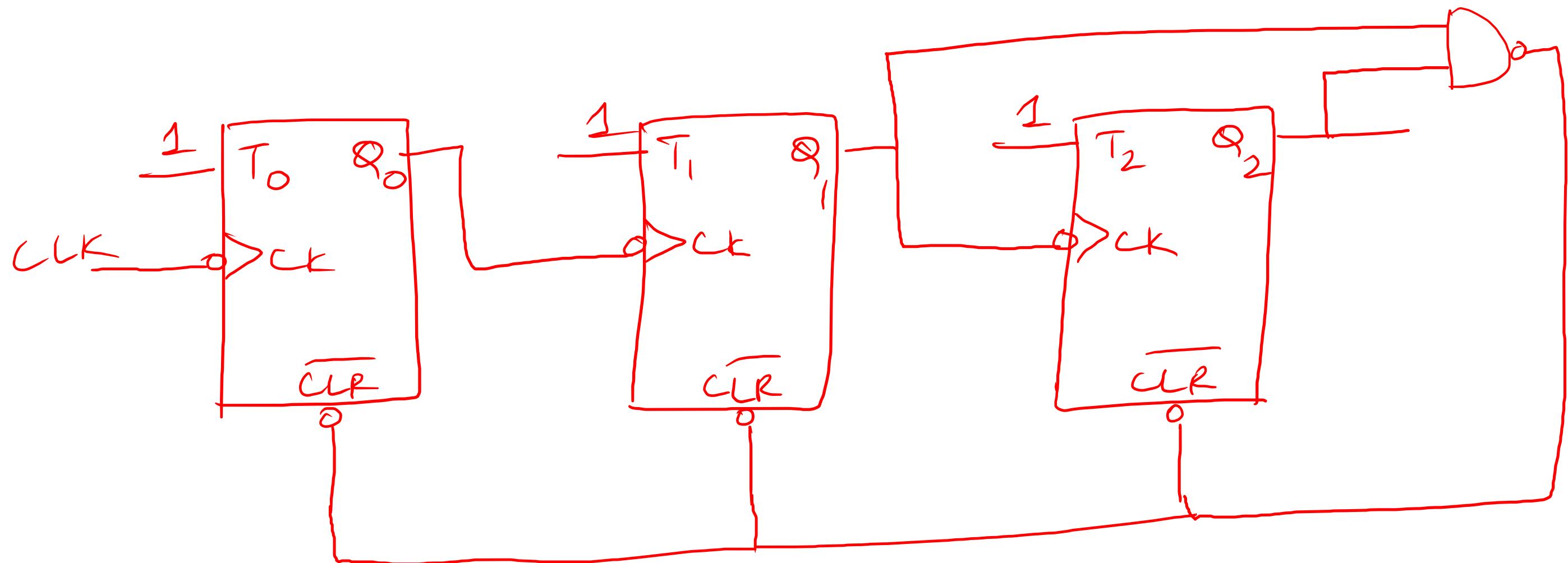
o/p of the gating ~~or~~ circuit
to \overline{CLR} i/p's of the ffs.

will be connected

Mod 6 counter

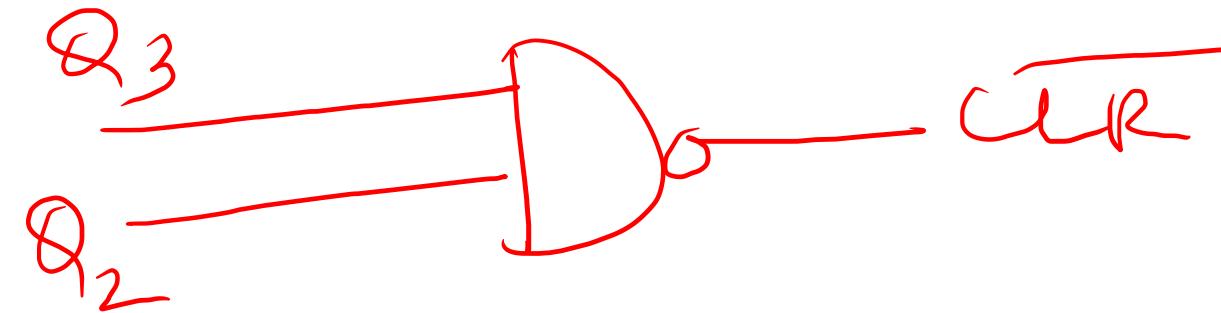


Mod 6 counter circuit



forbidden
state
 $Q_2 \quad Q_1 \quad Q_0$
1 1 0

Mod 12



4 bit counter

0 - 15

Mod 16

MSB

~~MSB~~ freq of pulse train at $Q_3 = f/16$

for mod M counter

freq of pulse train at MSB = f/M

0000 - 1011

forbidden state - 12

↓
1100
 $Q_3 Q_2 Q_1 Q_0$

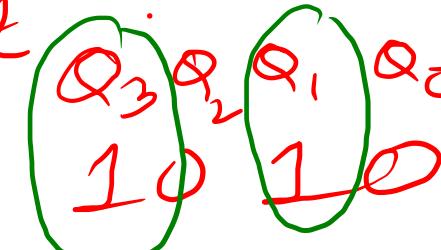
1001 - 9

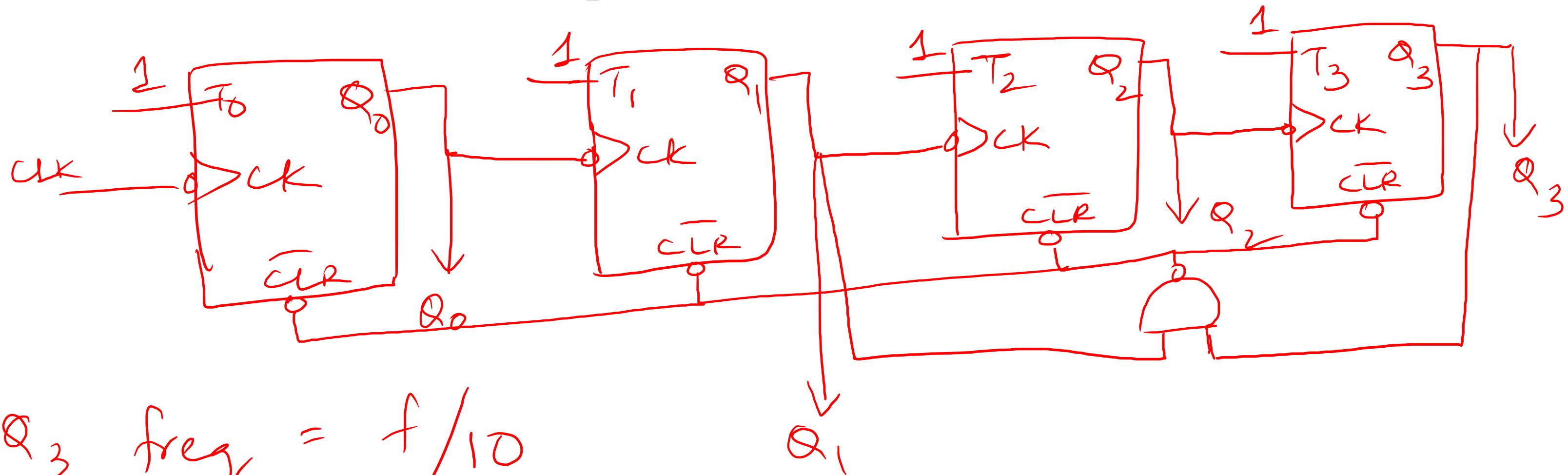
1010 - 10

1011 - 11

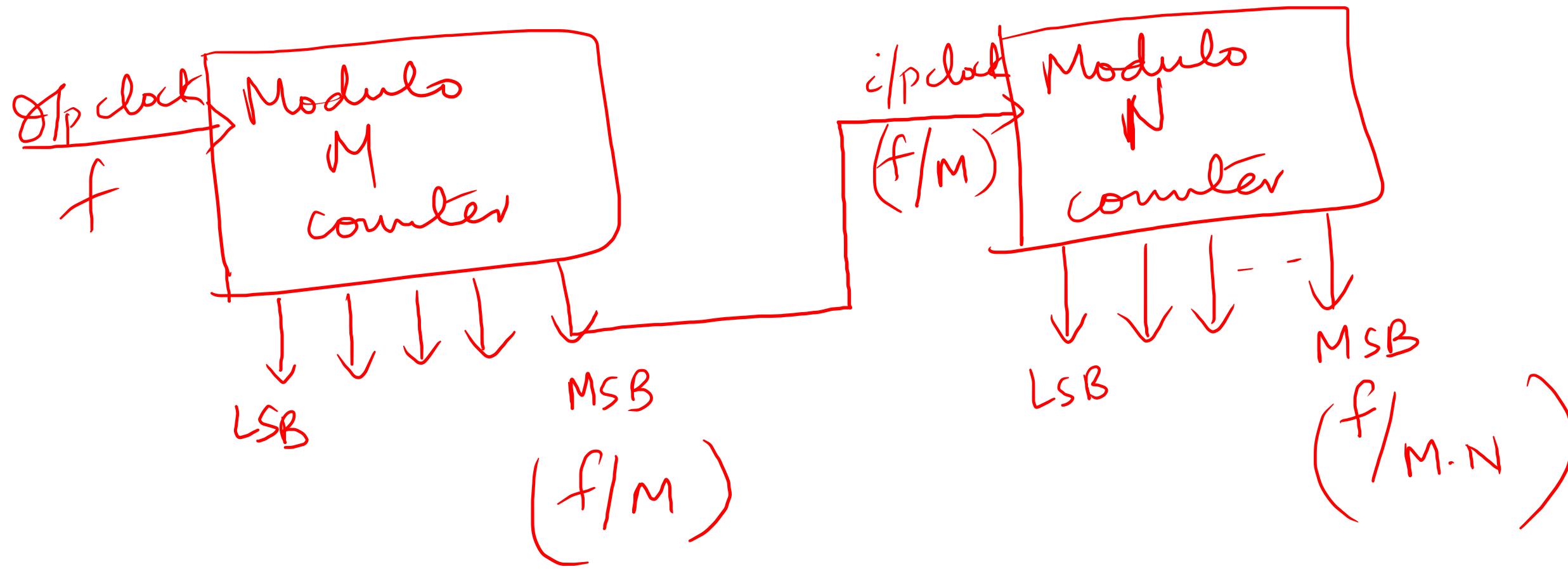
1100 - 12

Widely used ripple counter is mod - 10 .

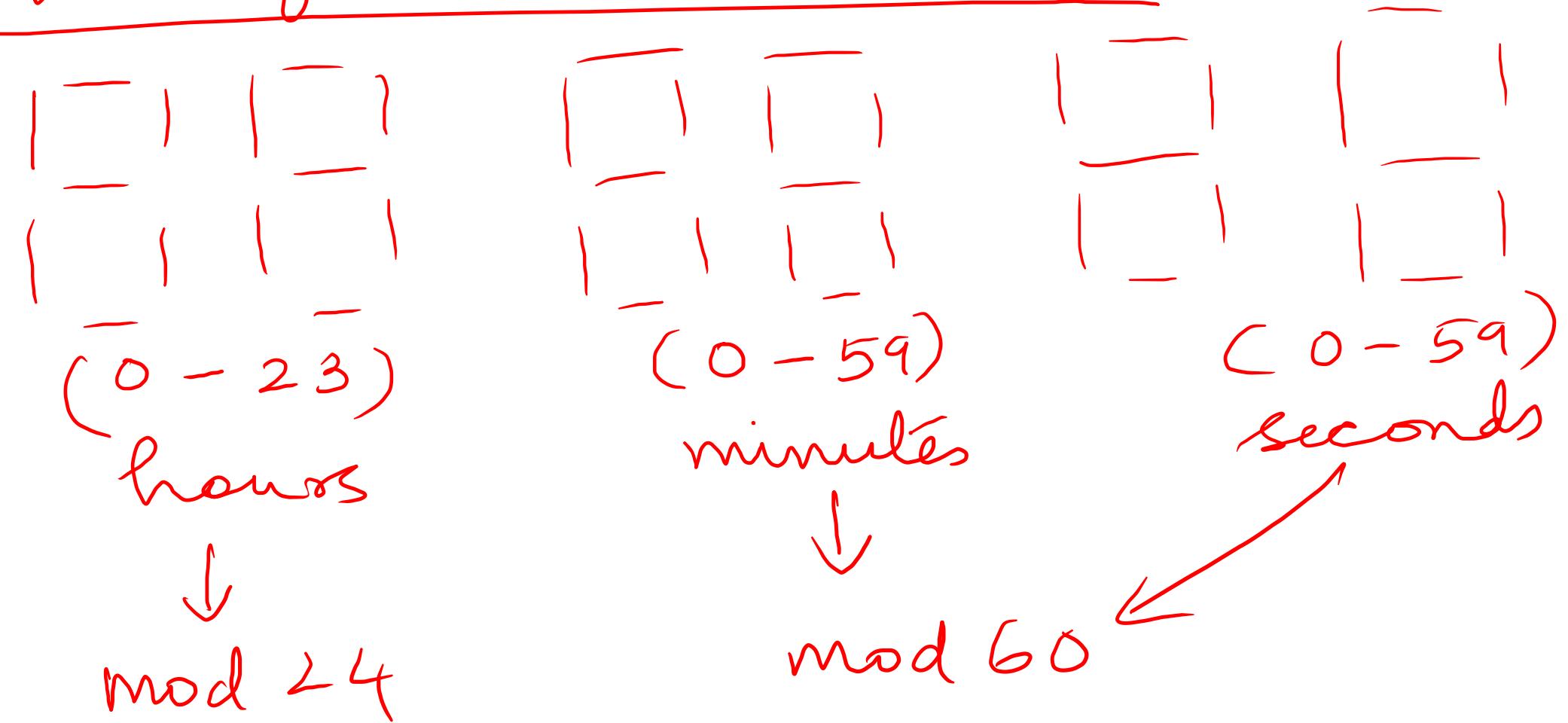
1001 - max count
forbidden state - 



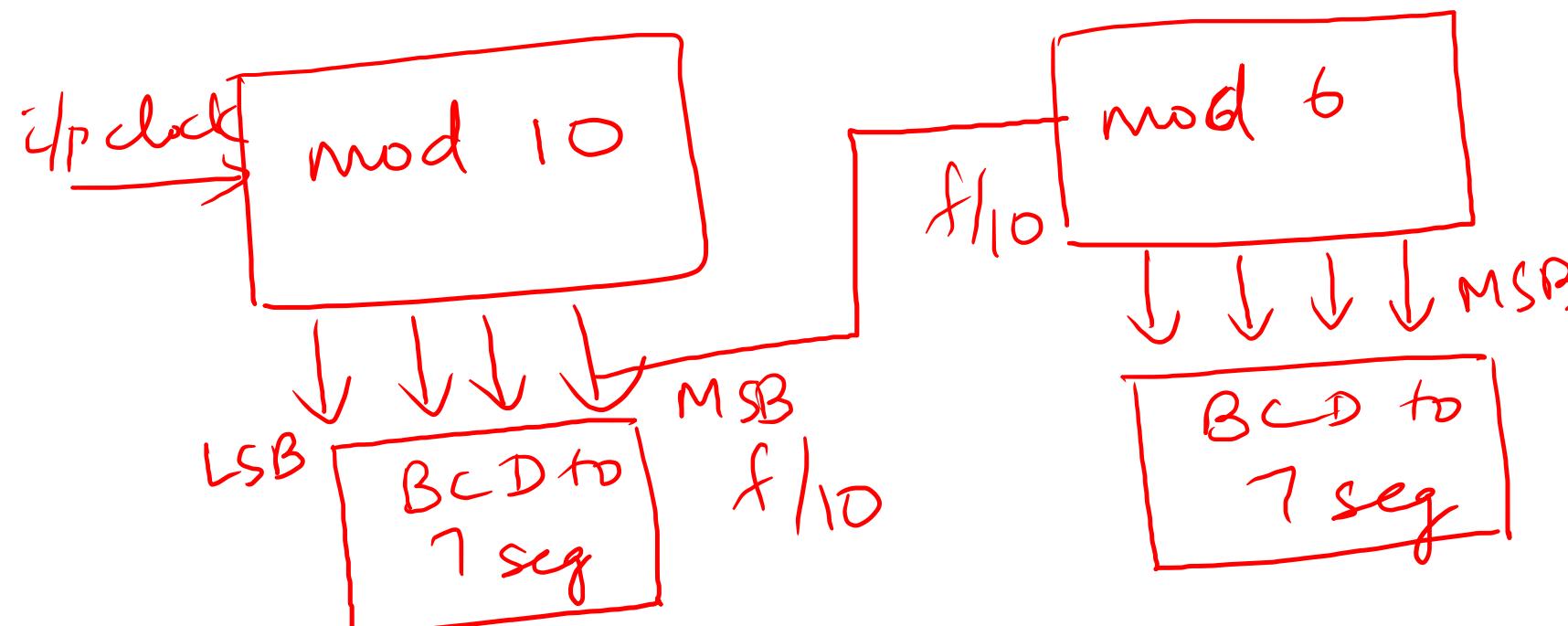
Cascading of ripple counters



Design of digital clock.

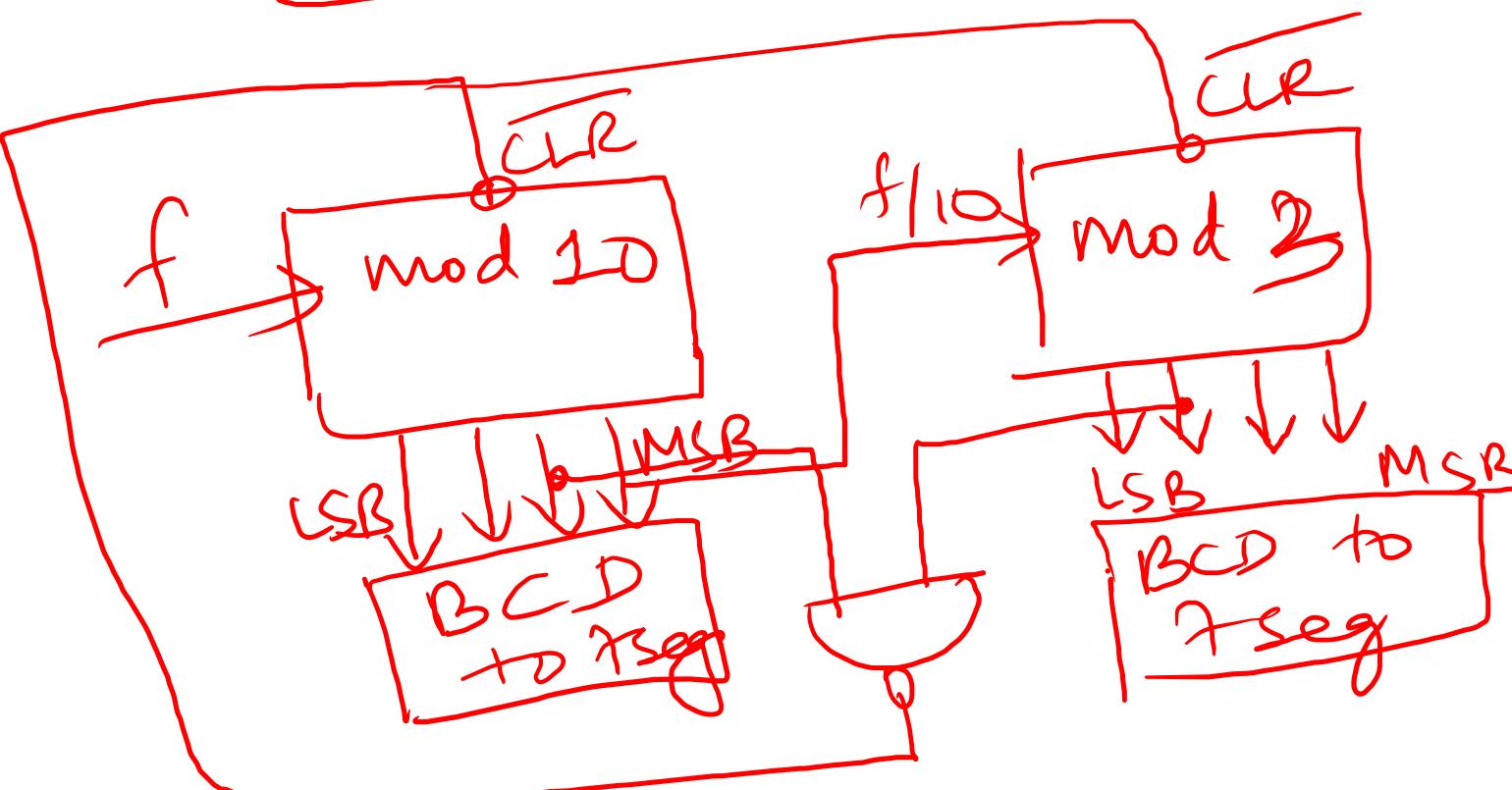


mod 60



$$f/_{10 \cdot 6} = f/_{60}$$

mod 24.



$$\begin{array}{r} 2 \quad 3 \\ 0010 \quad 0011 \end{array}$$

$$\begin{array}{c} \text{Mod } 24 \\ \text{Mod } 3 \\ 0010 \quad 0100 \end{array}$$