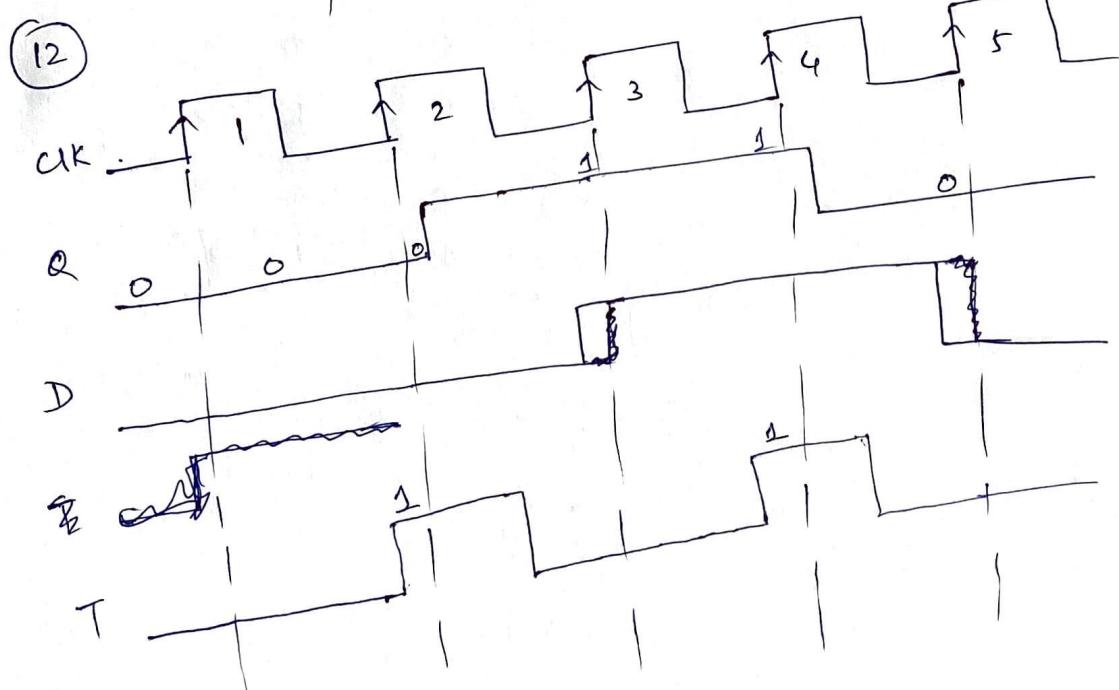
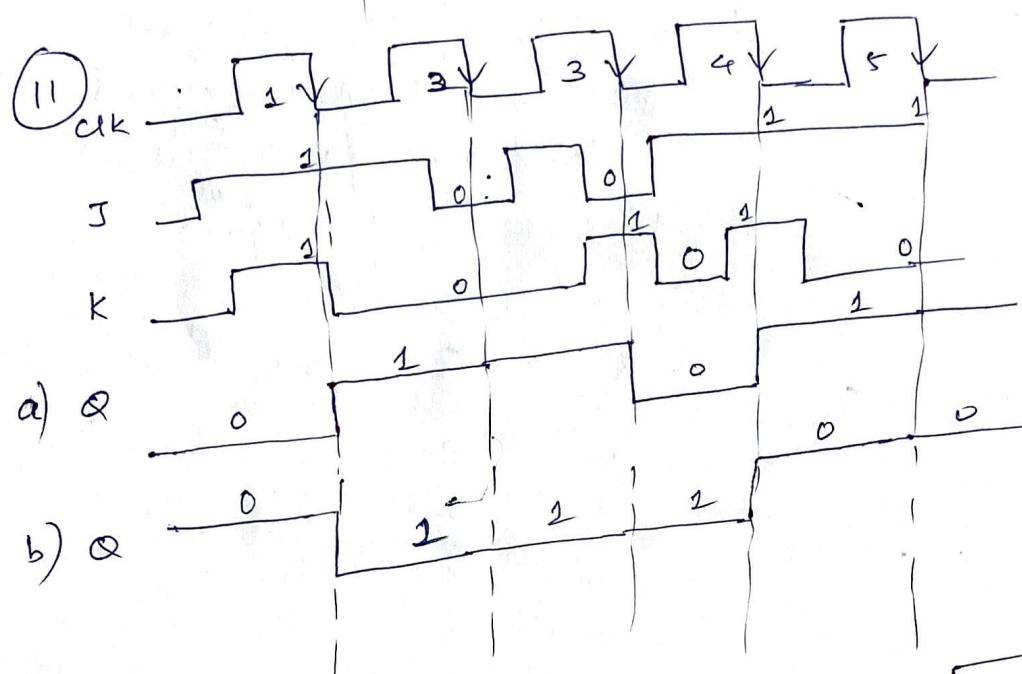
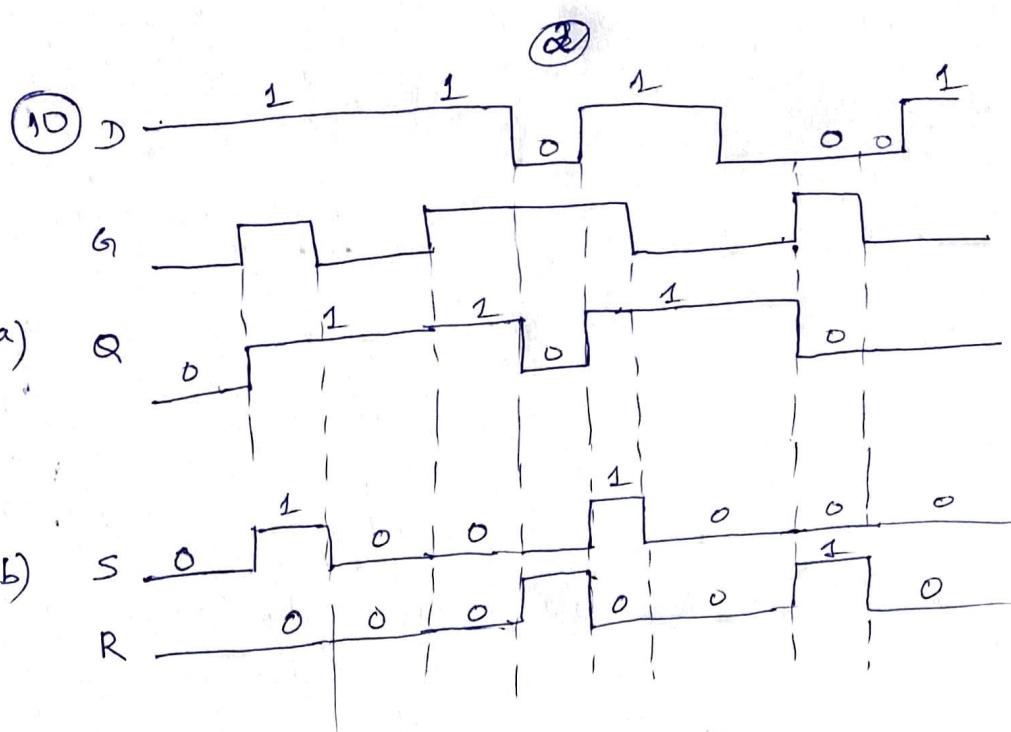


A	B	$Q_t$	$Q_{t+1}$
0	0	0	0 } Reset
0	0	1	0 }
0	1	0	0 } Memory
0	1	1	1 }
1	0	0	0 } Memory
1	0	1	1 }
1	1	0	1 } Set
1	1	1	1 }

$Q_{t+1}$

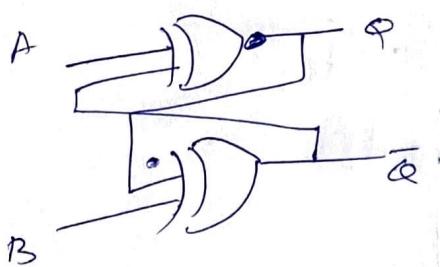
	AB	00	01	11	10
$Q_t$	0	0	0	1	0
0	0	0	1	0	0
1	0	1	1	1	1

$$\begin{aligned}
 Q_{t+1} &= AB + Q_t B + Q_t^A \\
 &= AB + Q_t (A+B)
 \end{aligned}$$

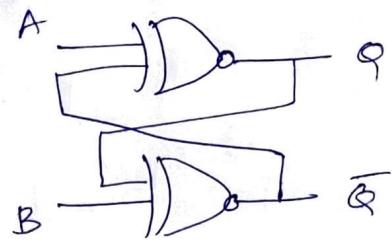


The cipss should  
be stable  
before the  
active edge  
of clock  
arrive

(13)



A	B	$Q_t$	$Q_{t+1}$
0	0	0	X
0	0	1	X
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

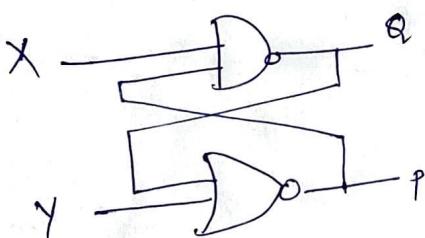


A	B	$Q_t$	$Q_{t+1}$
0	0	0	X
0	0	1	1

$AB = 00$  corresponds to memory state in SR latch.

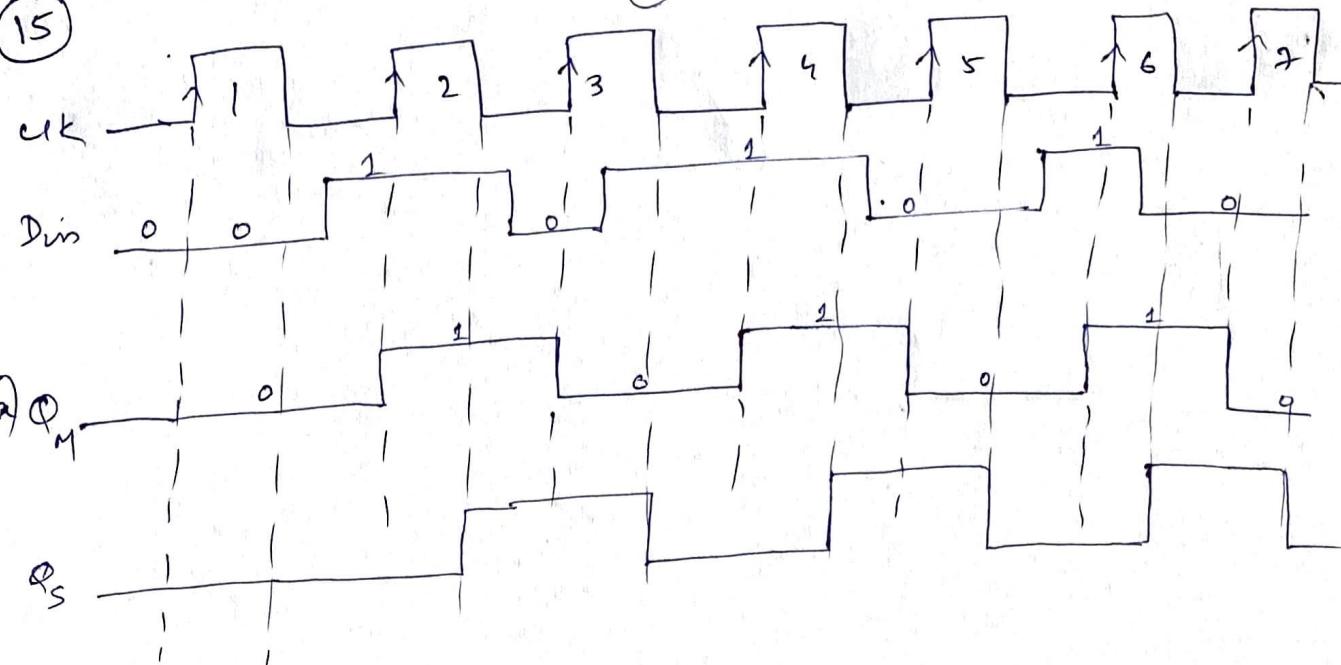
Since the condition is not satisfied in EXOR & EXNOR based cross coupled circuits, they don't function as SR latch.

(14)



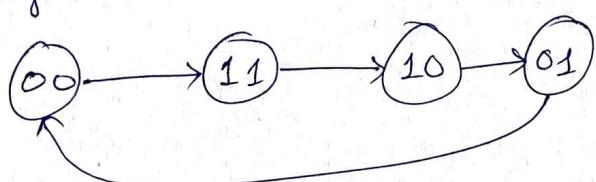
X	Y	$Q$	$Q_{t+1}$	P
0	0	0	1	1
0	0	1	1	0
<hr/>				
0	1	0	1	0
0	1	1	1	0
<hr/>				
1	0	0	0	1
1	0	1	1	0
<hr/>				
1	1	0	1	0
1	1	1	1	0

(15)

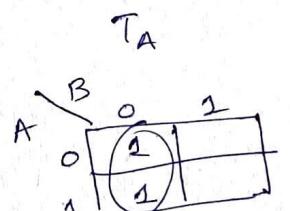


b)  $Q_M$  is active during -ve half of clock  
 $Q_S$  is active during the half cycle.

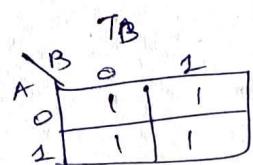
(20) Synchronous 2 bit counter



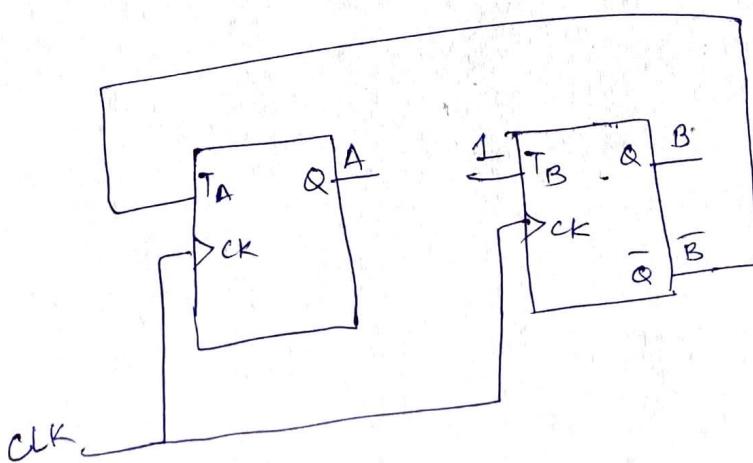
PS	NS	$T_A$	$T_B$
A B	A' B'		
0 0	1 1	1	1
1 1	1 0	0	1
1 0	0 1	1	1
0 1	0 0	0	1



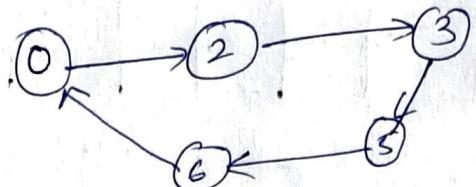
$$T_A = \overline{B}$$



$$T_B = 1$$



21



Excitation table		$J_K$
$Q_t$	$Q_{t+1}$	
0	0	0X
0	1	1X
1	0	X1
1	1	X0

PS

NS

PF c/pS

$A$	$B$	$C$	$A^+$	$B^+$	$C^+$	$J_A$	$K_A$	$J_B$	$K_B$	$J_C$	$K_C$
0	0	0		0	1	0		0	0X	1	X
*	*	*		0	0	0		0	X	X	0
0	1	0		0	1	1		1	X	X	1X
0	1	1		1	0	1		1	X	X	X0
*	*	*		0	0	0		X	0	1	X1
1	0	1		1	1	0		X1		X1	0X
1	1	0		0	0	0					
*	*	*		0	0	0					

$A$	$B$	$C$	$J_A$
0	0	0	X1
1	X	X	X1

$$J_A = C$$

$A$	$B$	$C$	$J_B$
0	0	0	X1
1	X	X	X1

$$J_B = \bar{B} = 1$$

 $J_B K_A$ 

$A$	$B$	$C$	$J_B K_A$
0	0	0	X1
1	X	X	X1

$$K_A = B$$

$$\text{or } K_A = \bar{C}$$

Depending on group

 $K_B$ 

$A$	$B$	$C$	$K_B$
0	0	0	X1
1	X	X	X1

$$K_B = A + C$$

$A$	$B$	$C$	$K_C$
0	0	0	X1
1	X	X	X1

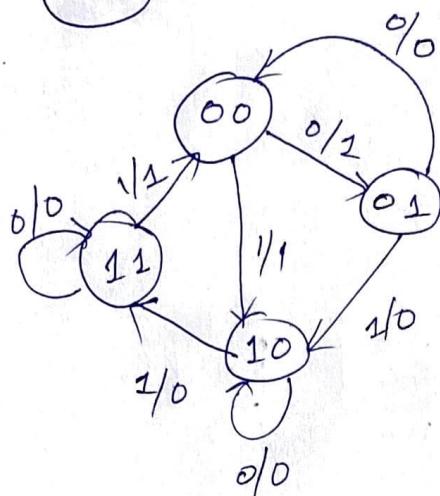
$$K_C = A$$

$A$	$B$	$C$	$J_C$
0	0	0	X1
1	X	X	X1

$$J_C = \bar{A}B$$

Draw the circuit

(22)



(4)

PS	i/P	NS	PP <i>i/Ps</i>	q/P
A	B	X	A <sup>+</sup> B <sup>+</sup>	D <sub>A</sub> D <sub>B</sub>
00	0	01	0 1	1
00	1	10	1 0	1
01	0	00	0 0	0
01	1	10	1 0	0
10	0	10	1 0	0
10	1	11	1 1	0
11	0	11	1 1	0
11	1	00	0 0	1

D<sub>A</sub>

AB	00	01	11	10
X	0	1	1	1
0	1	1	1	1

$$\begin{aligned} D_A &= X\bar{A} + A\bar{B} + \bar{X}A \\ &= X\bar{A} + A(\bar{B} + \bar{X}) \end{aligned}$$

D<sub>B</sub>

AB	00	01	11	10
X	0	1	1	1
1	1	1	1	1

$$\begin{aligned} D_B &= \bar{X}\bar{A}\bar{B} + \bar{X}AB \\ &\quad + XA\bar{B} \\ &= \bar{X}(A \odot B) + XAB \end{aligned}$$

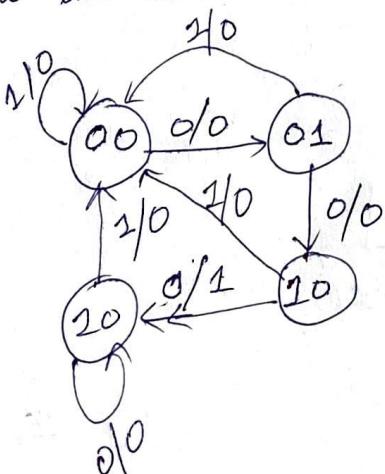
Z

AB	00	01	11	10
X	0	1	1	1
1	1	1	1	1

$$Z = \bar{A}\bar{B} + XAB$$

Draw the circuit

(23)

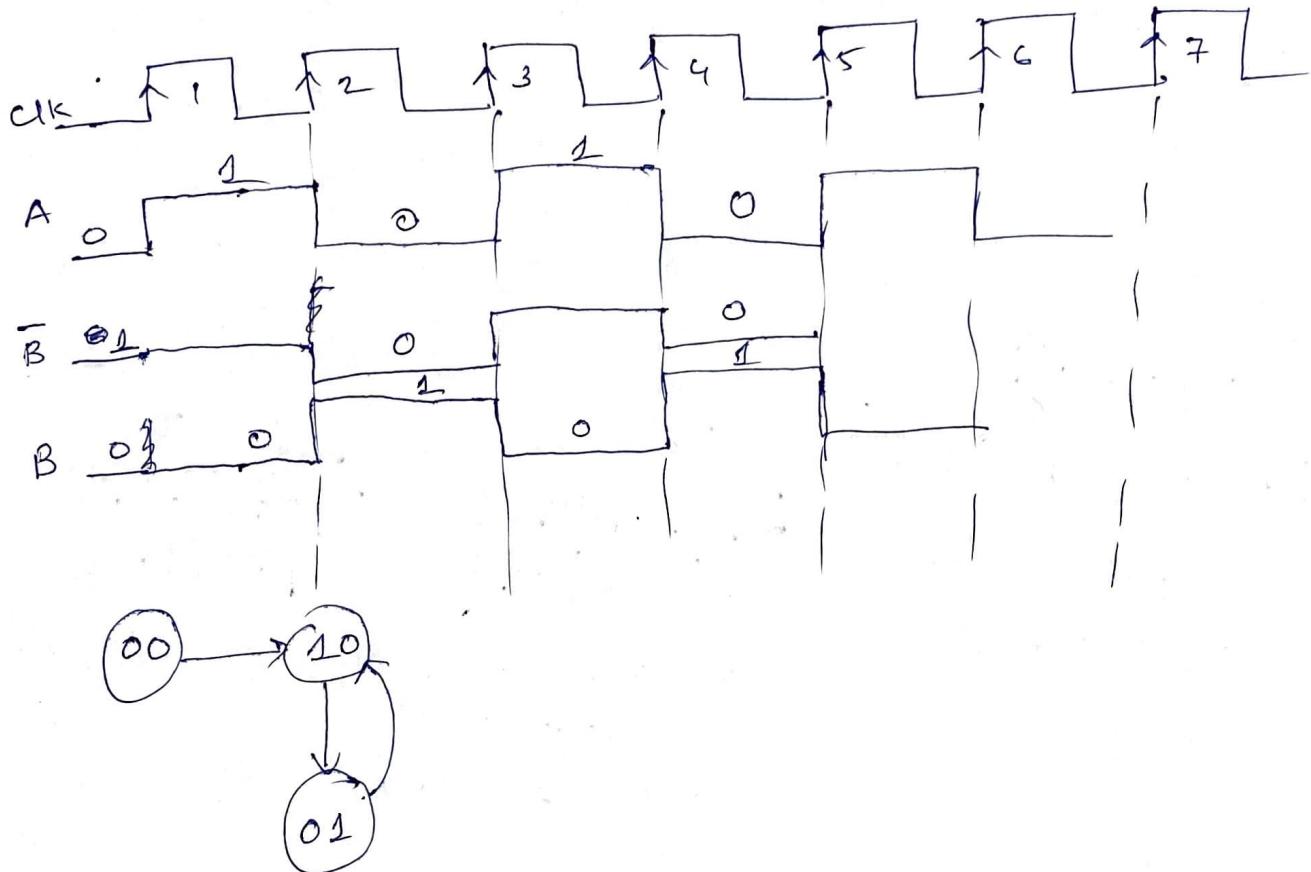
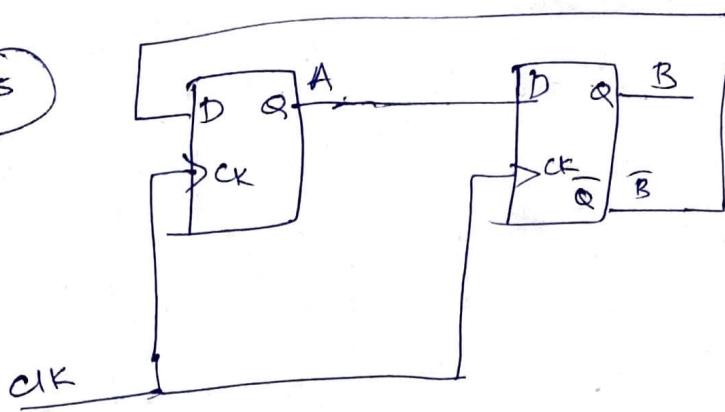


Continue with method given above

(24)

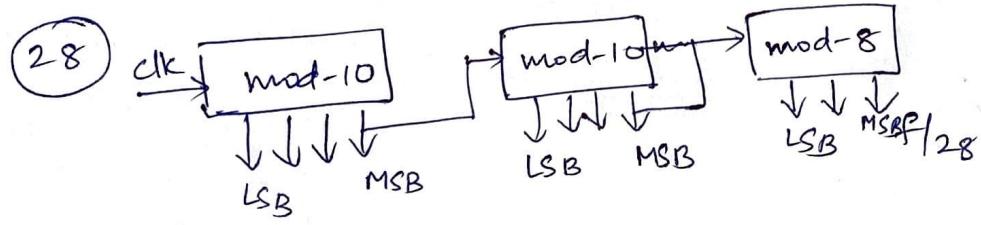
Same method (All are synchronous counters)

25



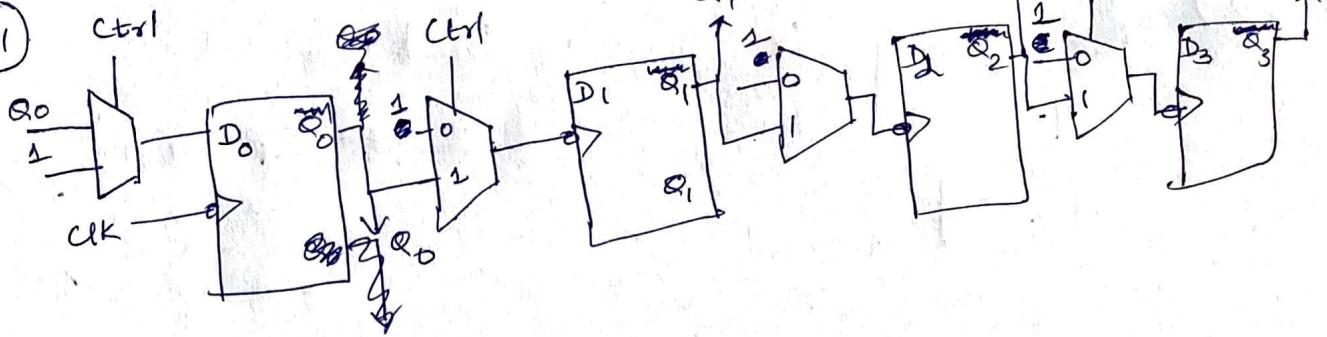
26 Done in class

27 "



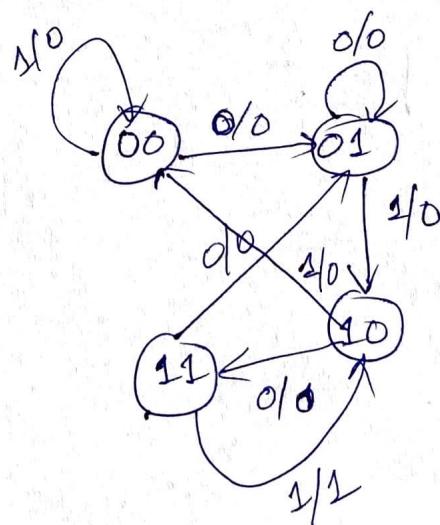
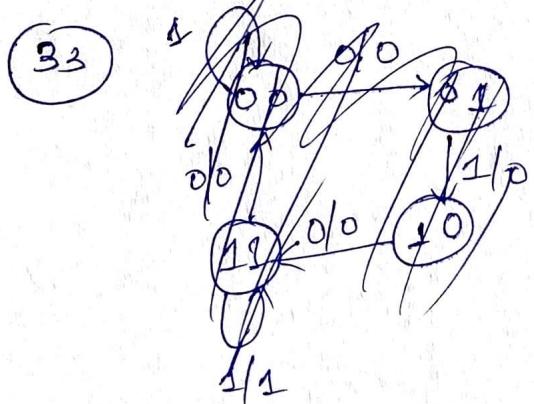
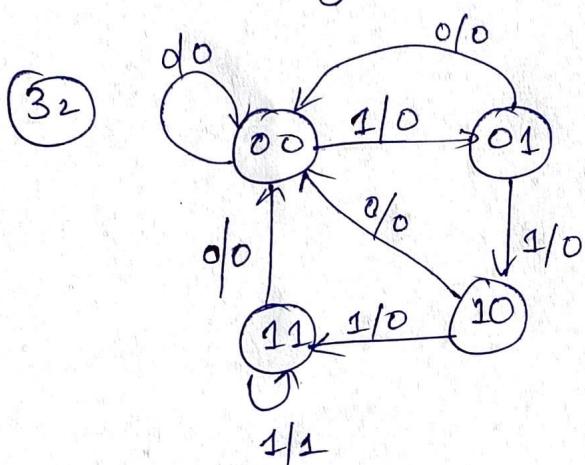
29 a) ~~to~~ connect  $\bar{Q}$  of first ff as clk of next ff & so on

b) connect  $\bar{Q}$  of first ff as clk of next ff & so on



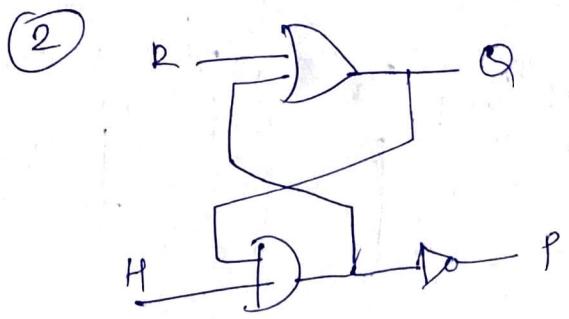
(30) Shift Multiply by 2 is left shift by 1 bit position  
 Divide by 2 is right shift by 1 bit position

b) For 2's complement no.  
 It is a signed no, so MSB should remain unchanged in any shift operation.



### Practice Sheet 5

You need not do Q 12, 13, 14, 15, 16 & 18.  
 It ~~is~~ has not been covered in class.



b) Excitation table

<del>R + H</del>	$Q_t$	$Q_{t+1}$	R	H
0	0	0	0	X
0	1	1	1	1
1	0	0	1	0
1	1	1	1	X

$R \ H \ Q_t \ Q_{t+1}$

00 0 0 { Reset

00 1 0

01 0 0 } Memory

01 1 1

10 0 X

10 1 X

11 0 1 } Set

11 1 1

$Q_{t+1}$	00	01	11	10
$Q_t$	0	0	1	X
R	0	0	1	X
H	0	1	1	X

$$Q_{t+1} = R + Q_t H$$

a) If  $R=1$  &  $H=0$  is not to be used

