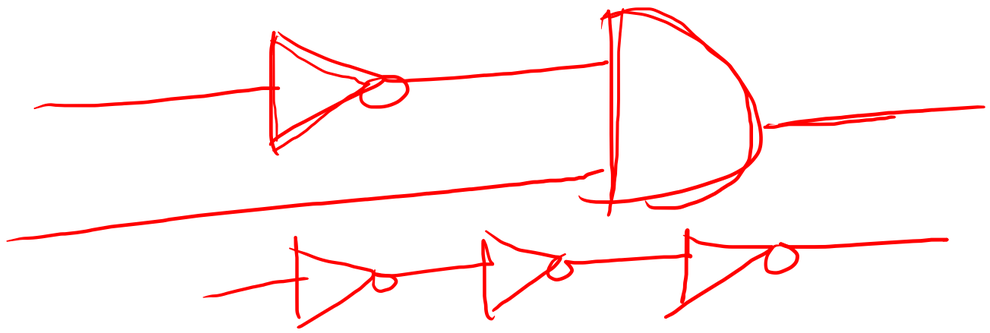
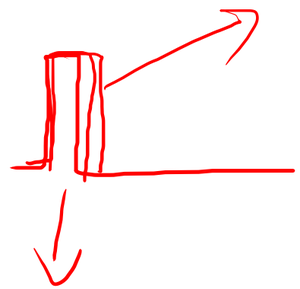
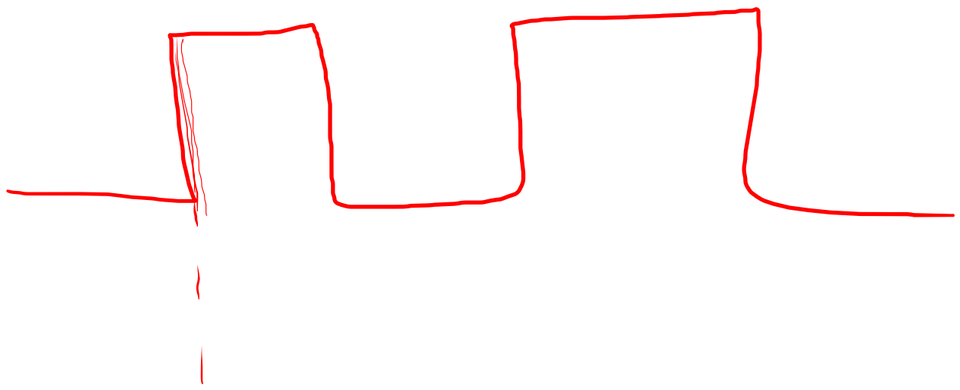
Edge trigger

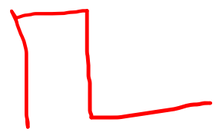




∝ delay of inverter

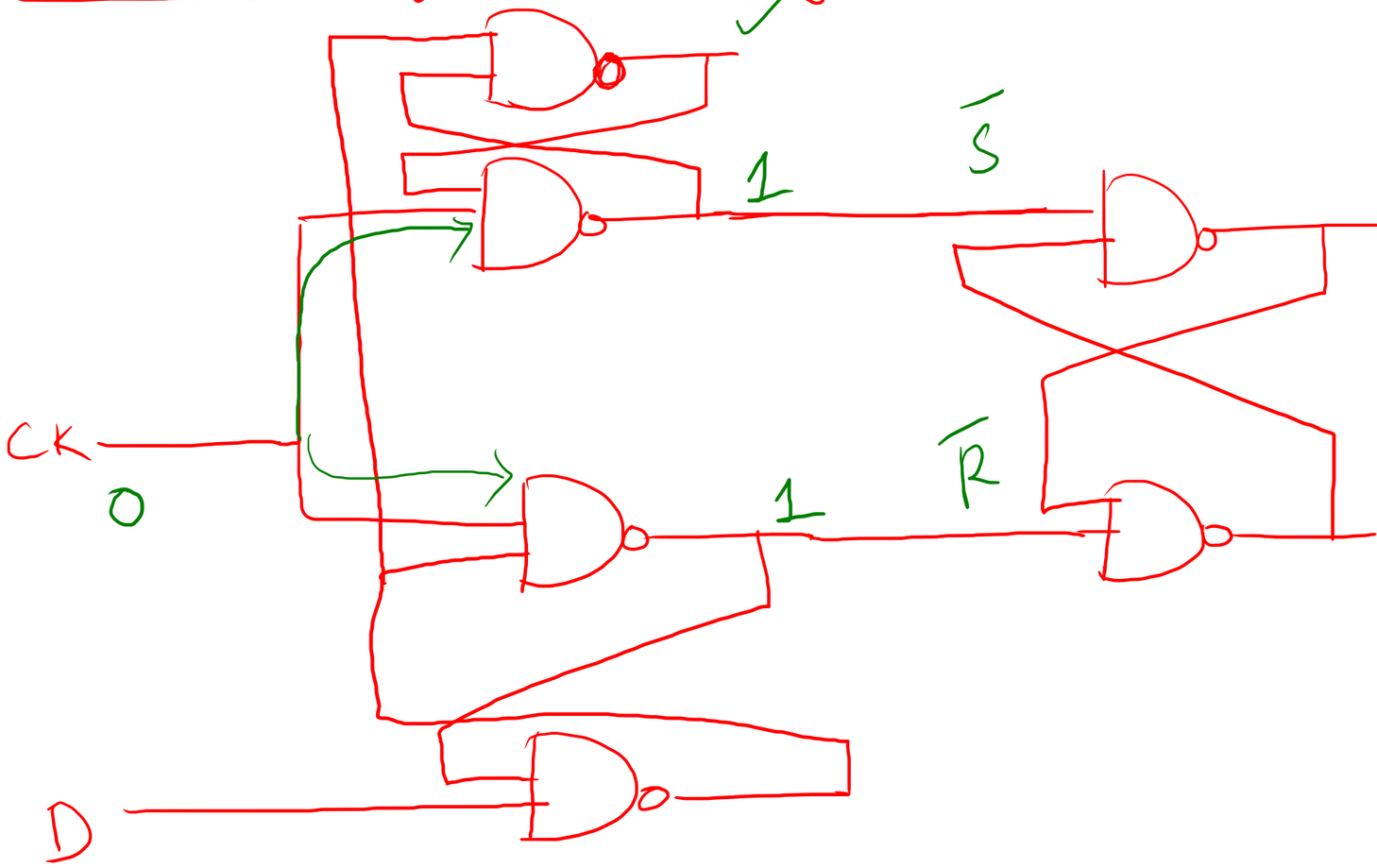
narrow pulse





Positive edge triggered D flipflop

Case 0

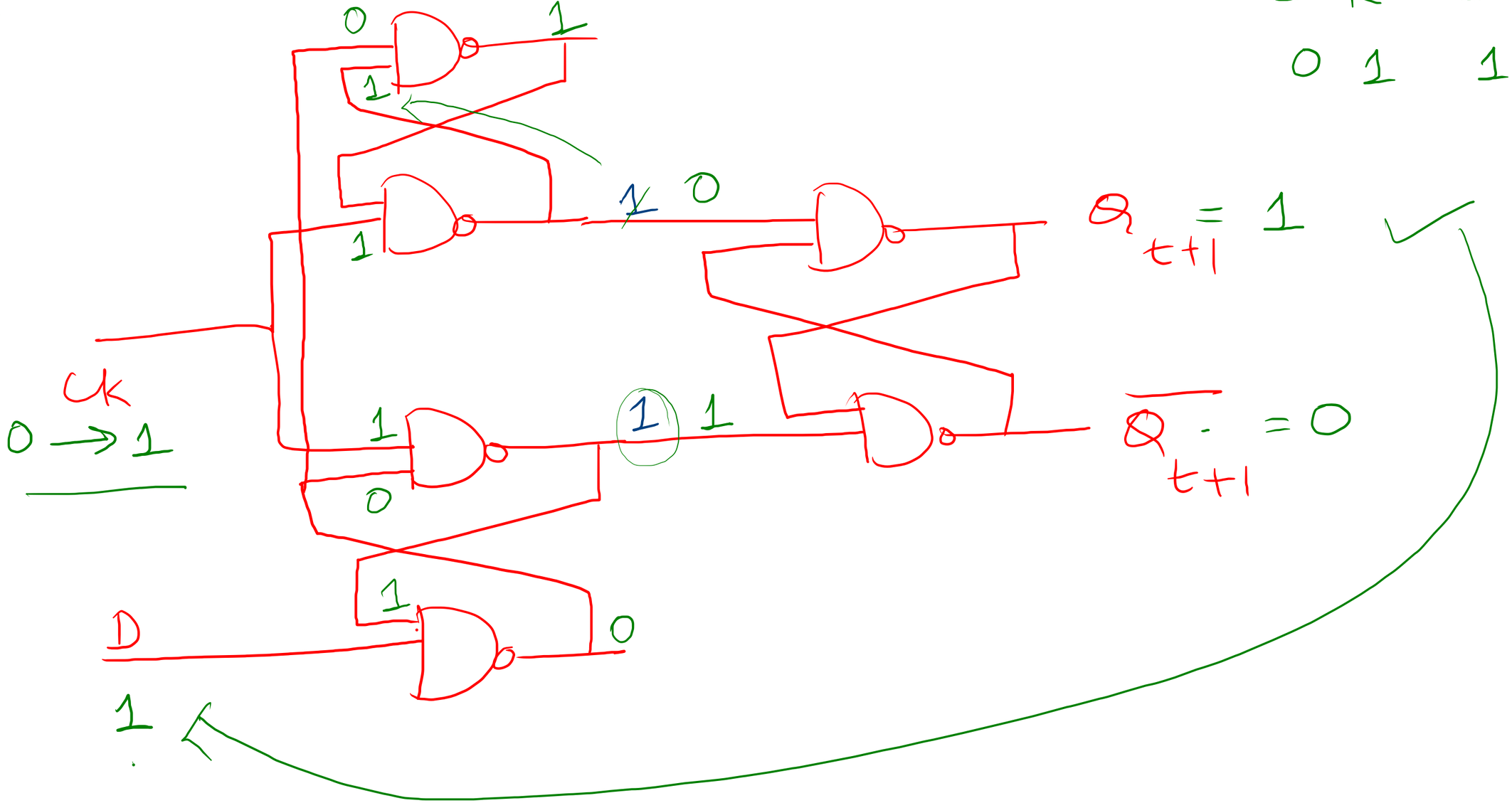


3 cross coupled latches

$\bar{S}$	$\bar{R}$	S R
1	1	0 0

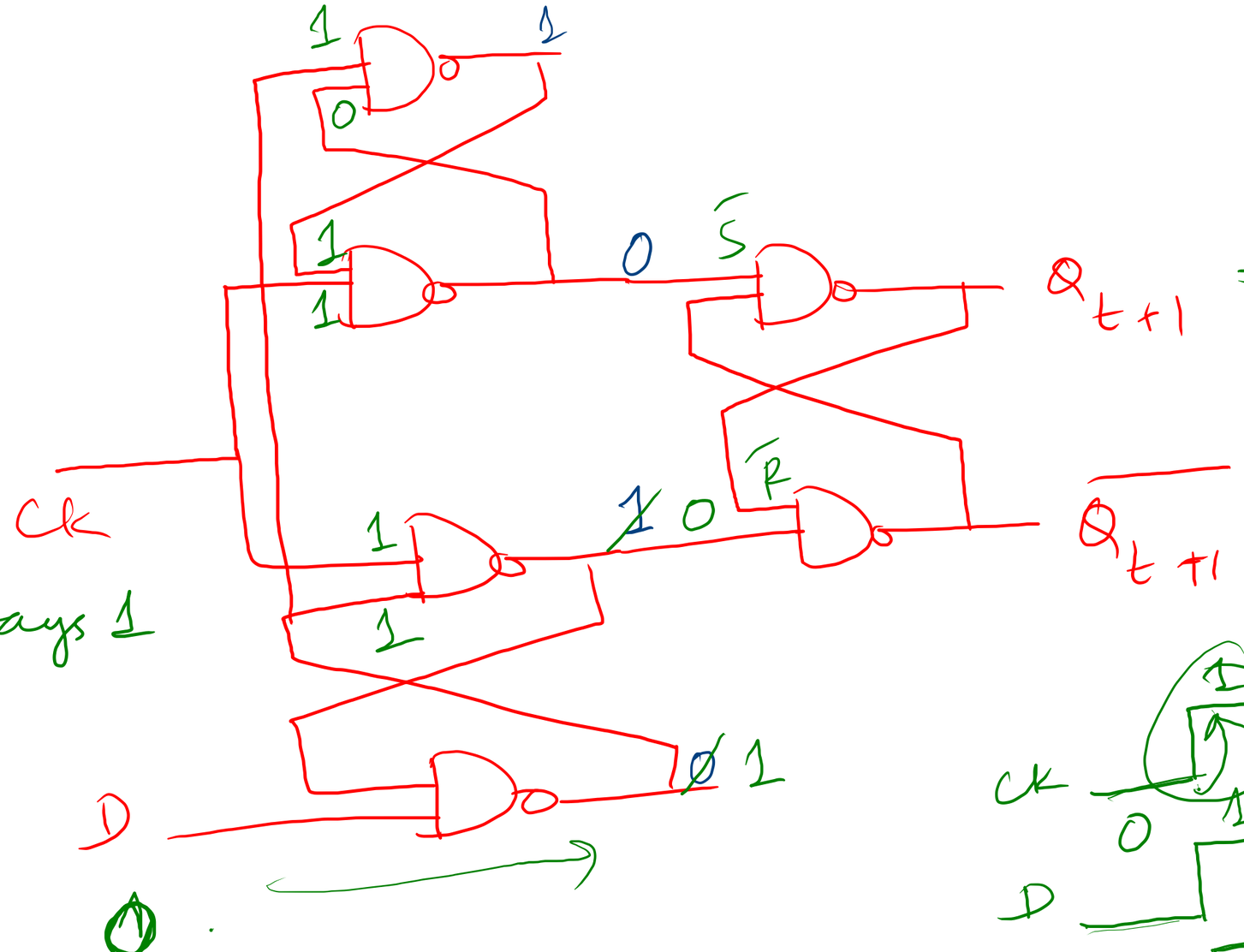
Case 1

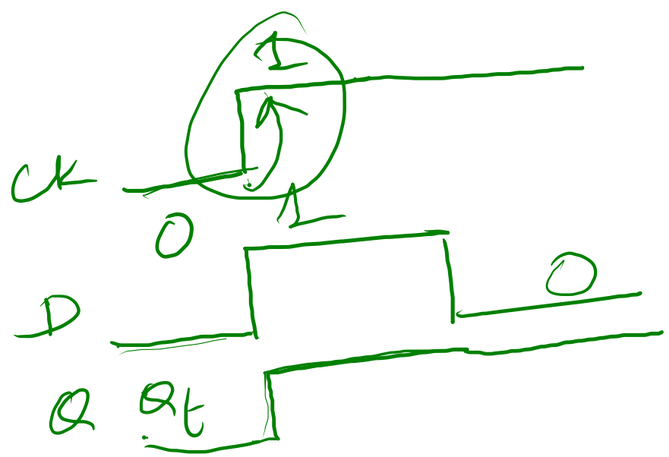
$\bar{S}$	$\bar{R}$	SR	Q_{t+1}
0	1	10	1

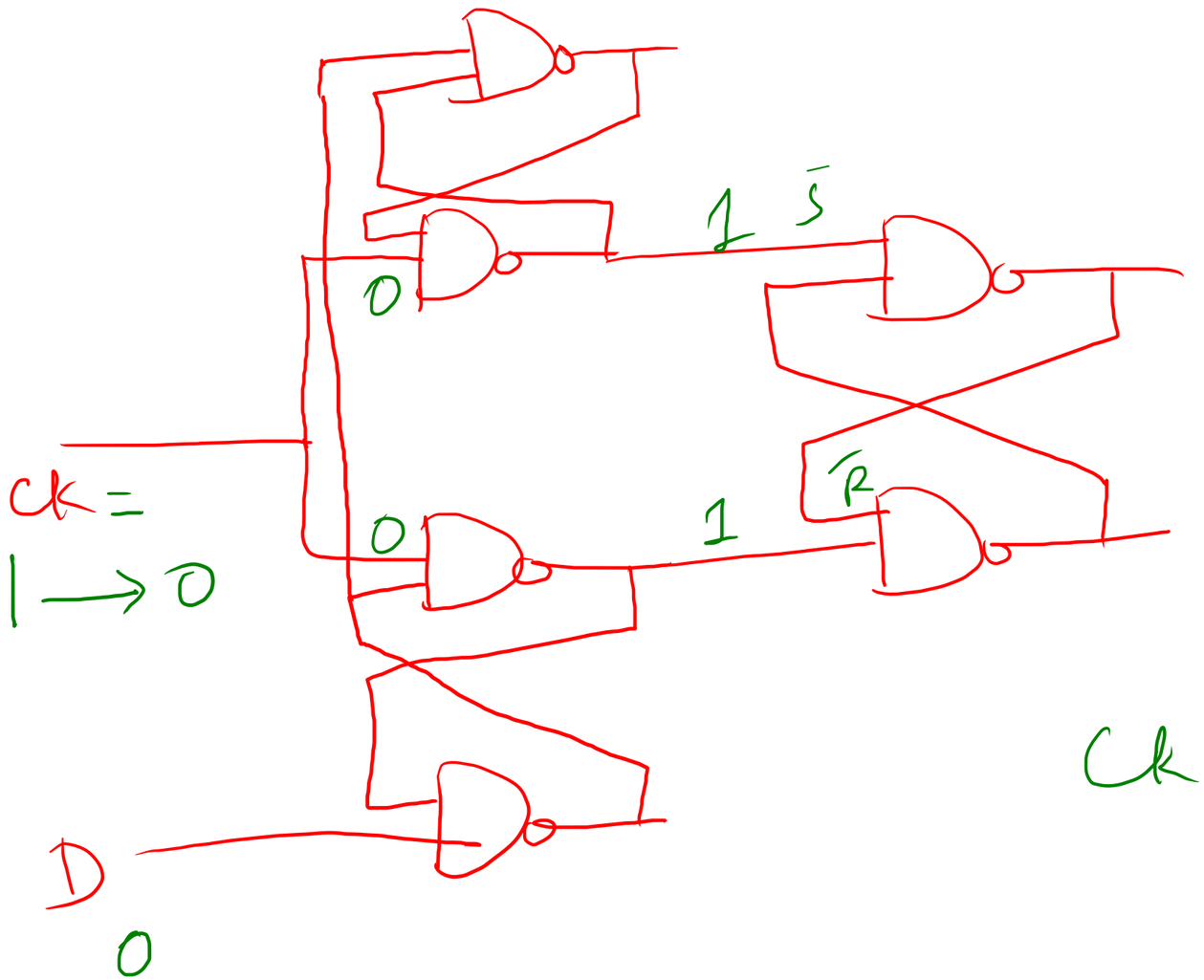


Case 2

$\bar{S}$	$\bar{R}$	SR
0	0	1 1







S	R	Q_{t+1}
0	0	Q_t

$Q_{t+1} = Q_t = 1$

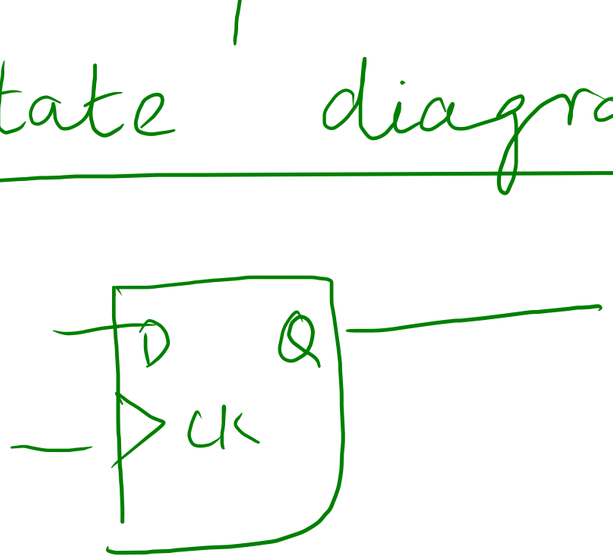
$\overline{Q_{t+1}}$

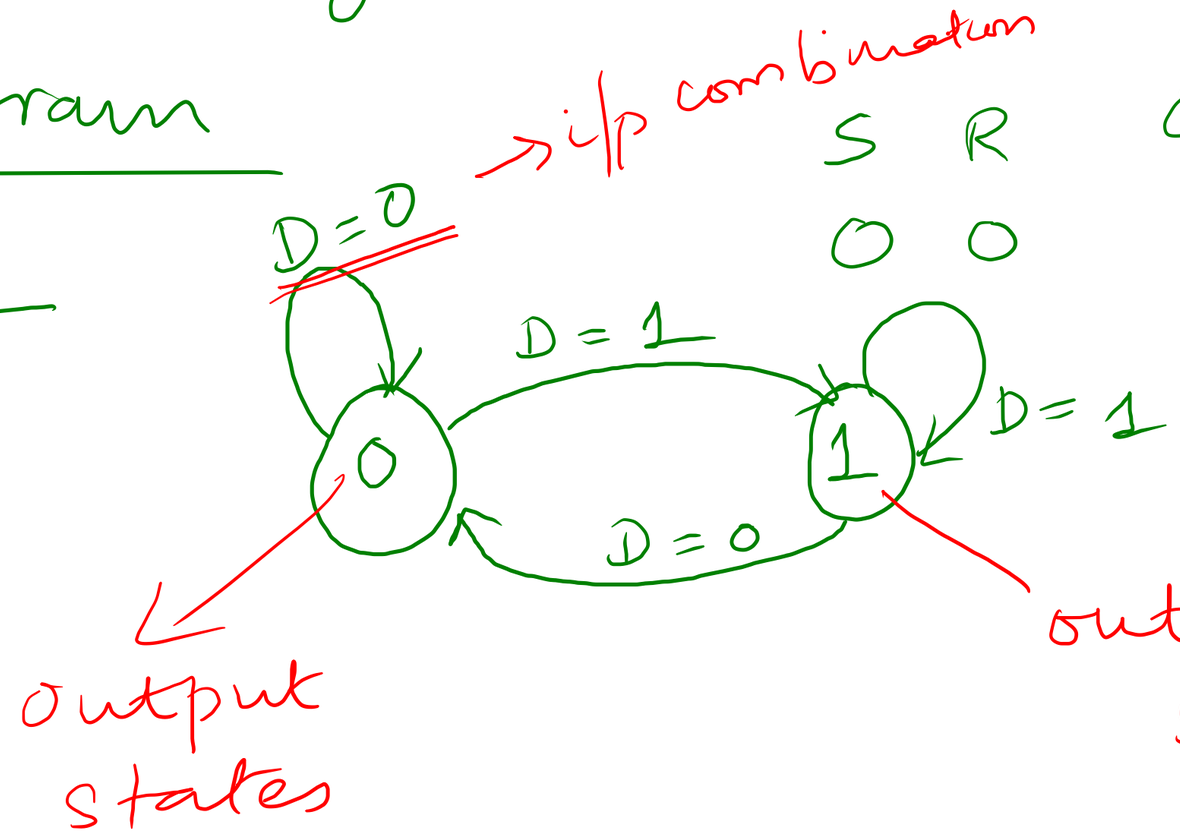
Ckt is not -ve edge triggered

-ve edge triggered ff.

Replace NAND gates with NOR gates

State diagram

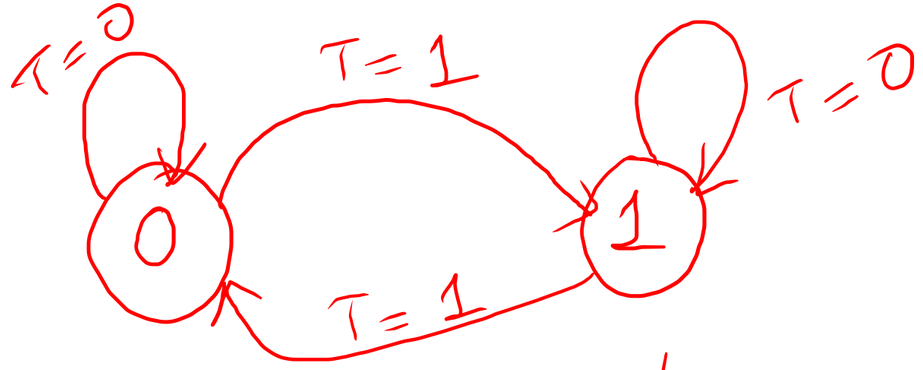




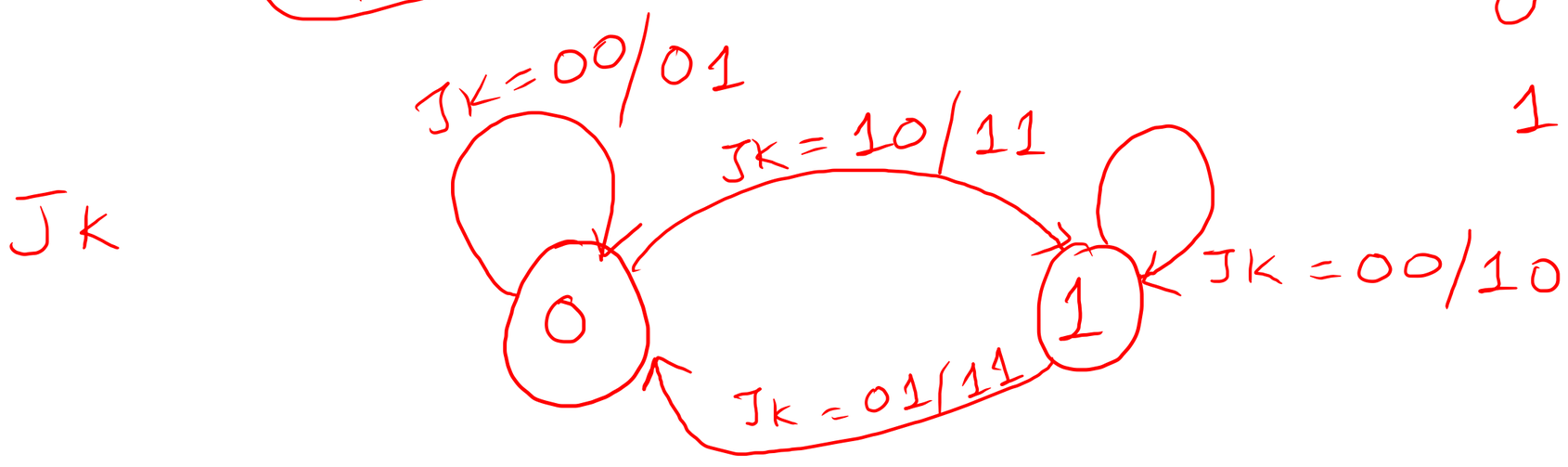
→ i/p combination

S	R	Q_{t+1}	
0	0	Q_t	(NC)

T ff. (Toggle)



Q_t	J K	Q_{t+1}
0	0 0	0
0/1	0 1	0
0/1	1 0	1
0	1 1	1
1	1 1	0



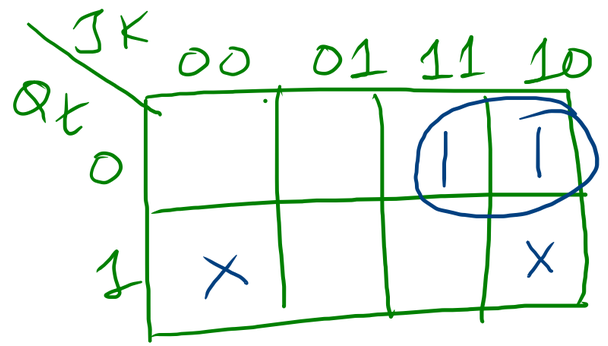
JK

Converting one ff to another

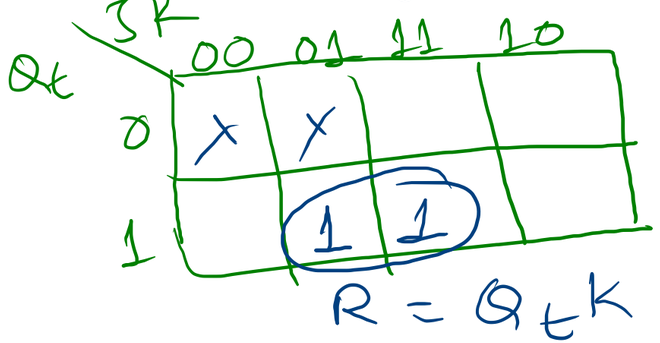
JK using SR

Required FF - JK (write state table for JK)

Q_t	J	K	Q_{t+1}	S	R
0	0	0	0	0	x
0	0	1	0	0	x
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	x	0
1	0	1	0	0	1
1	1	0	1	x	0
1	1	1	0	0	1



$S = \overline{Q}_t J$



$R = Q_t K$

$Q_t = 0$

$Q_{t+1} = 0$

S R

0 0 } 0 X

0 1 }

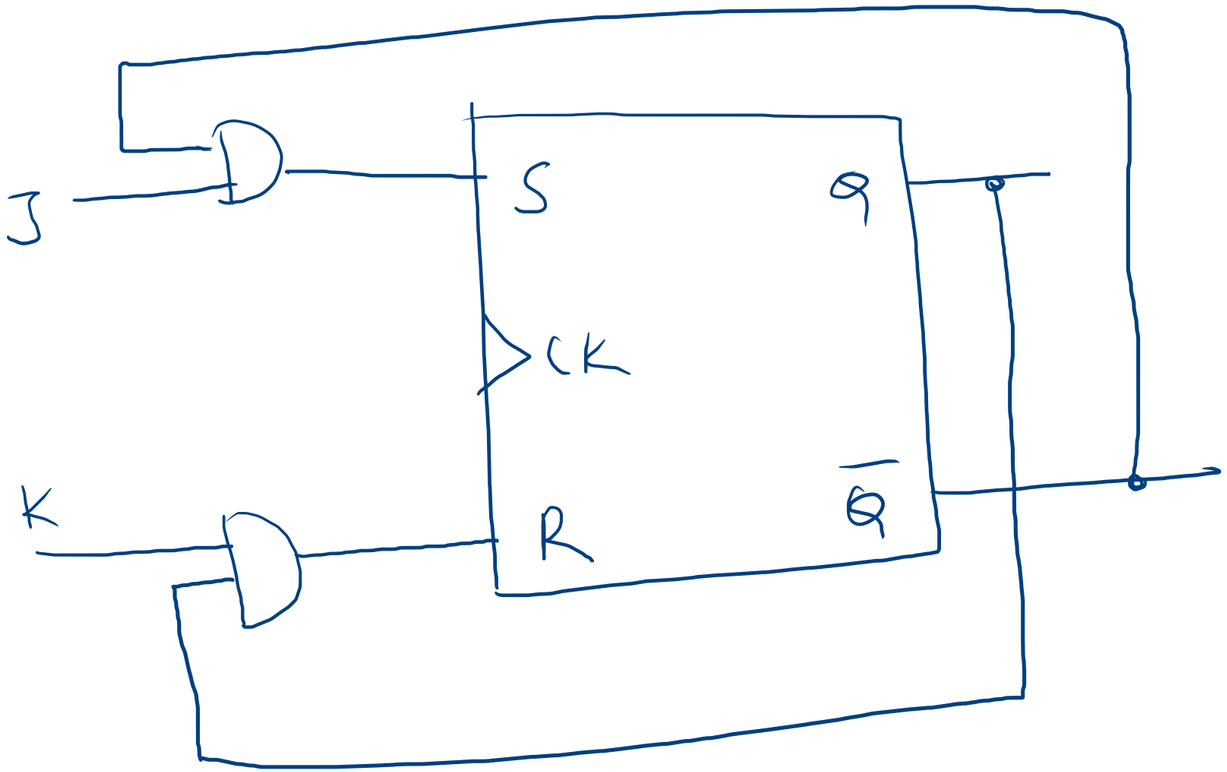
$Q_t = 0$, $Q_{t+1} = 1$

SR = 10

1 1

SR = 00 } X0

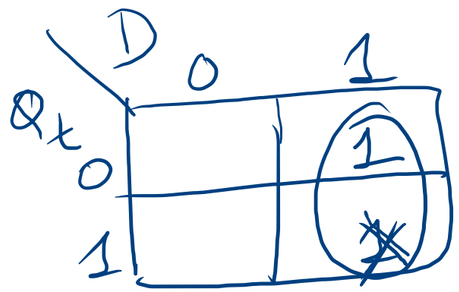
SR = 10 }


J
S
Q
CK
K
R
$\overline{Q}$

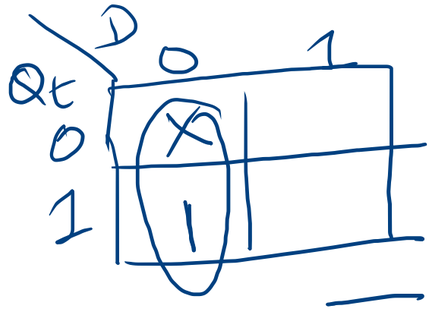
D using SR ff.

Q_t	D	Q_{t+1}	SR
0	0	0	0 X
0	1	1	1 0
1	0	0	0 1
1	1	1	X 0

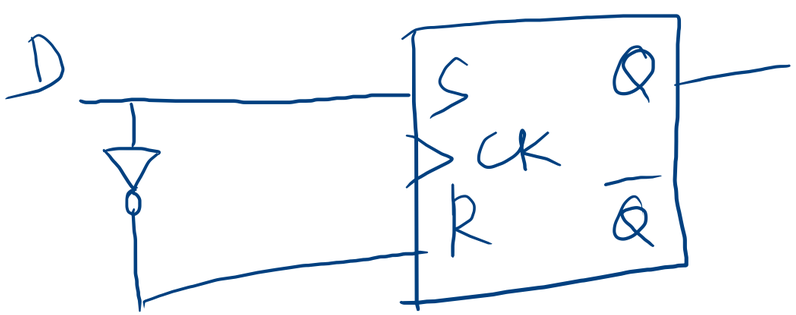
S



$S = D$



$R = \overline{D}$



Q_t	Q_{t+1}	SR
0	0	0 0 0 1 } 0X
0	1	1 0
1	0	0 1
1	1	0 0 1 0 } X0

SR using JK ff

Q_t	S	R	Q_{t+1}	J	K
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	X
0	1	1	X	X	X
1	0	0	1	X	0
1	0	1	0	X	1
1	1	0	1	X	0
1	1	1	X	X	X

J

Q_t \ SR	00	01	11	10
0			X	1
1	X	X	X	X

$J = S$

Q_t	Q_{t+1}	JK
0	0	00
		01
0	1	10
		11
1	1	00
		10
1	0	01
		11

JK

00, 01 } 0X

10, 11 } 1X

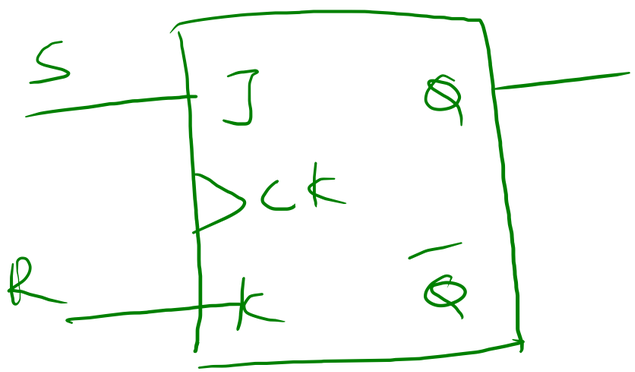
00, 10 } X0

01, 11 } X1

K

Q_t \ SR	00	01	11	10
0	X	X	X	X
1		1	X	

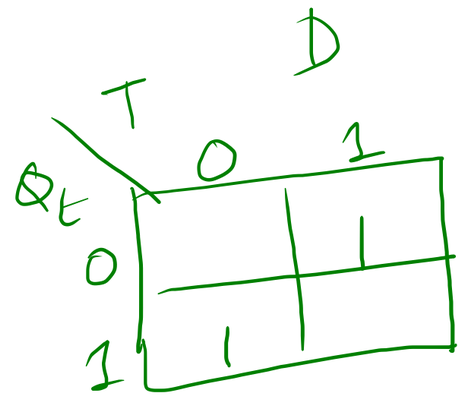
$K = R$



SR ff is a subset of JK ff.

T using D ff

Q_t	T	Q_{t+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0



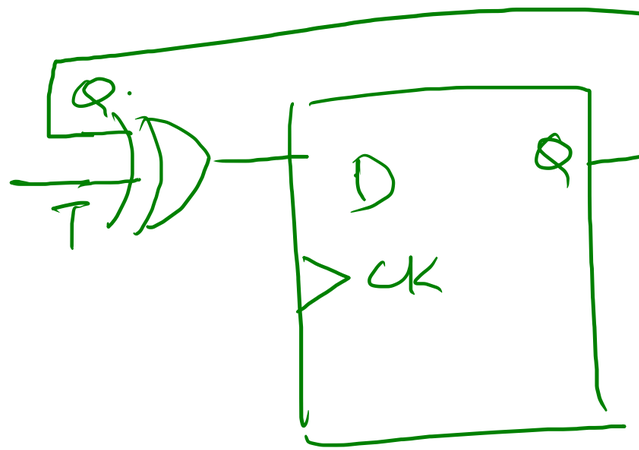
$$D = \bar{Q}_t T + Q_t \bar{T}$$

$$= Q_t \oplus T$$

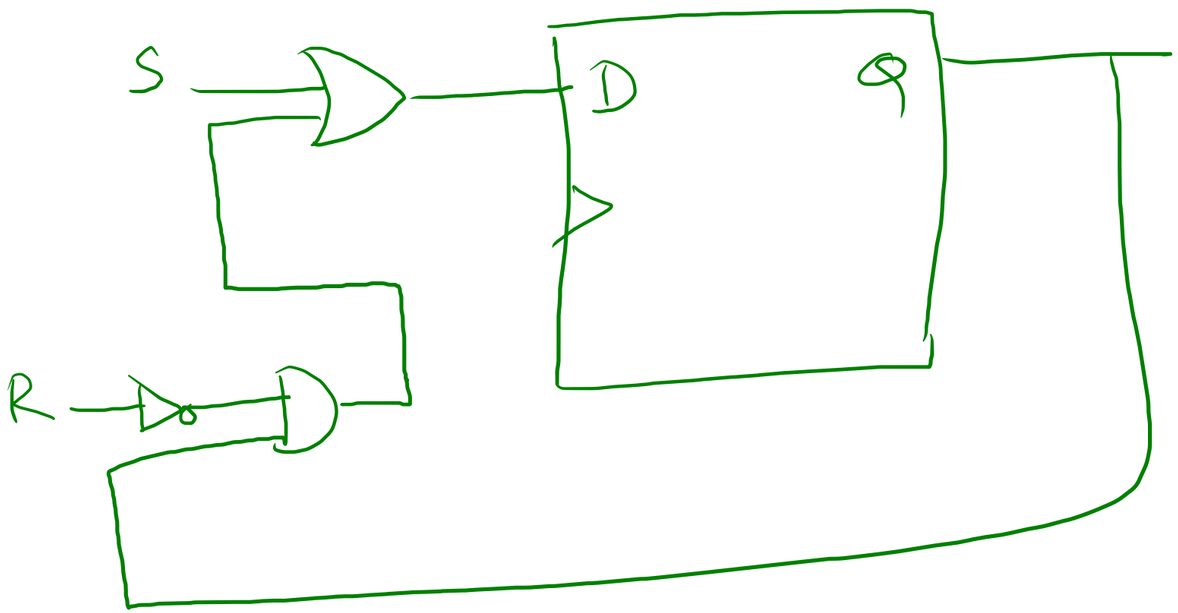
$T = 1$

$$Q_{t+1} = \bar{Q}_t$$

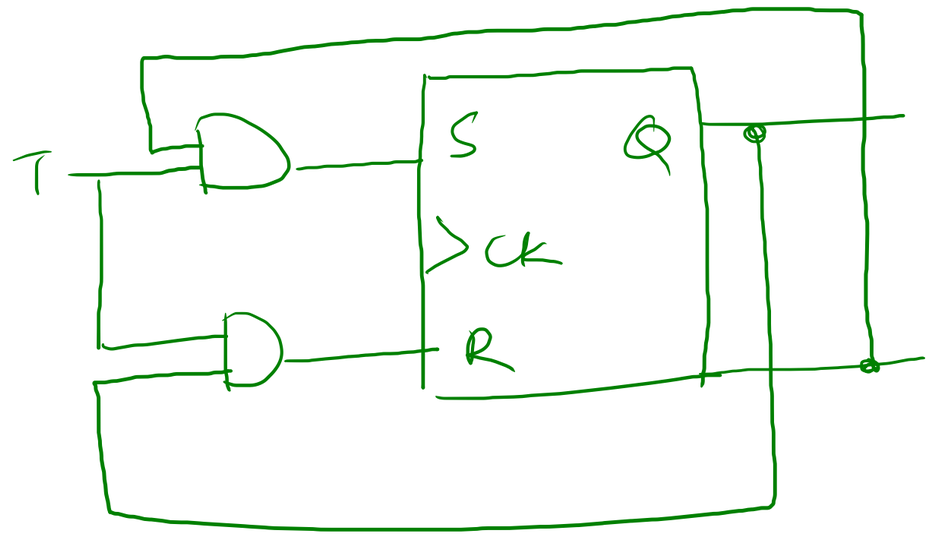
$Q_t = 0 \quad Q_{t+1} = 0$



SR using D ff



T using SR ff
(SR ff to T ff)

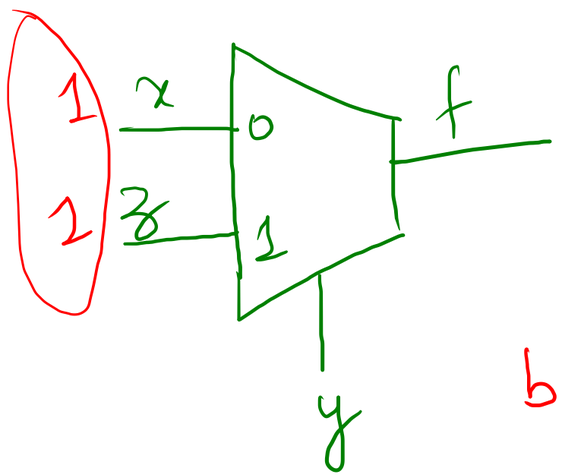


Glitches.

↓

can happen (Hazards) in combinational ckts as well.

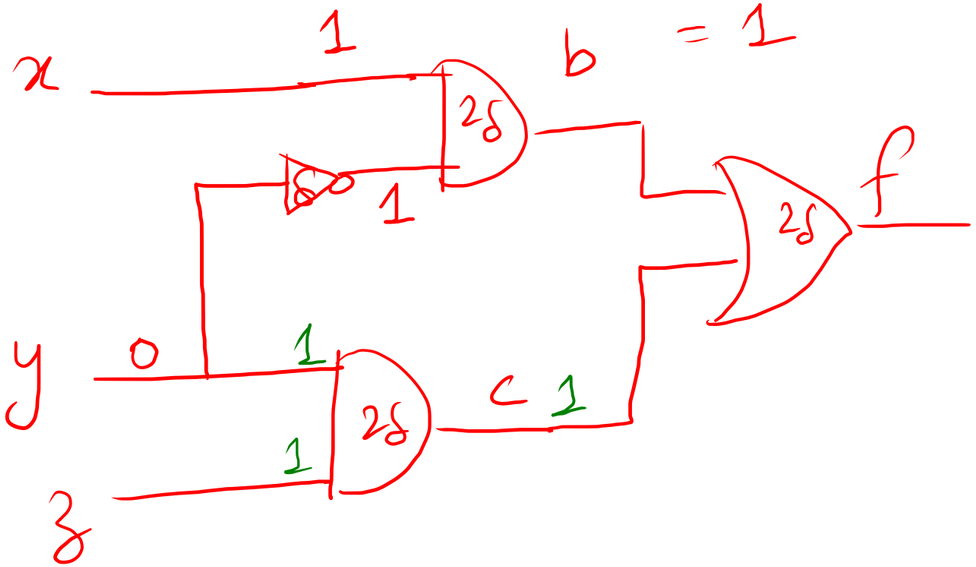
Dynamic hazard

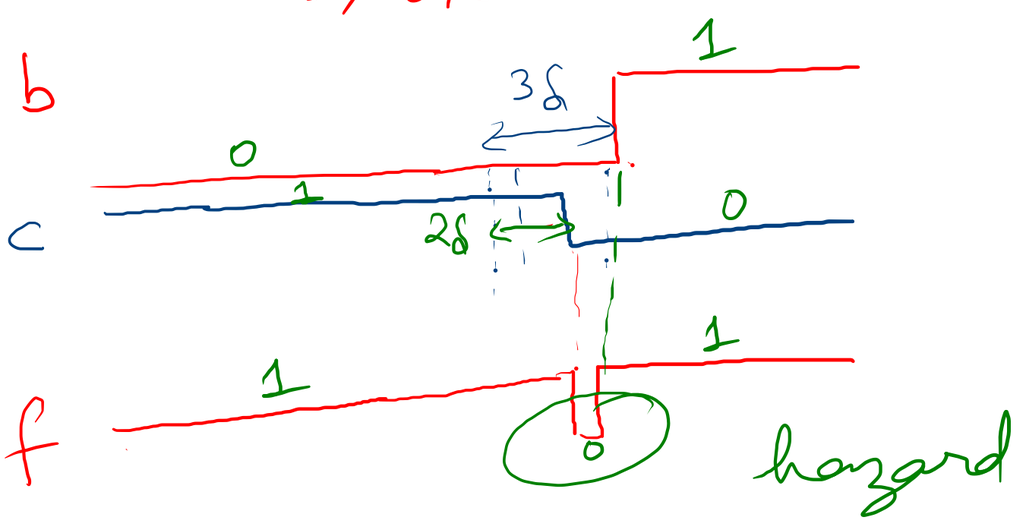


$f = x\bar{y} + zy$

Inverter δ (delay)

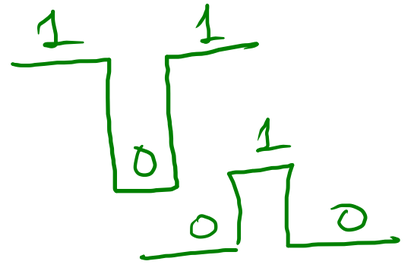
AND, OR - 2δ





Static 1 hazard

Static 0 hazard



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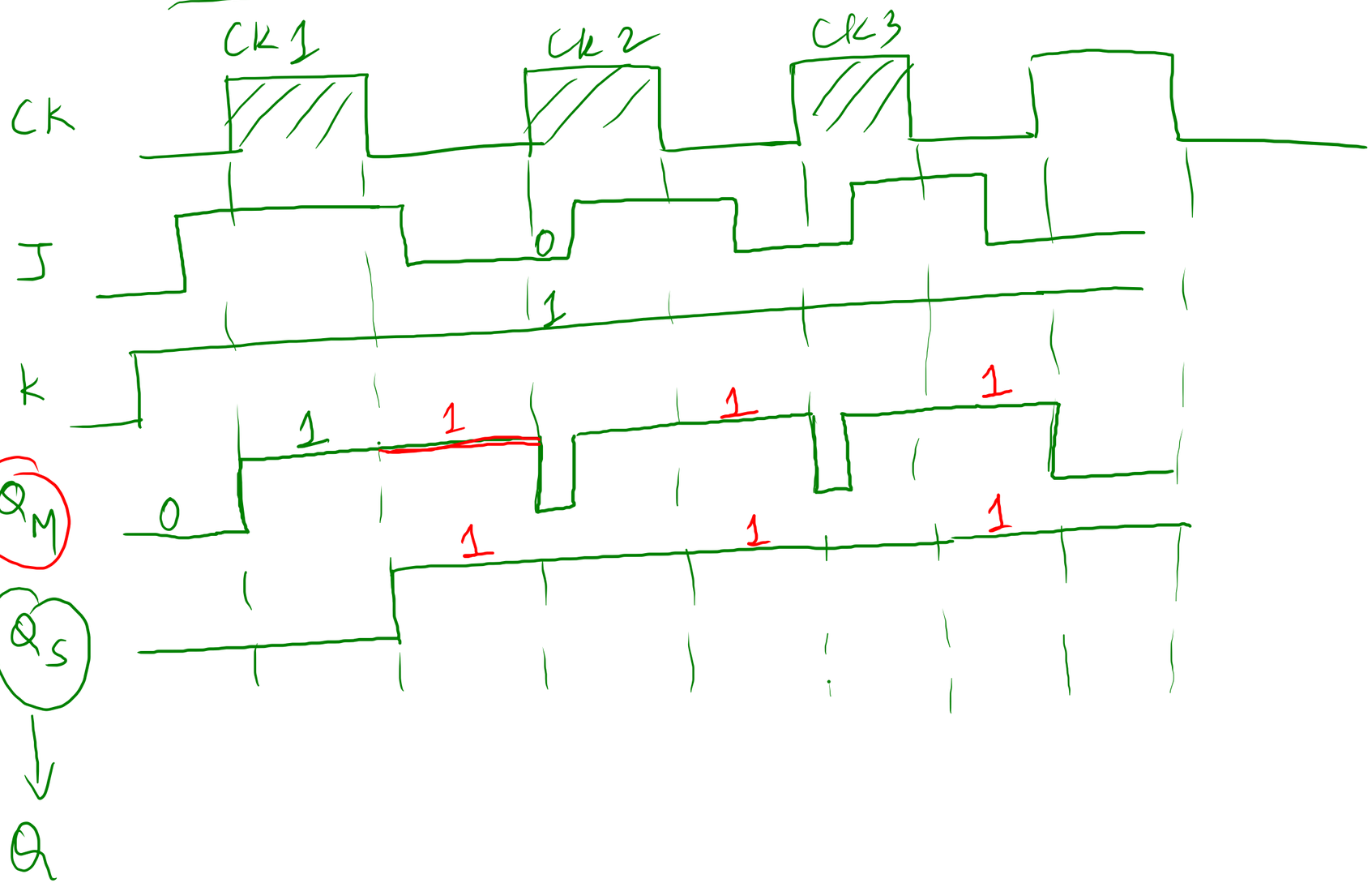
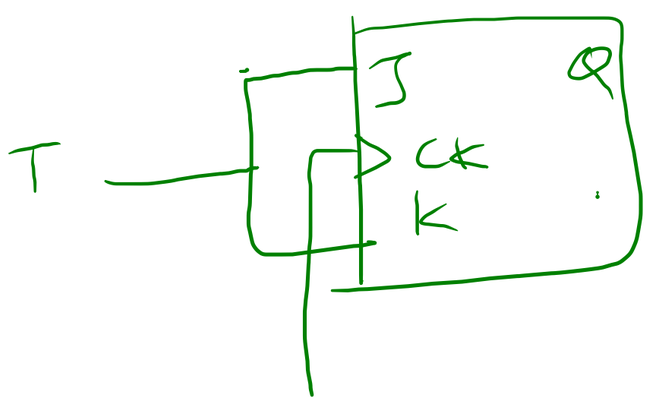
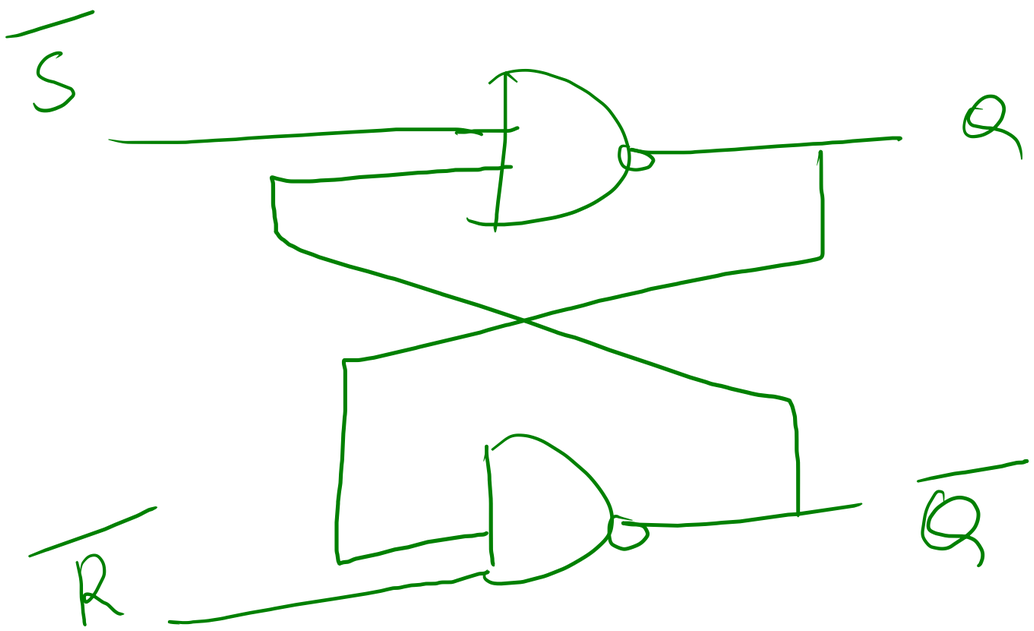
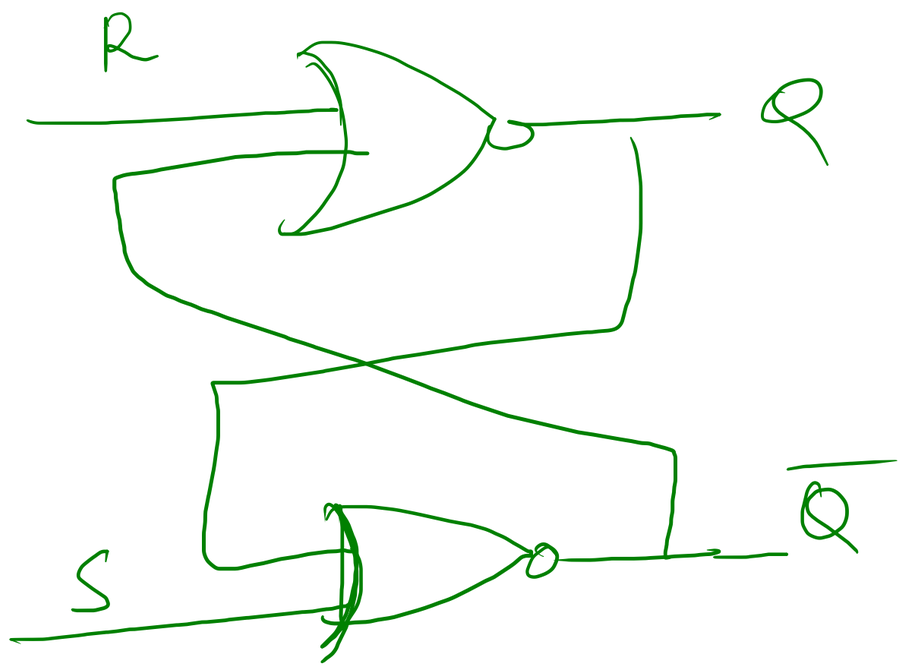


T using JK ff




S
Q
R
Q


R
Q
S
Q