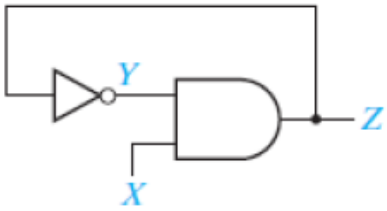
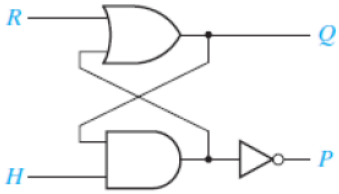
PRACTICE SHEET 6

Latches, Flip flops, Synchronous and Asynchronous Sequential Circuits

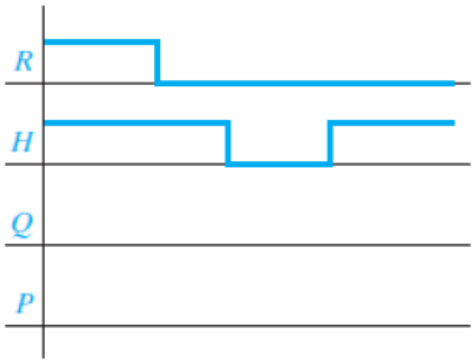
1. Assume that the inverter in the given circuit shown below has a propagation delay of 5 ns and the AND gate has a propagation delay of 10 ns. Draw a timing diagram for the circuit showing the response for Z, given that the timing transitions for X and Y are specified. Assume that X is initially at logic 0, after 10 ns X becomes 1 for 80 ns, and then X is 0 again. Y is initially at logic 1, transitions to 0 at t = 25 ns, transitions to 1 at t = 40 ns, transitions to 0 at t = 55 ns, transitions to 1 at t = 70 ns, transitions to 0 at t = 85 ns, and transitions to 1 at t = 100 ns. Your timing diagram must depict all the signals X, Y and Z and the time instants very clearly.



2. A latch can be constructed from an OR gate, an AND gate, and an inverter connected as shown below

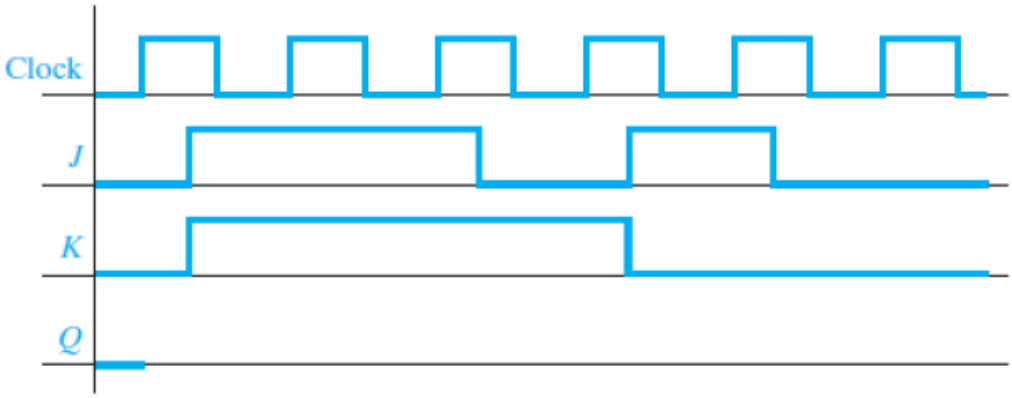


(a) What restriction must be placed on R and H so that P will always equal Q′ (under steady-state conditions)?
(b) Construct the characteristic table, excitation table, truth table and derive the characteristic (next-state) equation along with the state diagram for the latch.
(c) Complete the following timing diagram for the latch.

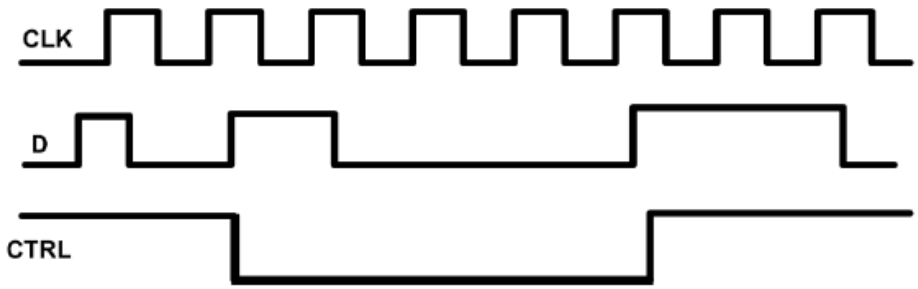


4. A reset-dominant FF behaves like an S-R FF, except that the input S = R = 1 is allowed, and the FF is reset when S = R = 1.
i. Derive the characteristic equation for a reset-dominant FF.
ii. Show how a reset-dominant FF can be constructed by adding gate(s) to an S-R FF.

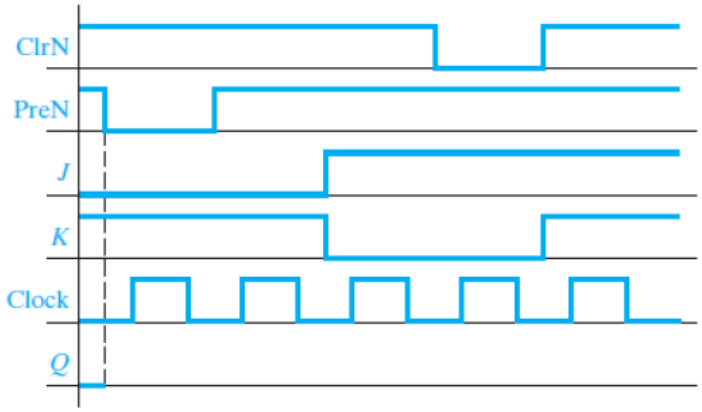
5. Complete the following timing diagram for the positive edge triggered J-K flip-flop given below. It is assumed the initial output Q = 0.



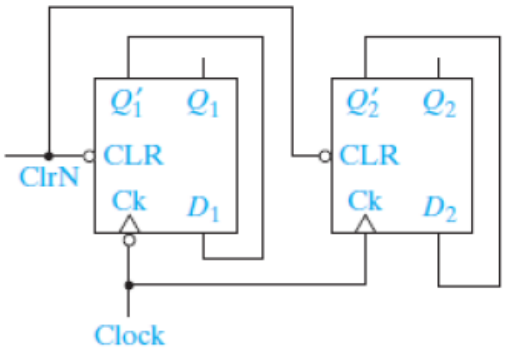
6. Complete the following timing diagram for output Q of a positive edge triggered D-FF assuming the possible scenarios (Assume Q = 0 initially). The FF is clock gated, which derives its clock from the AND-ed operation on CLK and CTRL signals.

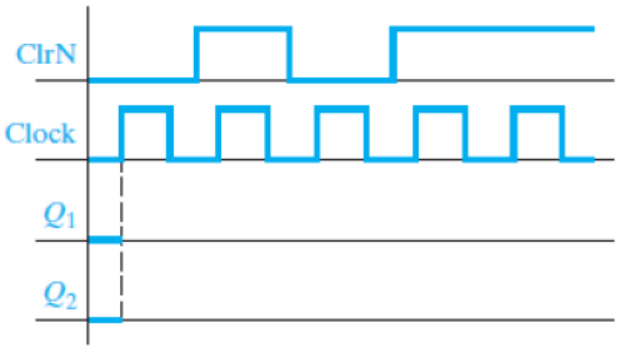


7. (a) Complete the following timing diagram of for a J-K flip-flop with a falling-edge trigger and asynchronous active low ClrN and PreN inputs.

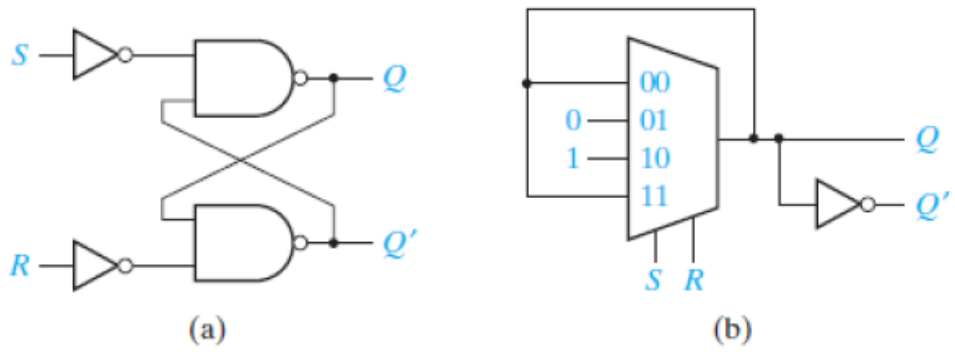


(b) Complete the timing diagram for the following circuit as shown below. Assume Q1 and Q2 begins with 0.



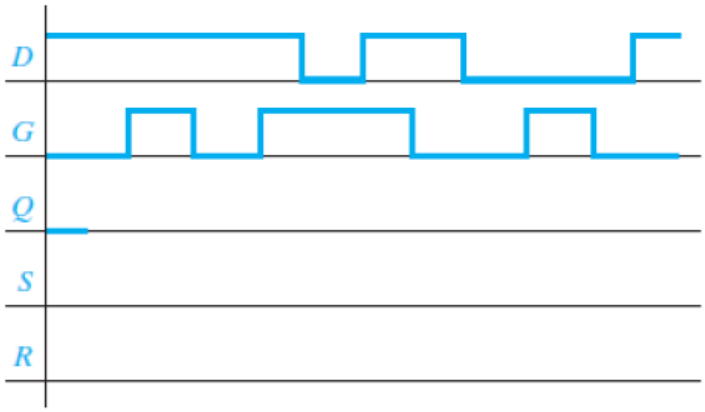


8. Confirm through appropriate justification that each of these circuits given below is an S-R latch. What happens when S = R = 1 for each circuit?

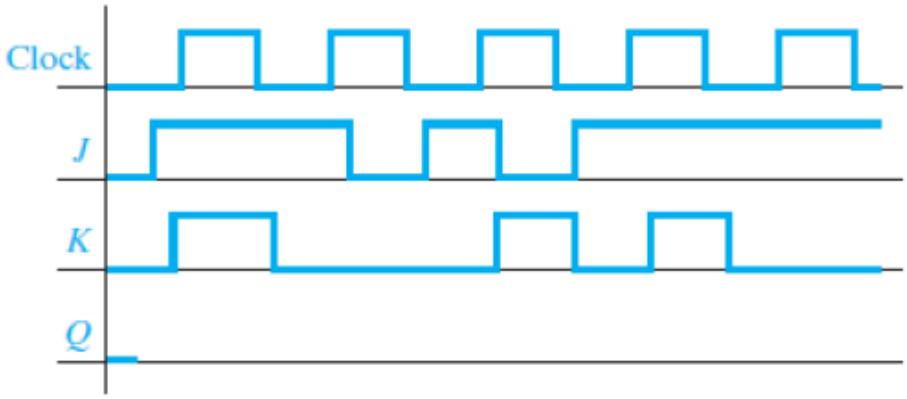


9. An AB latch operates as follows: If A = 0 and B = 0, the latch state is Q = 0; if either A = 1 or B = 1 (but not both), the latch output does not change; and when both A = 1 and B = 1, the latch state is Q = 1.
Construct the truth table and characteristic equation for this AB latch.

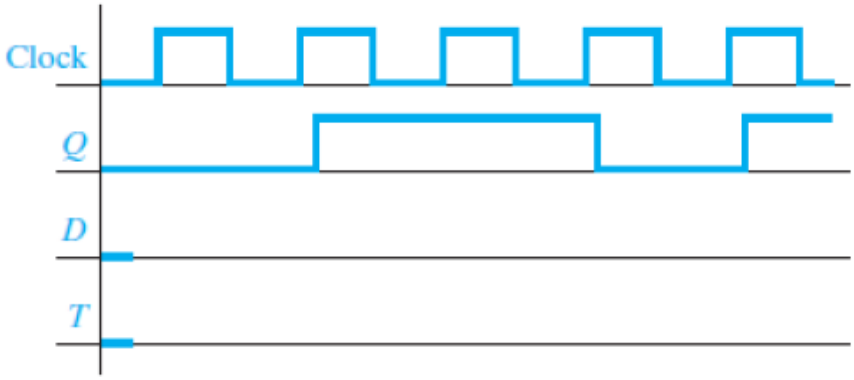
10. Complete the following timing diagram for a gated D latch, with G as the active high gating signal. Assume Q begins at 0.
(a) Trace the waveform for Q based on the behavior of a gated D latch.
(b) Assume the traced output waveform Q to be the output of an S − R latch, gated with the same active high enable signal G. Trace the waveforms of S and R, assuming that they begin at S = R = 0.



11. Complete the timing diagram for a falling-edge-triggered J − K FF for the following two cases:
(a) Assume Q begins at 0.
(b) Assume Q begins at 1.

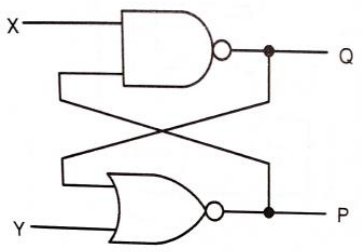


12. Complete the timing diagram by finding the input for a rising-edge-triggered D FF and T FF that would produce the output Q as shown.

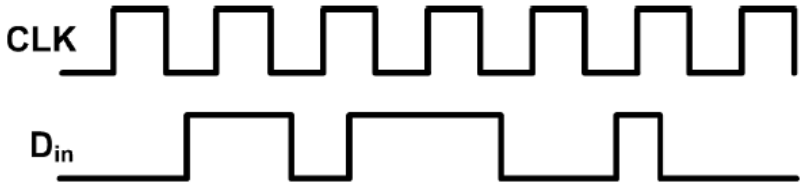


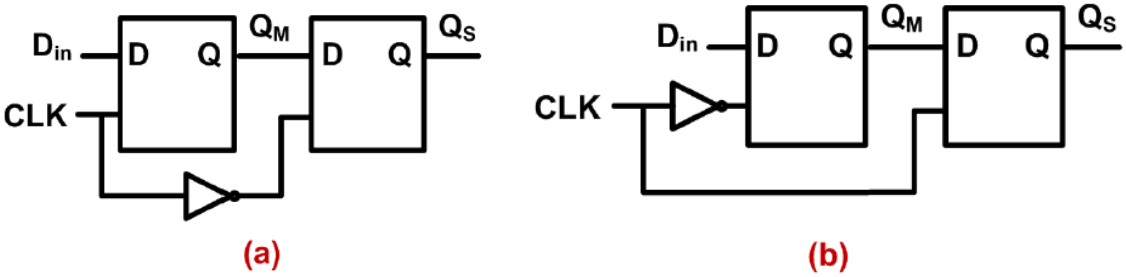
13. Can a cross-coupled 2-input XOR gate configuration function as an S-R latch? Justify with reasons. Repeat the same exercise for cross coupled 2-input XNOR gate configuration. For both cases, assume that there is no provision of asynchronous set/reset.

14. What is the function table for the feedback circuit shown below where X, Y are inputs and Q, P are outputs?



15. For the input waveforms CLK and Din as shown, plot:
(a) QM and QS for the circuit a
(b) QM and QS for the circuit b





16. Derive the characteristic table, excitation table, truth table, characteristic equation and state diagram for S − R, D, J − K and T FFs.

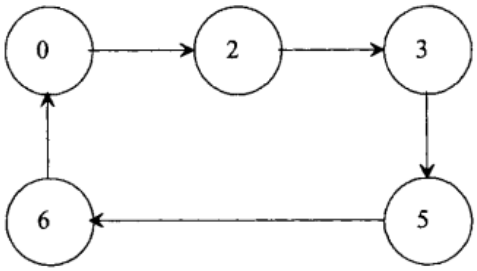
17. Convert an S − R FF into:
(a) D FF
(b) J − K FF
(c) T FF

18. Convert a D FF into:
(a) S − R FF
(b) J − K FF
(c) T FF

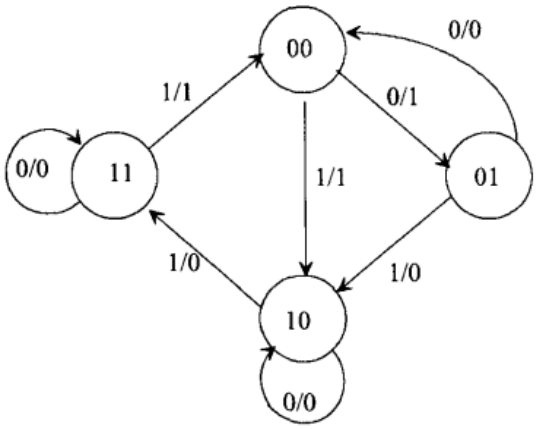
19. Convert a J − K FF into:
(a) S − R FF
(b) D FF
(c) T FF

20. Design a 2-bit counter that will count in the following sequence: 00,11,10,01, and repeat. Using T flip-flops:
(a) Draw a state diagram.
(b) Derive a state table.
(c) Implement the circuit.

21. A synchronous sequential circuit is represented by the state diagram shown in figure. Using JK flip-flops and undefined states as don't-cares:
(a) Derive the state table.
(b) Minimize the equation for flip-flop inputs using K-maps.
(c) Draw a logic diagram



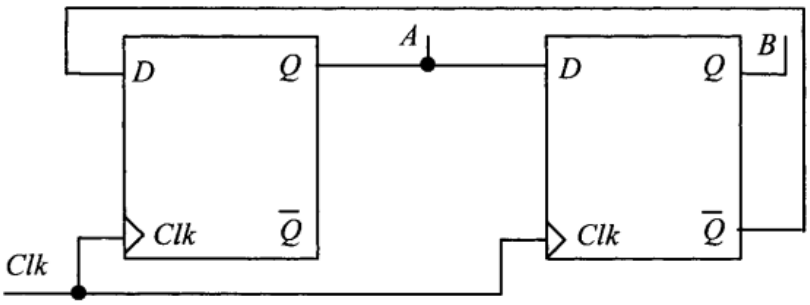
22. Design a synchronous sequential circuit using D flip-flops, whose state diagram is given below



23. Design a synchronous sequential circuit with one input x and one output y. The input x is a serial message, and the system reads x one bit at a time. The output y is 1 whenever the binary pattern 000 is encountered in the serial message. For example: If the input is 01000000, then the output will be 00001010. Use T flip-flops.

24. Design the following nonbinary sequence counters using the type of flip-flop specified. Assume the unused states as don't cares.
(a) Counting sequence 0, 1, 3, 4, 5, 7 and repeat. Use JK flip-flops.
(b) Counting sequence 0, 2, 4, 6 and repeat. Use D flip-flops.
(c)Counting sequence 0, 1,2, 4, 5, 6,7, and repeat. Use T flip-flops.

25. Consider the 2-bit Johnson counter shown in figure. Derive the state diagram. Assume the D flip-flops are initialized to A = 0 and B = 0.



26. Draw a 4-bit universal shift register.

S_1	S_0	Operation
0	0	Freeze
0	1	Right shift
1	0	Left shift
1	1	Load

27. Show how a mod 16 counter works as a frequency divider using a timing diagram.

28. How can we construct a mode 28 counter by cascading counters.

29. Design a 4-bit asynchronous up counter using:
(a) positive edge triggered FFs
(b) negative edge triggered FFs

30. A 4-bit universal shift register has its functionality decided by the control signals S1 and S0. When S1S0 = 00, the register retains its previous state. When S1S0 = 01, the register multiplies its contents by 2. When S1S0 = 10, the register divides its contents by 2. When S1S0 = 11, the register loads a new 4-bit data. Design this universal shift register using flip-flops and combinational circuits, if it treats its stored contents as an:
(a) unsigned number
(b) two's complement number

31. Design a 4-bit up-counter with minimum hardware that counts in the upward direction when CTRL = 1, and freezes its contents when CTRL = 0.

32. A long input sequence enters a one-input one-output synchronous sequential circuit, that is required to produce an output symbol z = 1 whenever the sequence 1111 occurs. Overlapping sequences are accepted; for example, if the input sequence is 01011111. . ., the required output sequence is 00000011. . ..

(a) Draw the state diagram.
(b) Draw the state table.
(c) Show the state encoding which you have adopted.
(d) Draw the corresponding logic diagram using:
   i. D flip-flops
   ii. T flip-flops
   iii. S − R flip-flops
   iv. J − K flip-flops

33. A long input sequence enters a one-input one-output synchronous sequential circuit, that is required to produce an output symbol z = 1 whenever the sequence 0101 occurs. Overlapping sequences are accepted.
(a) Draw the state diagram.

(b) Draw the state table.
(c) Draw the corresponding logic diagram using D flip-flops.