Master slave ffs SR moster slave ff noster slave ff D masler slave ff

 $\begin{array}{c|c}
\hline
D_1 & Q \\
\hline
C_2 & C_4 \\
\hline
Q & Q
\end{array}$ 

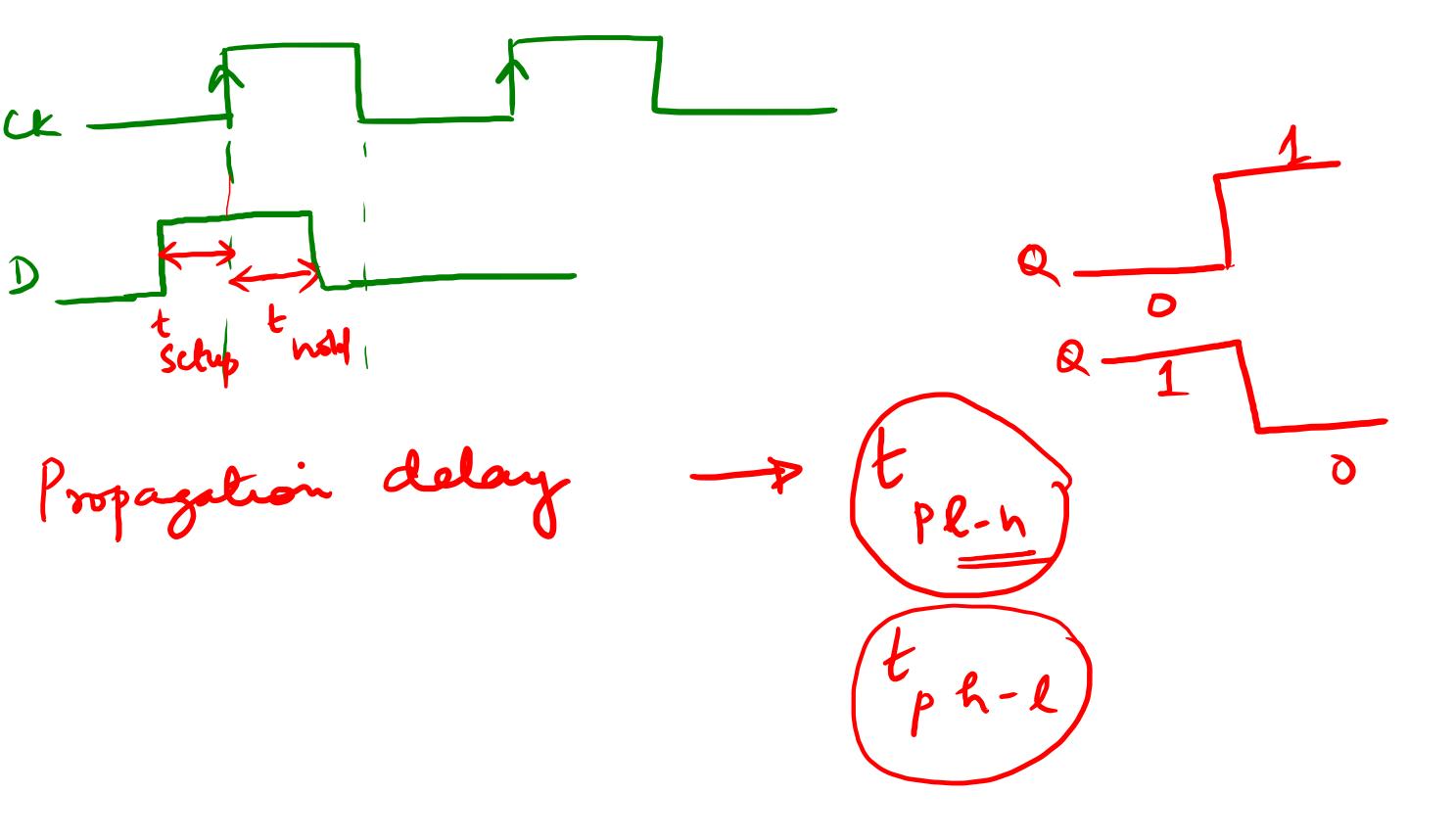
Dur G Dur G Der G asynchronous ( set ofp )

Stade	table	of M	aster	Slave D	ff	nith preset
Preset	Clear	CK	D	q		
0	1	×	×	1 0		
1	0	×	×	0 1		
0	0	×	×	1 1	Cno	t allowed)
1	1	1	٥	0 1		
1	1	1	1	10		

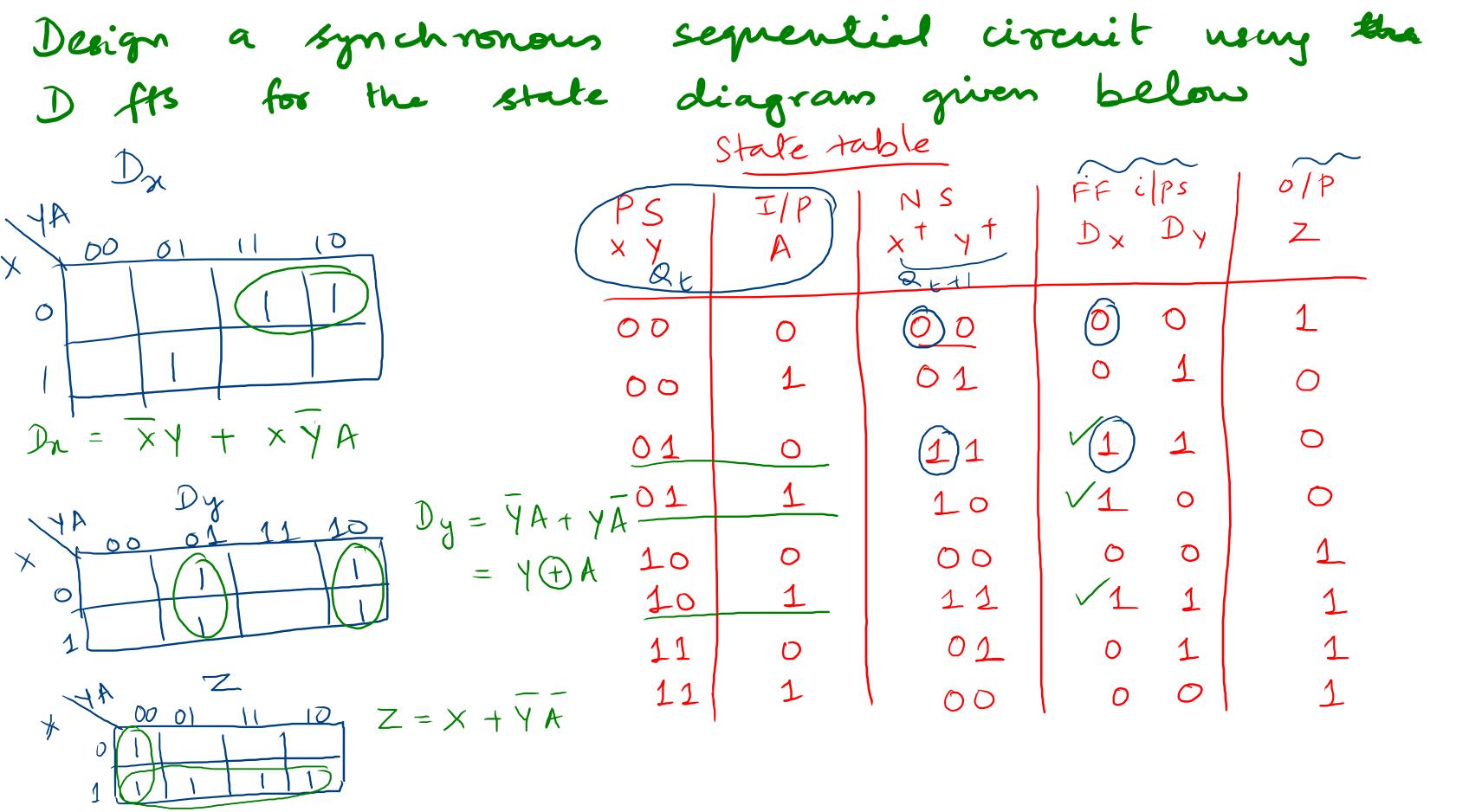
Timing Issues. - clock midth (tw) Min time tos which clock pulse should be high for the flipflops that it feeds to work properly + w → tw

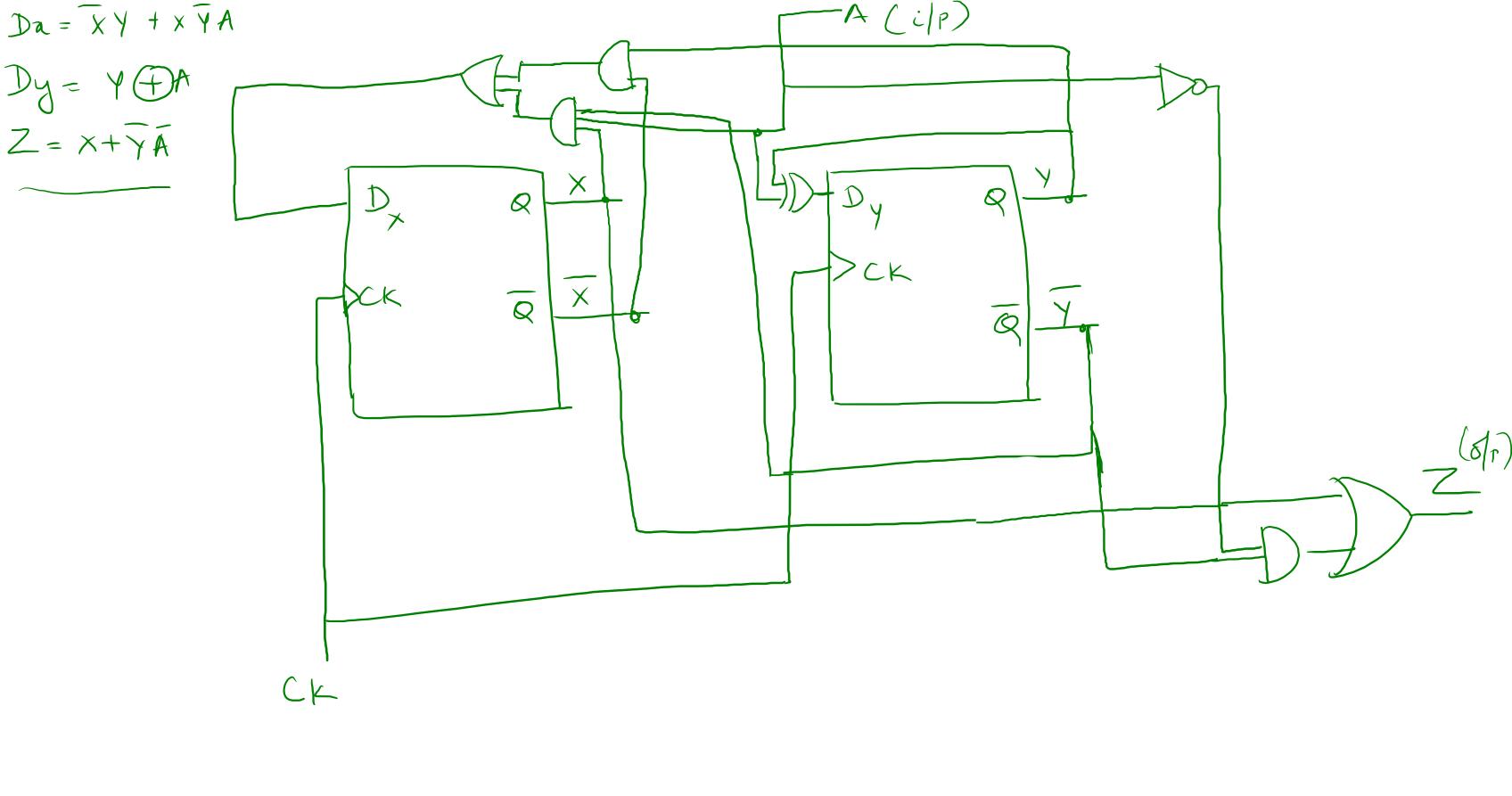
- Set up time (t Set up) Amount 25 time the ip to a ff should be stable before the arrival & actue edge of clock pulse - Hold time (thold)

Amount of time the i/p to a ff should be stable after the active slock edge arrives.

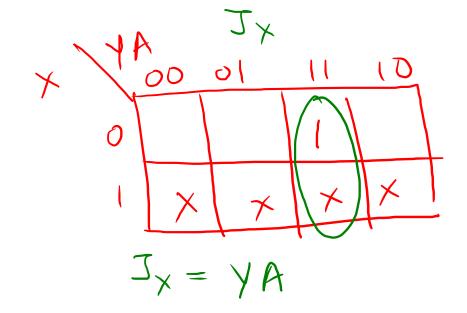


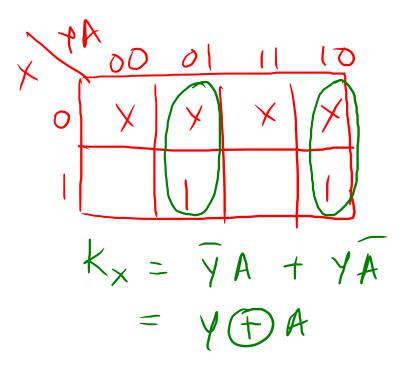
- Various types of HI latches.
- clocking
- State table / State diagrams
- Conversion of to another
Design of synchronous sequential ckts
1. Devive the State table & state diagram from
2. Obtain the minimized form for ff ilps & ofps using K map  3. Draw the losic diagrams
3. Draw the losse to

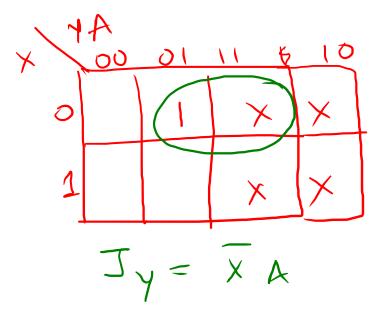




the state diagram sequential ekt given 01 L P5 MY PS A IP  $\times$  1 X 00 0 XY 10 X O  $\times$  |  $\bigcirc$ X 11 0 1 01 X 01 01 11 01  $\times$ 10  $\times$ 







$$k_y = x$$