Practice Sheet 4

1. Find the minimal sum-of-products and minimal product-of-sums expressions for:

   $f(w, x, y, z) = \Pi(1, 4, 5, 6, 11, 12, 13, 14, 15)$

   Is your answer unique?

2. A binary-coded-decimal (BCD) message appears in four input lines of a switching circuit. Design an AND, OR, NOT gate network that produces an output value 1 whenever the input combination is 0, 2, 3, 5 or 8.

3. Each of the following functions actually represents a set of four functions, corresponding to the possible assignments of the don't-care terms.

   $f1(w, x, y, z) = \Sigma m(1, 3, 4, 5, 9, 10, 11) + \Sigma d(6, 8)$

   $f2(w, x, y, z) = \Sigma m(0, 2, 4, 7, 8, 15) + \Sigma d(9, 12)$

   (a) Find $f3 = f1.f2$ using Σm and Σd notation, along with SOP and POS function. How many functions does f3 represent?

   (b) Find $f4 = f1 + f2$ using Σm and Σd notation, along with SOP and POS function. How many functions does f4 represent?

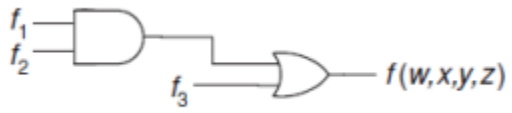
   (Hint: Just for expressing f3 and f4 using Σm and Σd notation, you need not minimize f1 and f2 using Karnaugh maps).

4. Let $f = \Sigma m(5, 6, 13)$, and $f1 = \Sigma m(0, 1, 2, 3, 5, 6, 8, 9, 10, 11, 13)$.

   Find f2 such that $f = f1f' 2$ both using SOP and POS. Is f2 unique? If not, indicate all possibilities; (you may state it in words, and not necessarily derive functions for all possibilities if at all multiple possibilities exist).

5. From the circuit given below, determine the functions f2 and f3 if f1 = xz′ + x ′ z, and the overall transmission function is f(w, x, y, z) = Σm(0, 4, 9, 10, 11, 12)

   (Hint: You need not minimize f using Karnaugh maps to determine f2 and f3)



6. Find the minimum sum of products and the minimum product of sums for each function:

   (a) f(a, b, c, d) =ΠM(0, 1, 6, 8, 11, 12).ΠD(3, 7, 14, 15)

   (b) f(a, b, c, d) = Σ_m(1, 3, 4, 11) + Σ_d(2, 7, 8, 12, 14, 15)

   (c) f(a, b, c, d, e) = Σm(0, 1, 2, 6, 7, 9, 10, 15, 16, 18, 20, 21, 27, 30)+Σm(3, 4, 11, 12, 19)

   (d) f(a, b, c, d, e) =ΠM(0, 3, 6, 9, 11, 19, 20, 24, 25, 26, 27, 28, 29, 30).ΠD(1, 2, 12, 13)

7. A combinational network with four inputs A, B, C, and D, three intermediate outputs Q, P, and R, and final two outputs T1 and T2 is shown in Fig. 2.

   (a) Assuming that G1 and G2 are both AND gates, show the map for the smallest function Pmin (i.e., with the minimum number of minterms) that makes it possible to produce T1 and T2.

   (b) Show the maps for Q and R that correspond to the above Pmin. Indicate explicitly the don't-care positions.

   (c) Assuming that G1 and G2 are both OR gates, find the largest Pmax and show the corresponding maps for Q and R.

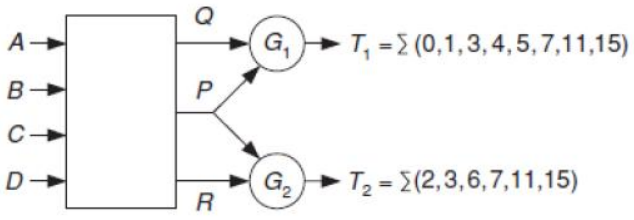


Figure 2: Combinational network

8. You are supplied with just one NOT gate and an unlimited amount of AND and OR gates and are required to design a circuit that realizes the expression

   $T(w, x, y, z) = w'x + x'y + xz'$

   Only unprimed variables are available as inputs. (Hint: You may find the map of T helpful.)

9. A certain four-input gate, called a LEMON gate, realizes the switching function LEMON(A,B,C,D) = BC(A + D). Assume that the input variables are available in both primed and unprimed form.

   (a) Show a realization of the function $f(w, x, y, z) = \Sigma m(0, 1, 6, 9, 10, 11, 14, 15)$ with only three LEMON gates and one OR gate.

   (b) Can all switching functions be realized with LEMON and OR logic?

   (Hint: Draw the map for LEMON and utilize possible "patches" (coverings of the minterms of f with the LEMON function) on the map of f.)

10. A logic module A, shown in Fig. 3, operates as follows: output yi = 1 if and only if i inputs out of x0, x1, x2 are equal to 1. Design unit B in such a way that the overall logic function of unit C will be to produce an output zi = 1 if and only if i inputs out of x0, x1, x2, x3 are equal to 1.

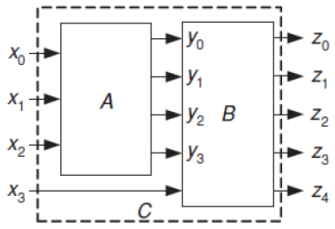


Figure 3: Logic modules

11. (a) Write the complete truth table of a 2:1 multiplexer. Re-write the truth table using don't-care combinations at the inputs to reduce the number of rows of the truth table.

    (b) Using don't-care combinations at the inputs, write the truth table of a 4:1 multiplexer.

    (c) Draw the gate level implementation of a 4:1 multiplexer using NAND gates only.

12. (a) Using 2-input gates ONLY, design a 4-bit controlled incrementer /decrementer circuit, which performs increment operation when a control input P = 0, and performs decrement operation otherwise.

(b) Using the 4-bit controlled incrementer / decrementer circuit as a sub-circuit, design a 16-bit controlled incrementer / decrementer.

13. (a) Using 2-input gates ONLY, design a 4-bit controlled 2's complementer circuit, which performs 2's complementation when a control input P = 1, and leaves the input unchanged otherwise.

    (b) Using the 4-bit controlled 2's complementer circuit as a sub-circuit, design a 16-bit controlled 2's complementer circuit.

14. Design a 4-bit leading one detector. The detector circuit accepts a 4-bit input and generates a 4-bit output string with a single logic 1 exactly at that position where the first 1 is encountered, starting from the MSB side of the input. If the input comprises all zero bits, the output is identical to the input. Do not use gates having a fan-in of more than two.

15. Using a single 2:1 multiplexer and two 2-input XOR gates, construct a full adder cell. (Hint: You may use the concept of carry propagate driving the select line of the multiplexer.)