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Objective:

The objective of this project is to design, simulate, and implement fundamental sequential logic circuits using flip flops in order to analyze their behavior in clocked digital systems. The project focuses on the analysis of flip flops and latches as memory elements, comparison of synchronous and ripple counter architectures, implementation of counters and shift registers using TTL integrated circuits, validation of theoretical operation through hardware measurements, and observation of timing behavior and propagation delay.

This project explored three major designs:

1. 3 Bit Modulo 8 Synchronous Counter
2. 3 Bit Modulo 8 Ripple Counter
3. 4 Bit Shift Register

Each design was first simulated using Multisim, then constructed on a protoboard to validate theoretical predictions with real hardware measurements.

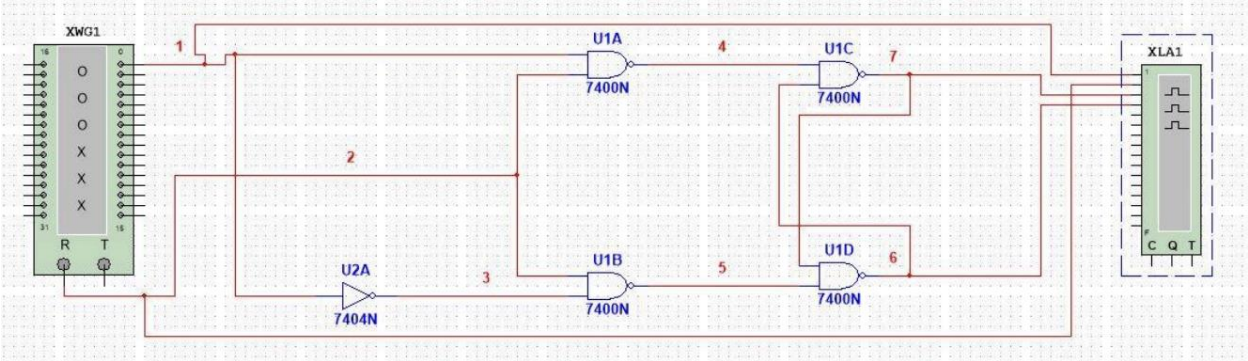

Figure 1: Half of a D type Master Slave Flip Flop (Multisim)

1. *D Type Latch*

A D latch updates its Q output to match the D input whenever the clock is logic high. Unlike an edge triggered flip flop, it is level sensitive. Figure 1 in the manual was replicated in Multisim to confirm that Q follows D only when CP=1 and holds its previous value when CP=0.

2. *Timing Verification*

Using the Word Generator and Logic Analyzer, I observed the CP, D, and Q signals. The timing diagram matched the expected behavior: Q changed only during the high level of CP and remained stable otherwise.

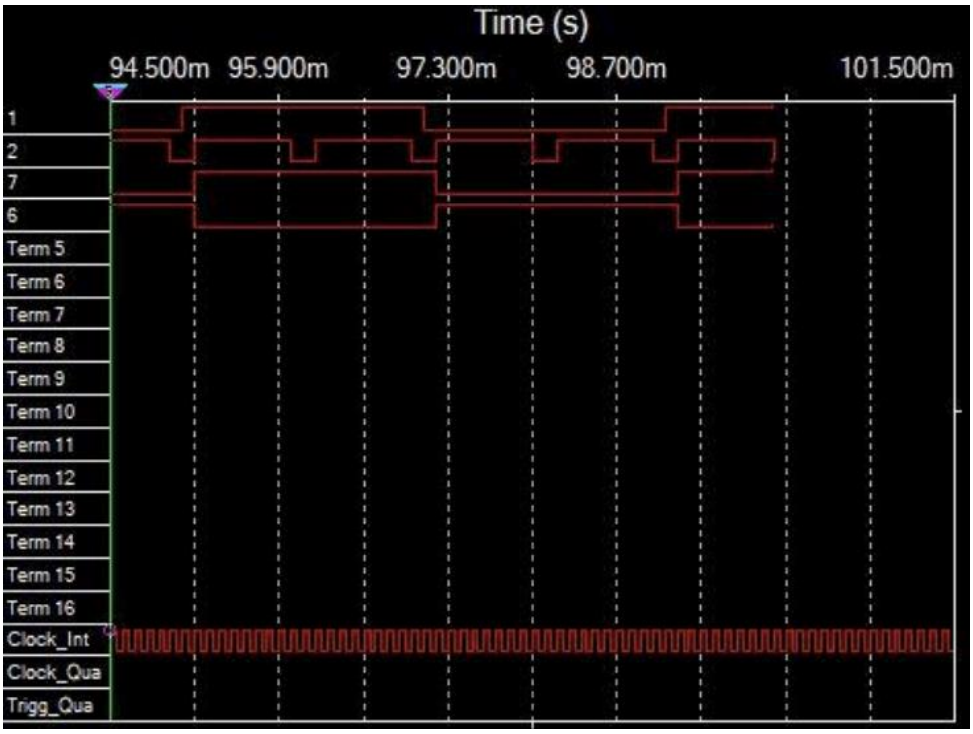

Figure 2: Logic Analyzer

For the logic analyzer the first pin connects to the D input and the second pin connects to the CP and the third pin connects to Q output and the fourth pin connects to the Q' output. When the D input is 1, and the CP input is 1 then the output is 1. If any of the inputs are 0 then the output is 0. This shows that Q tracks D when the clock is high and holds value when it's low.

3 Bit Modulo 8 Synchronous Counter:

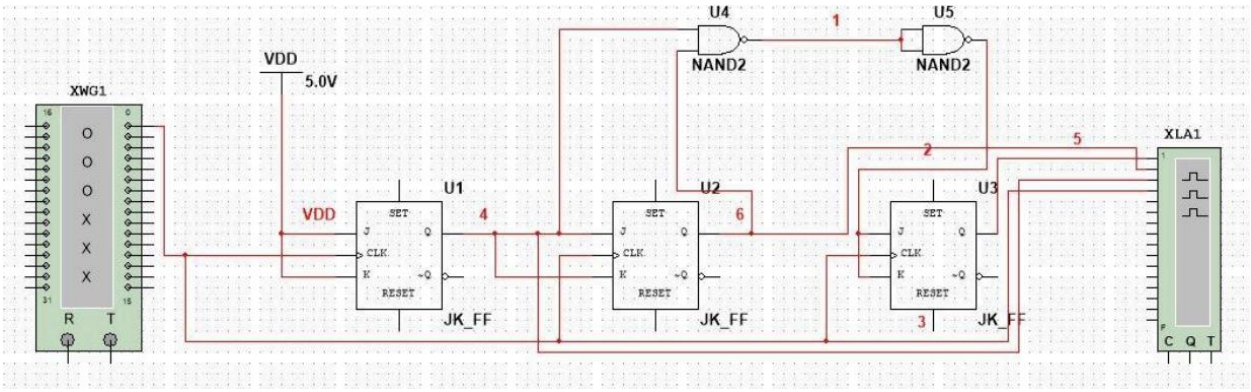

Figure 3: 3 Bit Modulo 8 Synchronous Counter (Multisim)

The Multisim constructed above has 3 JK flip flops and 2 NAND gates combined in a way that the NAND gates output as an AND gate. Attached are the word generator and logic analyzer.

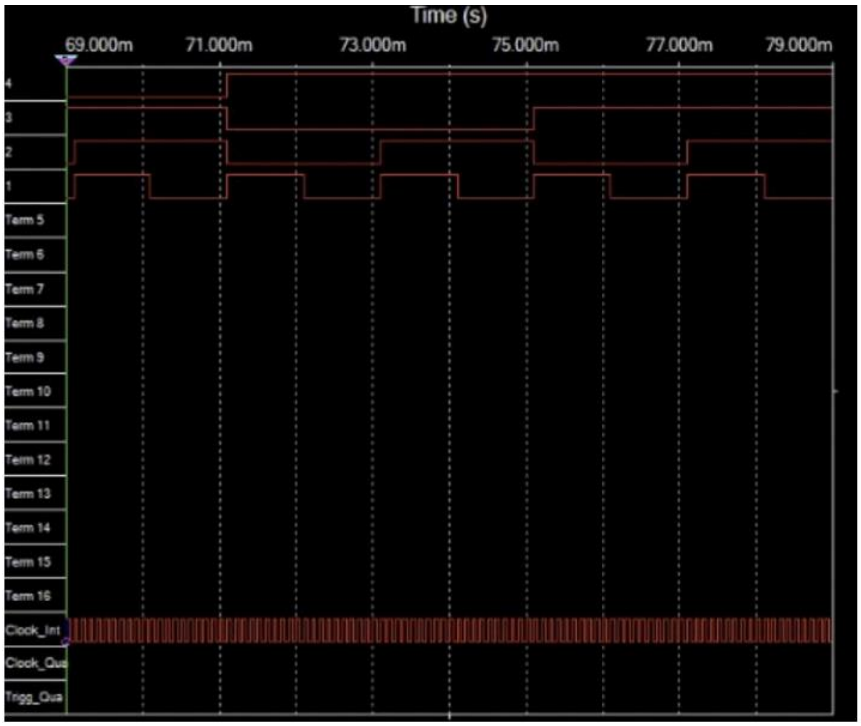

Figure 4: 3 Bit Modulo 8 Synchronous Counter Output

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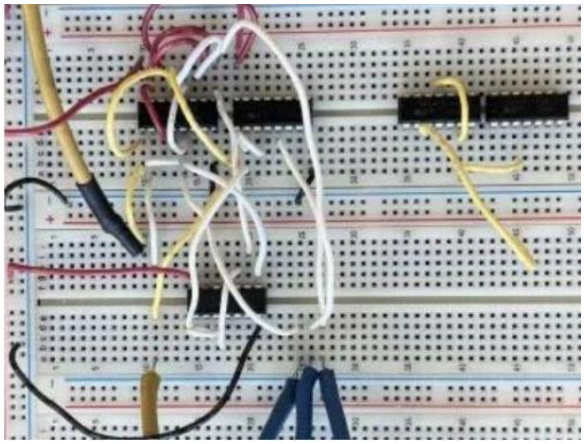
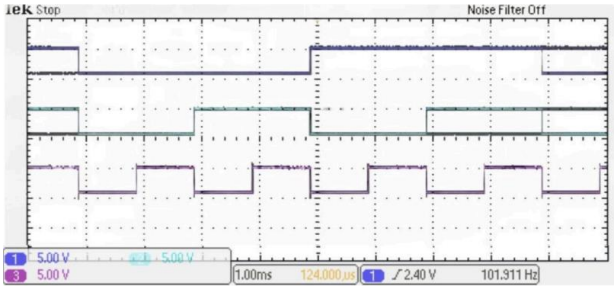
This simulation shows the counter from states 0 to 7, with each output at half frequency of the prior.

Protoboard:



I constructed this circuit on the protoboard using the JK flip flops and NAND gates. The IC chips used were 74LS76 which served as the JK flip flops and the 74LS00 which acted as a NAND gate.



The image above is the oscilloscope data. I supplied a 5v power supply to the circuit. Each stage operated as expected, dividing the signal frequency by two compared to the preceding flip flop.

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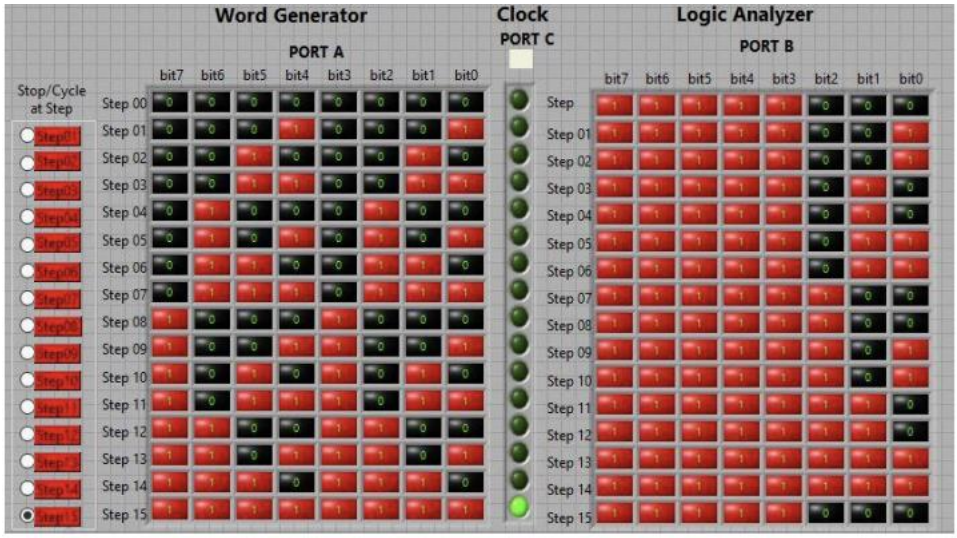

The image above shows the data taken from both the word generator and logic analyzer.

After constructing the circuit on the protoboard I connected the word generator and logic analyzer and through LabView I viewed the previous data. By monitoring the JK flip flop with the logic analyzer while it is driven by the word generator, the step by step input and output signals confirm that the counter follows the expected pattern.

3 Bit Modulo 8 Ripple Counter:

Constructed with three D flip flops, the modulo 8 ripple counter functions as an asynchronous device. The external clock drives only the first flip flop; subsequent stages are triggered by their predecessor's output, introducing minor propagation delays when compared with a synchronous counter. The circuit advances through binary states 0 to 7.

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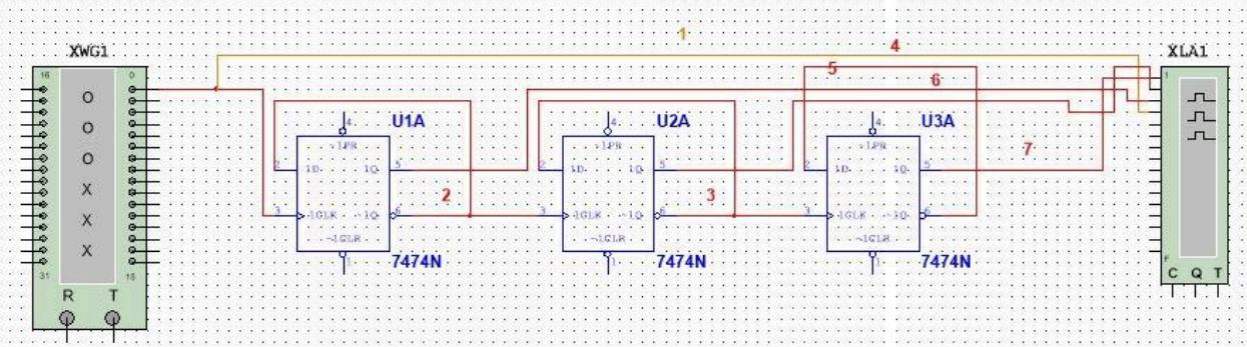
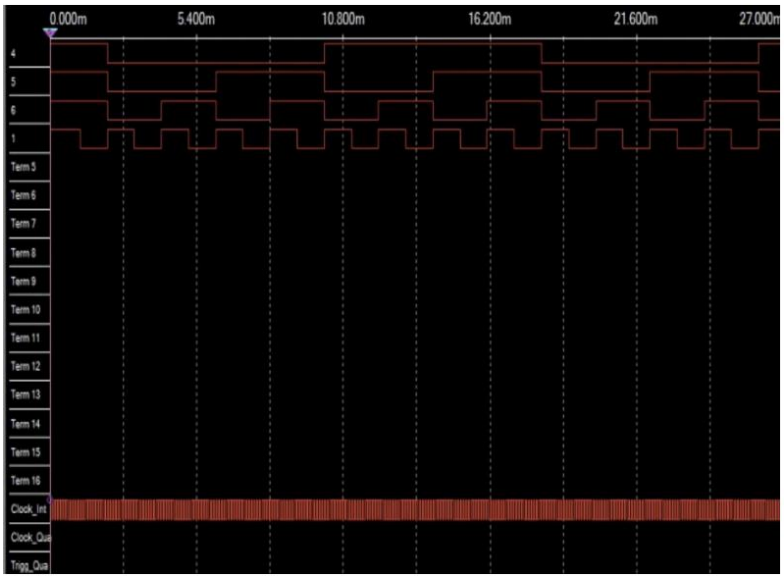


The image above depicts the 3 Bit Modulo 8 Ripple Counter constructed in Multisim. It is built of 3 D flip flops and connected to a word generator and logic analyzer.



The image above shows the output derived from running the circuit.

The ripple counter circuit is constructed below. Using 74LS74 D flip flops, I constructed a ripple counter and observed its operation on the oscilloscope. The positive edge triggering of the 74LS74 ensured reliable frequency division, with the clock applied to the first stage and each successive flip flop driven by the previous stage's output.

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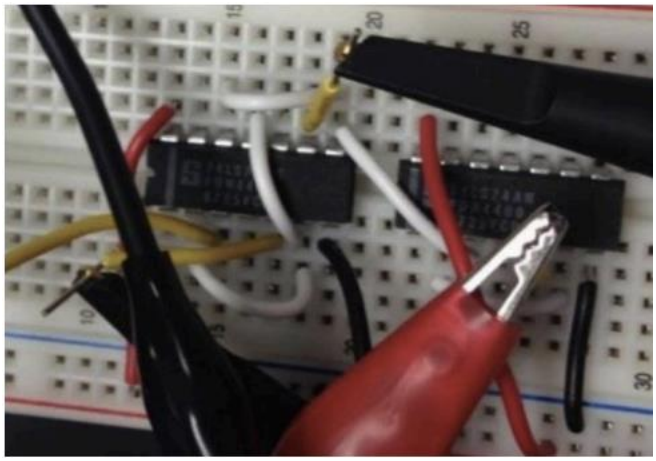

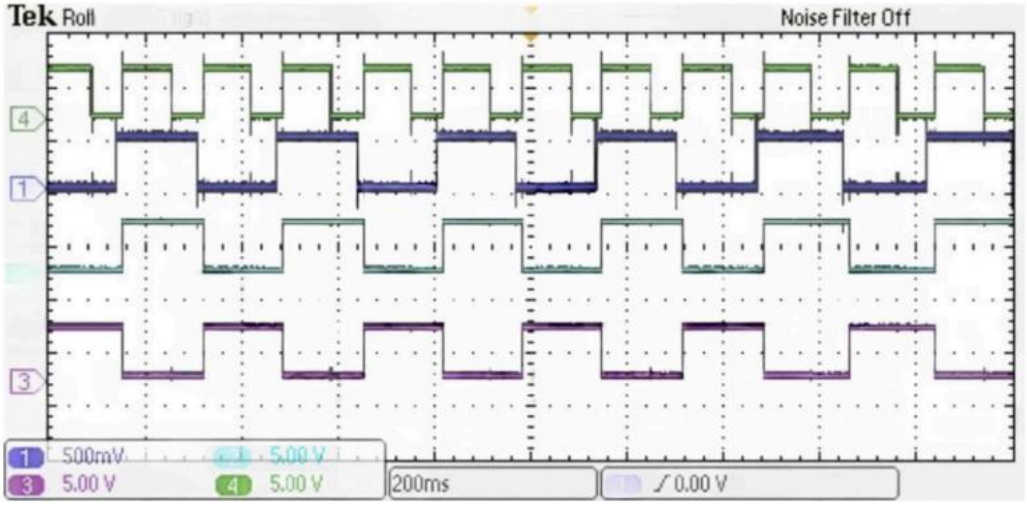

The image above shows the data retrieved from the oscilloscope for the ripple counter.

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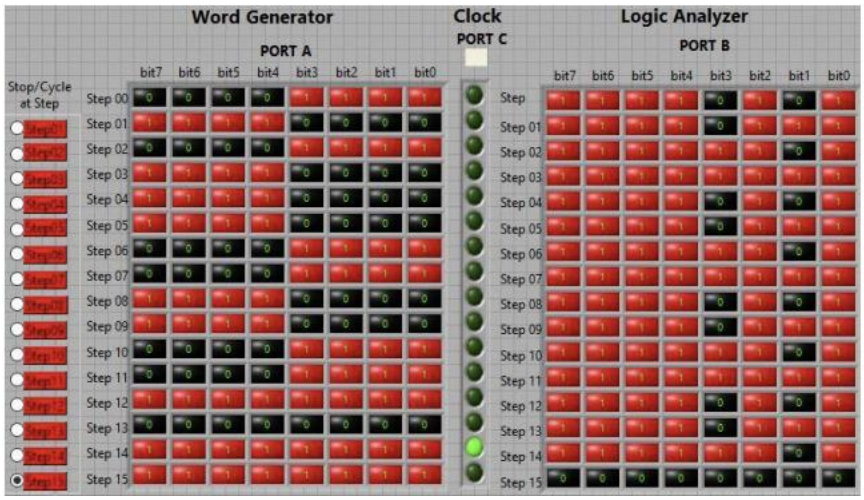
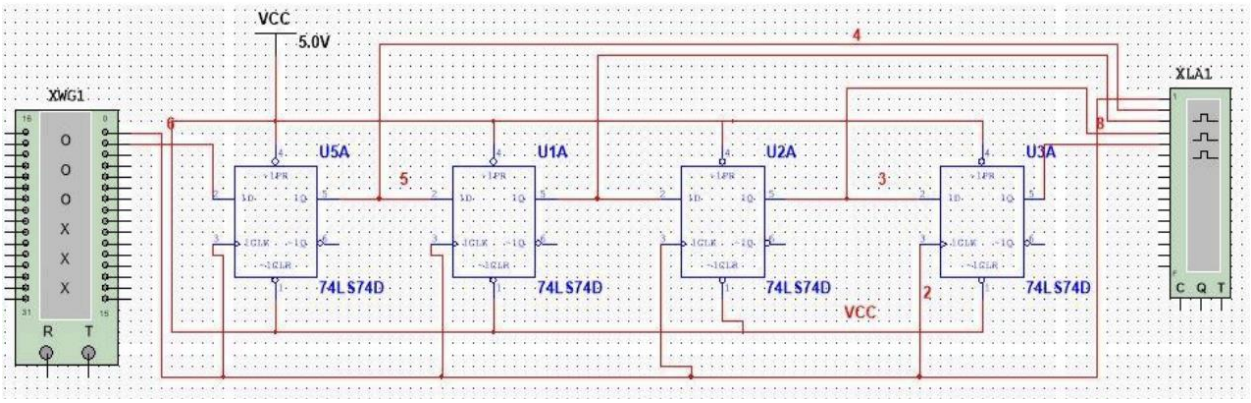


This is the data retrieved from the word generator and logic analyzer.

4 Bit Shift Register:



A 4 bit shift register is a sequential digital circuit made of four flip flops connected in series, each representing one bit of storage. Every flip flop shares the same clock signal so they all update simultaneously at each clock pulse.

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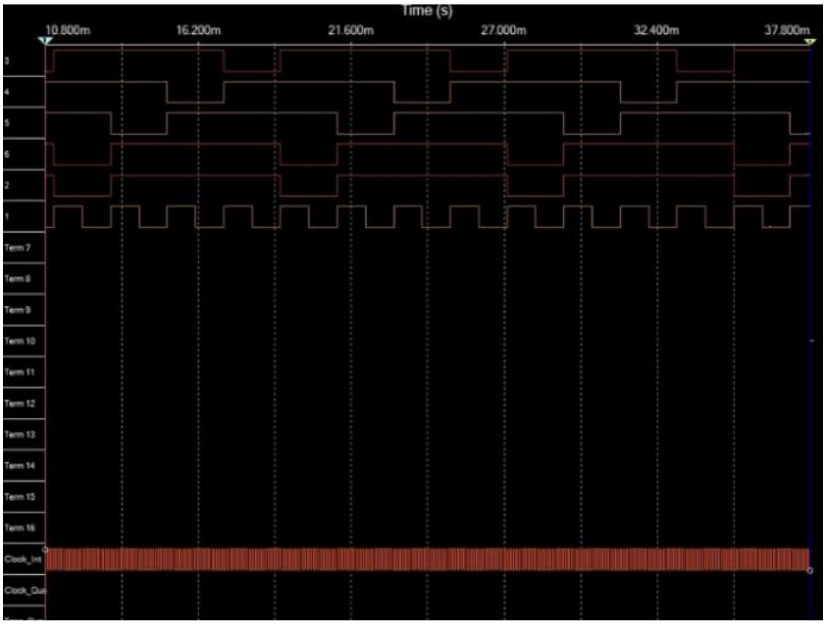
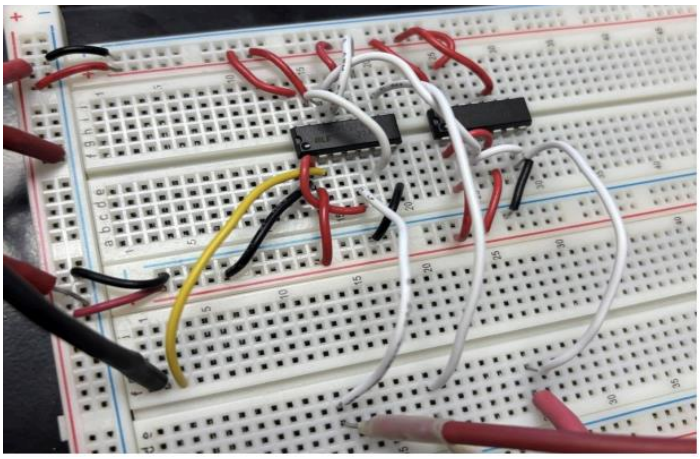


This is the data taken after designing the circuit on Multisim.



This is the 4 bit shift register reconstructed onto the protoboard. The 4 bit shift register was assembled on a breadboard with D flip flops, showcasing step by step data movement as each clock pulse advances the input bit to the next stage.

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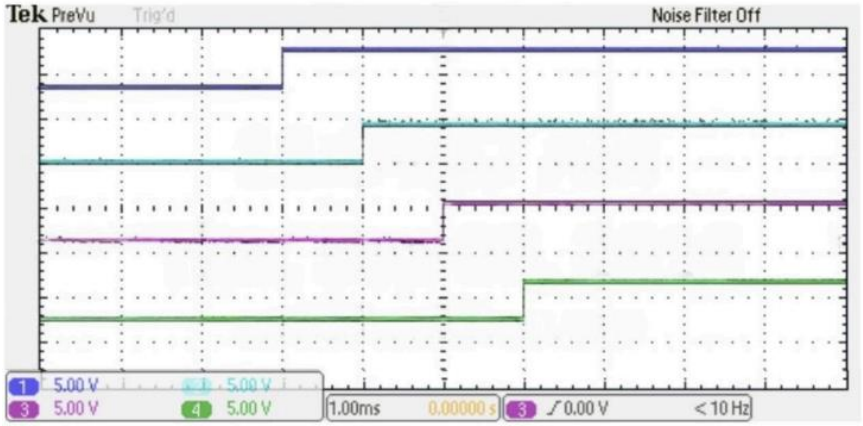
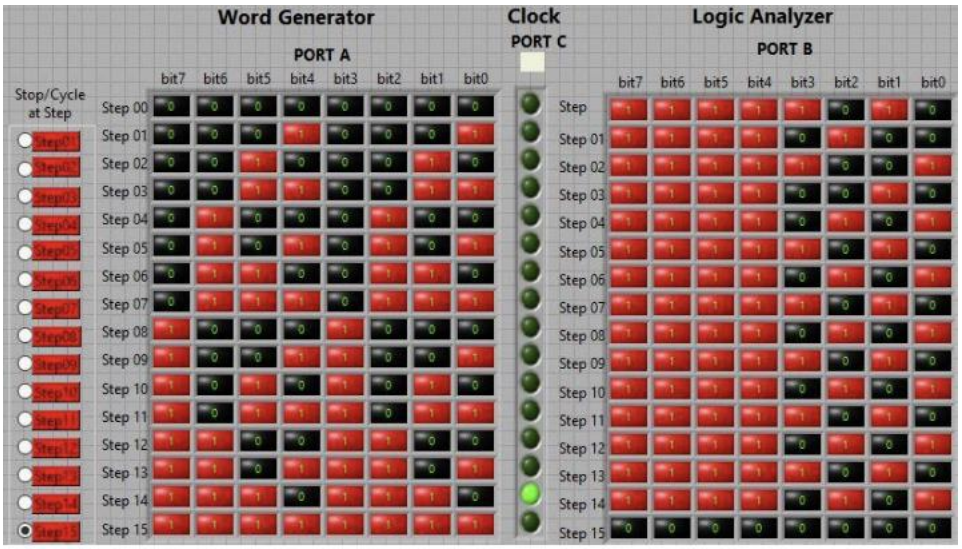


This is the data taken from the oscilloscope of the 4 bit shift register. With each clock pulse, the input bit advances by one stage, moving sequentially through the flip flops.



This shows the logic analyzer trace of the 4 bit shift register, illustrating how data bits move step by step through each stage on every clock pulse.

Results and Observations:

Hardware measurements closely matched Multisim simulation results, confirming correct circuit operation. Synchronous counters demonstrated superior timing performance compared to ripple counters, with clean and predictable state transitions due to simultaneous clocking of all flip flops. Ripple counters exhibited expected cumulative propagation delays between stages, which were clearly visible in timing measurements.

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Shift register operation was successfully verified using oscilloscope and logic analyzer measurements, showing correct sequential data movement with each clock pulse. Minor noise was occasionally observed due to breadboard wiring, but this did not significantly affect overall circuit performance.