Objective

The objective of this project is to design, implement, and test a digital clock using discrete digital integrated circuits and seven-segment displays. The system is evaluated by verifying correct counting, cascading, and display behavior for seconds, minutes, and hours. Emphasis is placed on timing accuracy, counter synchronization, and practical troubleshooting of hardware based digital systems.

This project utilized:

- **BCD Counters (CD4510 and CD4518)**: To count seconds, minutes, and hmys.
- **Seven-Segment Display Driver (CD4543)**: To convert BCD inputs into visible numerical outputs.

By cascading counters and using logic levels for control, I created a functional digital clock capable of displaying time in a 12-hmy format.

Materials and Equipment

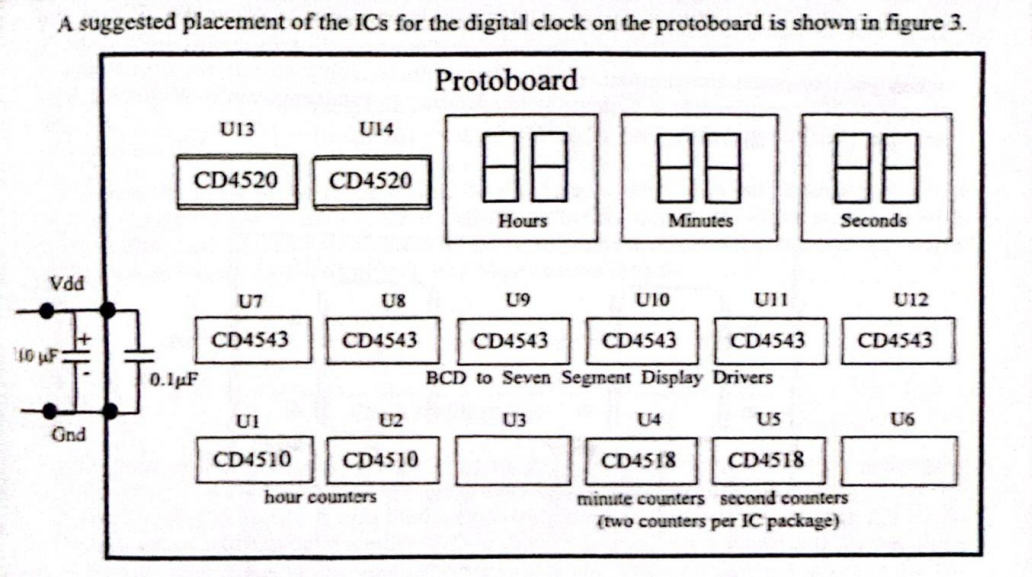
1. **ICs Used**:
    a. CD4543: BCD to Seven-Segment Display Driver
    b. CD4510: Presettable BCD Counter
    c. CD4518: Dual BCD Counter
    d. CD4081: AND Gate

2. **Other Components**:
    a. Seven-Segment LED Displays
    b. Protoboard and jumper wires
    c. Power Supply
    d. Sine Wave Generator

Procedure

1. **Seven-Segment Display Setup**:
    a. Configured the CD4543 IC to drive the seven-segment displays and display numbers 0-9 based on BCD input.
2. **Seconds and Minutes Counting**:
    a. Connected CD4518 counters to count from 0 to 59 for both seconds and minutes.
    b. Implemented cascading counters to ensure the minutes increment after 59 seconds.
3. **Hmy Counting**:
    a. Set up CD4510 counters to count from 1 to 12 and reset after reaching 12 to simulate a 12-hmy clock format.

My finished model should reflect this circuit



Seconds

The components used in this part of the digital clock were the seven-segment display, and the IC chips, CD4543 and CD4518, as well as the AND gate CD4081.

The datasheet for the IC chip, CD4543

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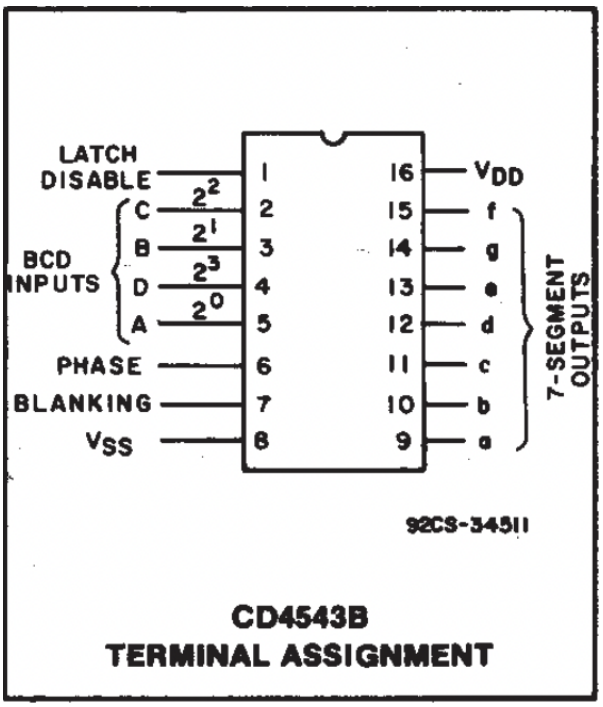

CD4543B
TERMINAL ASSIGNMENT

The datasheet for the IC chip, CD4518

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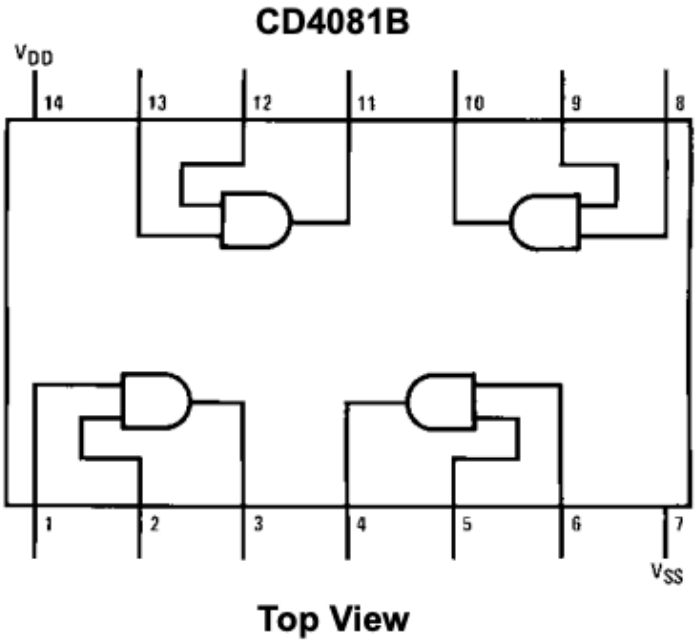
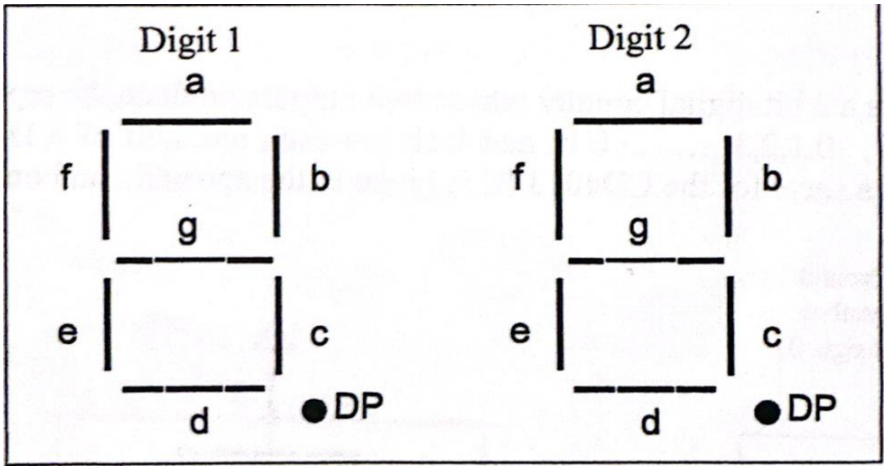
The datasheet for the AND gate, CD4081



The datasheet for the seven-segment display



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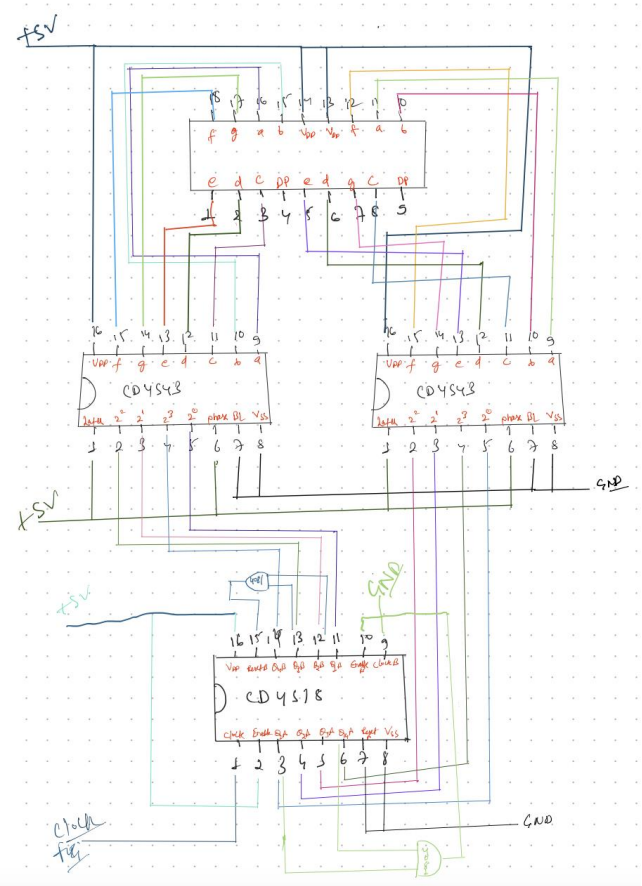
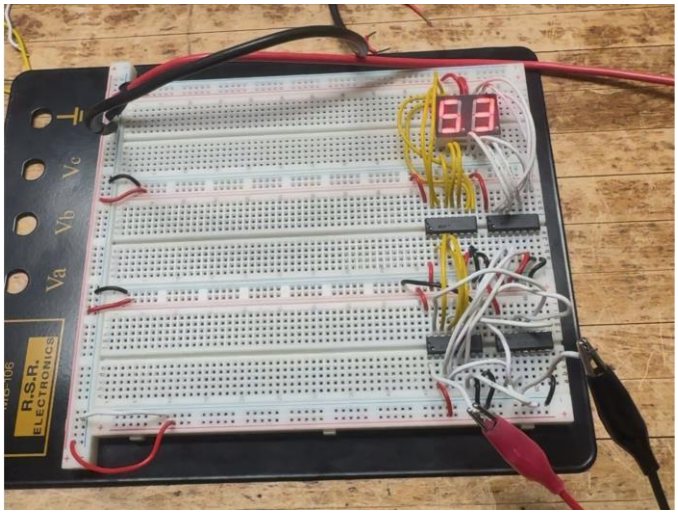
To construct this digital clock, I drew the wiring diagram provided below:



After performing the connections shown above, my circuit correctly displayed the seconds.



Description for Seconds

The expected output is for the display segment to portray the digits from 0 to 59 and then repeat back to 0 before reaching 60. The components used were the seven-segment display, the chips CD4543 and CD4518 and the AND gate CD4081. Even though this was the first portion of this project, it proved to be difficult. After configuring the circuit by replicating the wiring diagram I encountered the first problem, which was that one side of the display wouldn't light. My first idea was to go over the circuit once more to confirm the correct connections and after checking and guaranteeing that my wiring was right, I began to think again what the issue could be. I decided it might be something with the components used that may have been damaged. To check this, I switched the components and still encountered my issue. As I continued projecting, I noticed that fidgeting with the wires would cause the display to illuminate completely and decided my issue could be the wires or the breadboard itself. I then disassembled the circuit and stripped new wire and made the connections again. At this point my

circuit was still providing issues. I later noticed some spaces on my breadboard were very loose and when I shook the components on those squares my display started to count. I then disassembled the connections to the AND gate to shift it down one square for a more stable connection. After this my display started to count the seconds as expected. To power the circuit, I supplied 5 volts dc from the power supply, and connected the sine wave generator to a wire protruding from the square connected to the IC chip CD4518's pin 1 (clock).

Minutes

The exact components used to assemble the seconds were now used to assemble the minutes.

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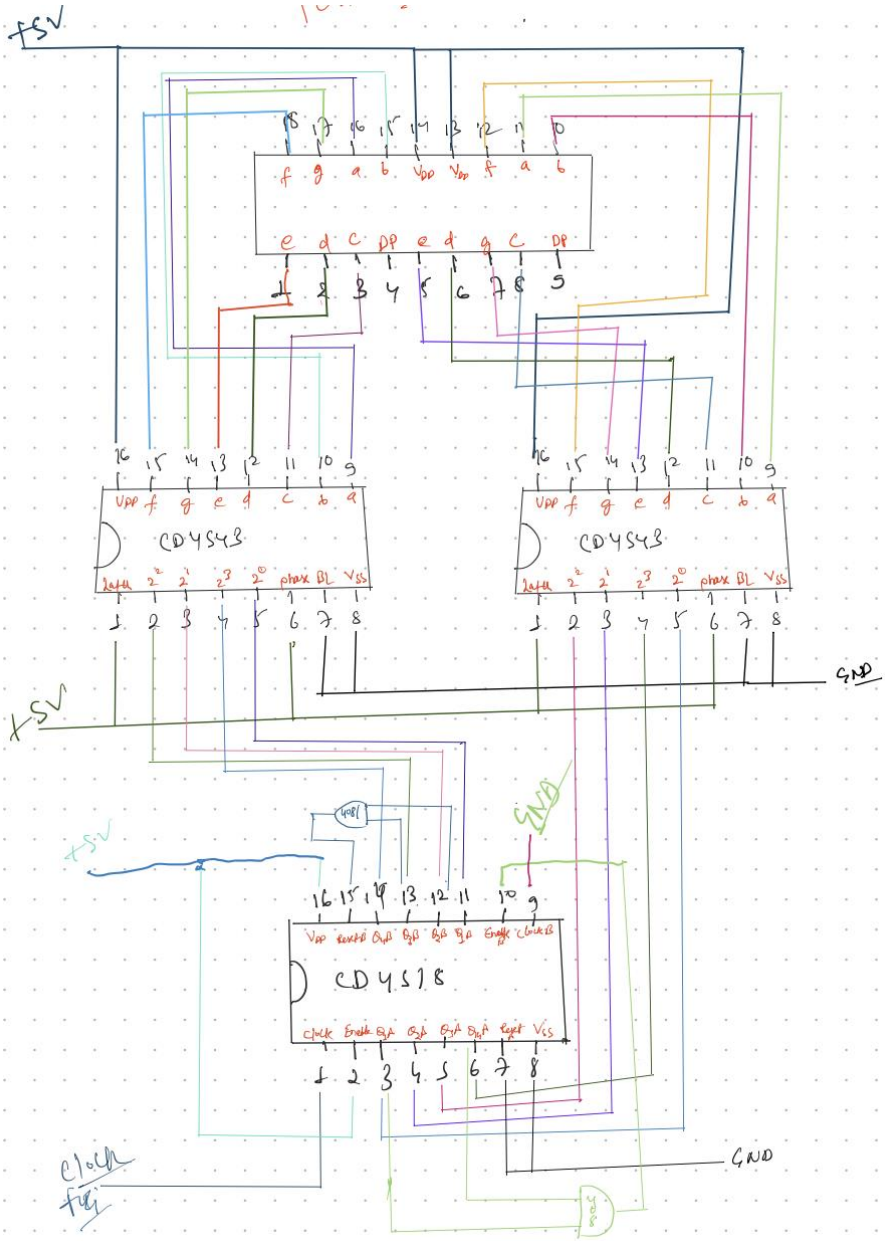

After performing the connections above I began cascading the minutes to seconds. This act allows the minutes to work in accordance with the seconds counter.

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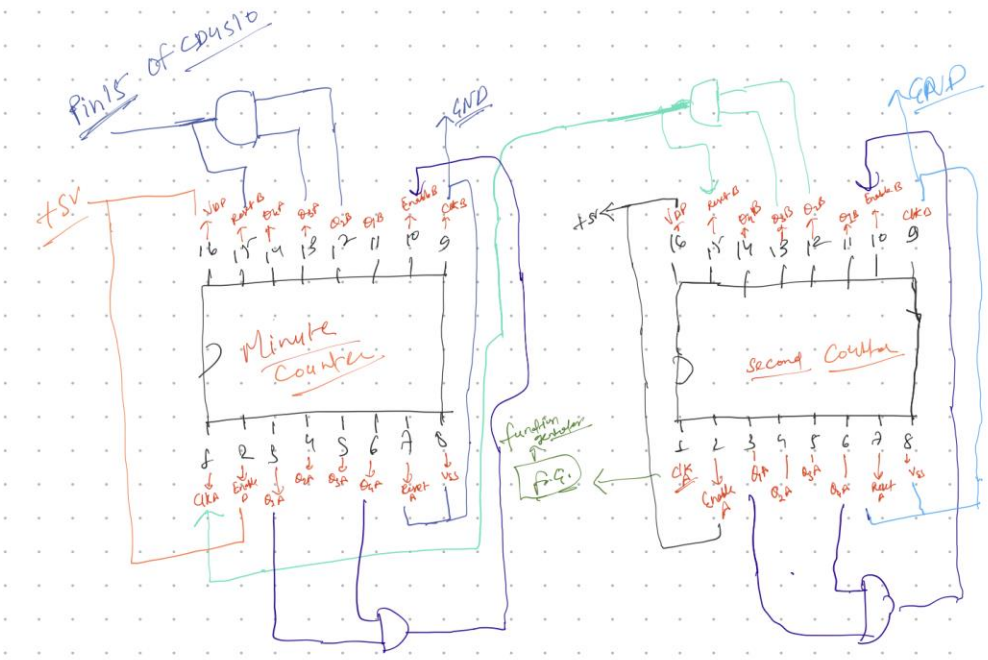
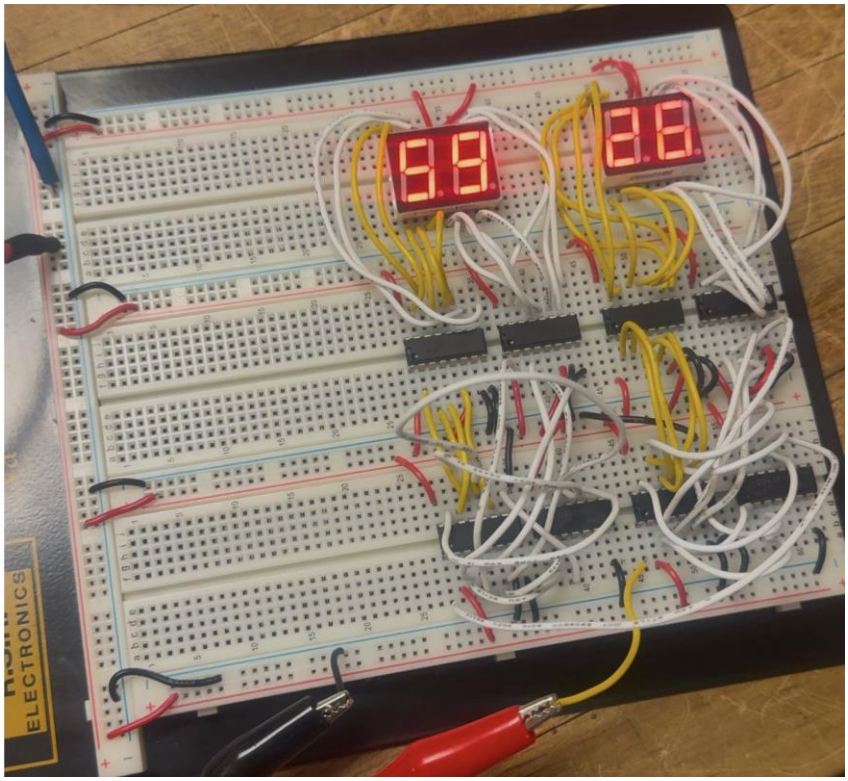


After performing the connections shown above, my circuit correctly displayed the minutes.



Description for Minutes

Configuring the circuit according to the wiring diagram for the second display, it is supposed to portray an accurate minute counter. At this point in the project I had one display wired up showing the seconds and another displaying the minutes. After the seconds counter reached 59 and reset back to 0 to begin again, the minutes counter would be updated and begin counting. This would repeat, as the first display reached 60 seconds the second display would now count 1 minute and hold that value until 60 seconds were counted again. The minutes counter would then reset back to 0 after 59 minutes passed and begin again. The components used in this part of the project were

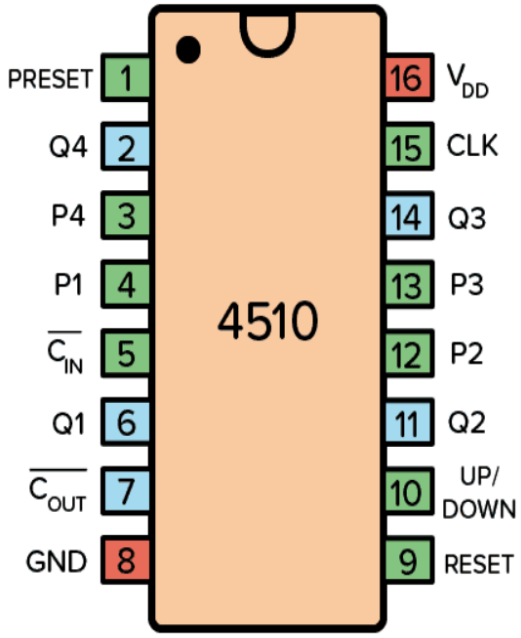
the same as the previously used in seconds. This consisted of a seven-segment display, two IC chips: CD4543 and CD4518, and an AND gate: CD4081. After configuring the minutes accordingly, I then cascaded them to the seconds so that it could begin counting after 60 seconds and hold that value until another 60 seconds has passed. While constructing this portion of the project I ran into problems. My issues resembled the same problems encountered in the first portion of the project, the display wasn't lighting every section of the number and then it began not counting correctly. After running into the first problem with incorrect lighting across the display, I moved the wires around and this would solve the problem. But after this I noticed, the numbers would begin counting in a random manner, such as 9, 43, 64... and so on. I began to troubleshoot; my first approach was to confirm the wiring, where I found nothing wrong. My next approach was to check the connection of the wires. I did this by making sure each wire was pushed in properly, then fidgeting with them and putting them at different angles for a more secure connection if that was the problem. This caused my seconds to begin acting up and counting incorrectly, from 0 to 9 and then resetting back to 0. This proved my main issue was a combination of the wires and the breadboard. I decided my best action would be to restart after not being able to fix the issue. In this second attempt I stripped new wires for every connection to assure none of my wires were too bent or broken under the insulation. After confirming the seconds, I began again on the minutes. After constructing the circuit, I cascaded the two and my minutes began counting correctly. The cascading connected pin 1 (clock) from the chip CD4518 from the minutes and connected it to pin 15 of the AND gate. The minutes were

supposed to count to 60 minutes representing one hmy, and to then reset back to 0 to begin again. Because this would take too long, I adjusted the frequency being input. It was a direct relationship between the frequency and the speed of the counters. Just as with the second's counter, I supplied 5 volts dc to the protoboard and then connected the sine wave generator to pin 1 of the CD4518 IC chip from the second's counter.

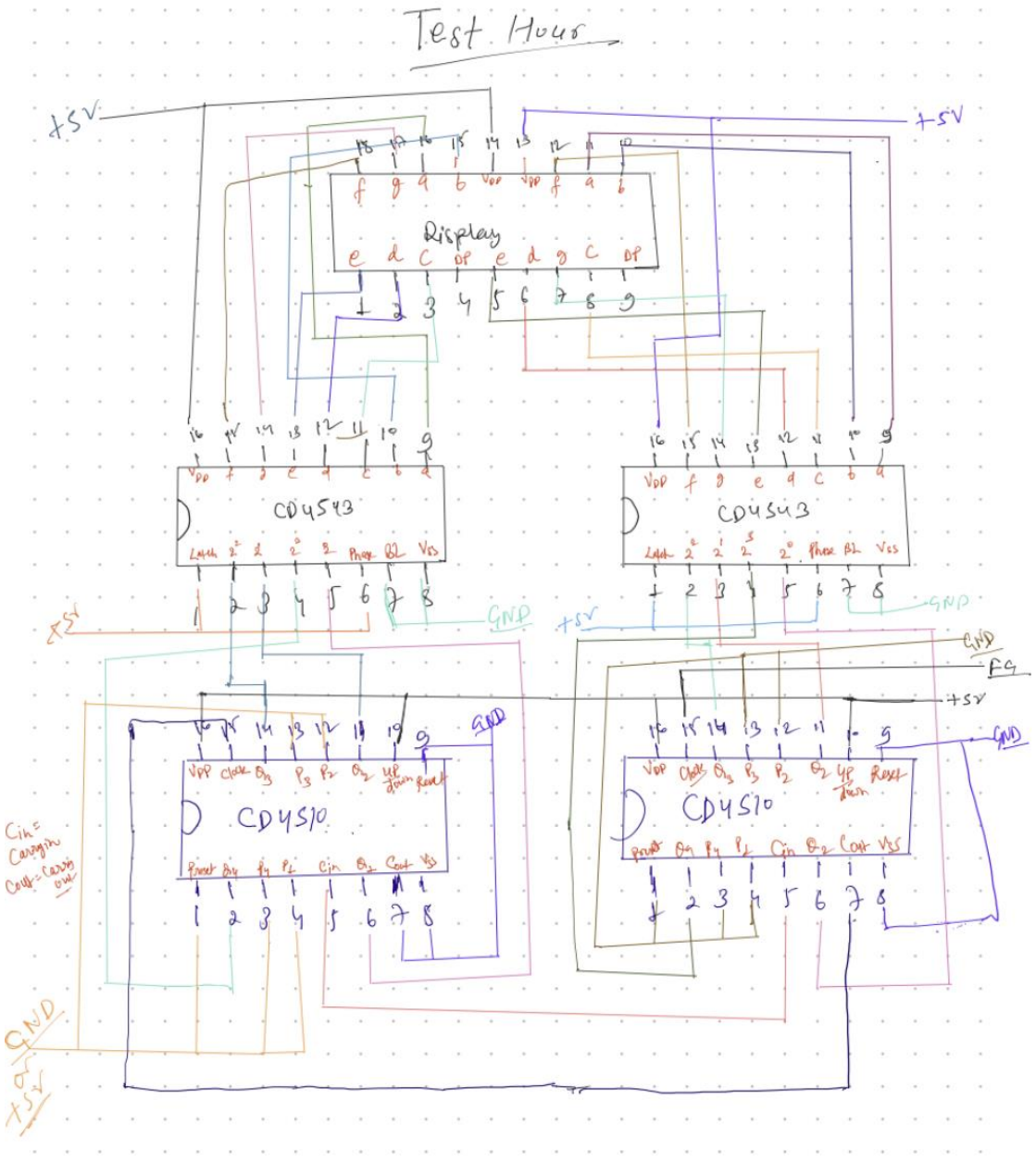
Hmys

Constructing the circuit for the hmys required a new component; the chip CD4510, and was used twice in this circuit.

The datasheet for the IC chip, CD4510



The wiring diagram for the hmys are as shown



After the connections were completed, I began cascading. Cascading for this portion of the project was a bit more complicated as you had to cascade the two IC chips CD4510 together as well as cascading to the AND gate used in the minute's connections so that it could begin counting after every 60 minutes.

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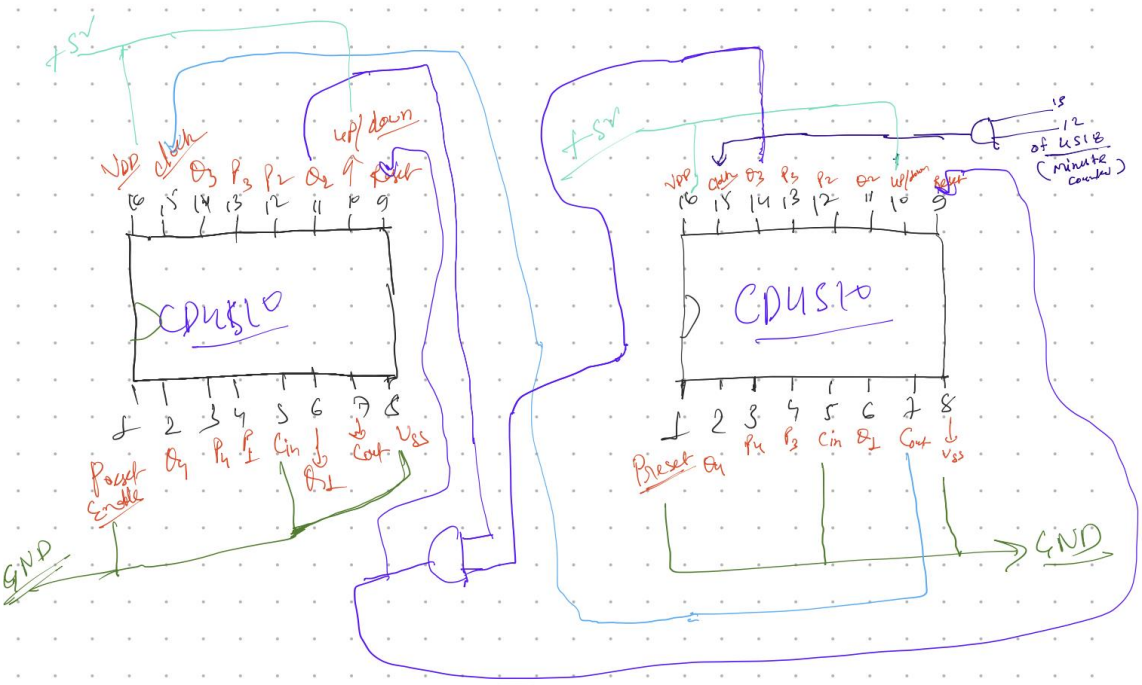
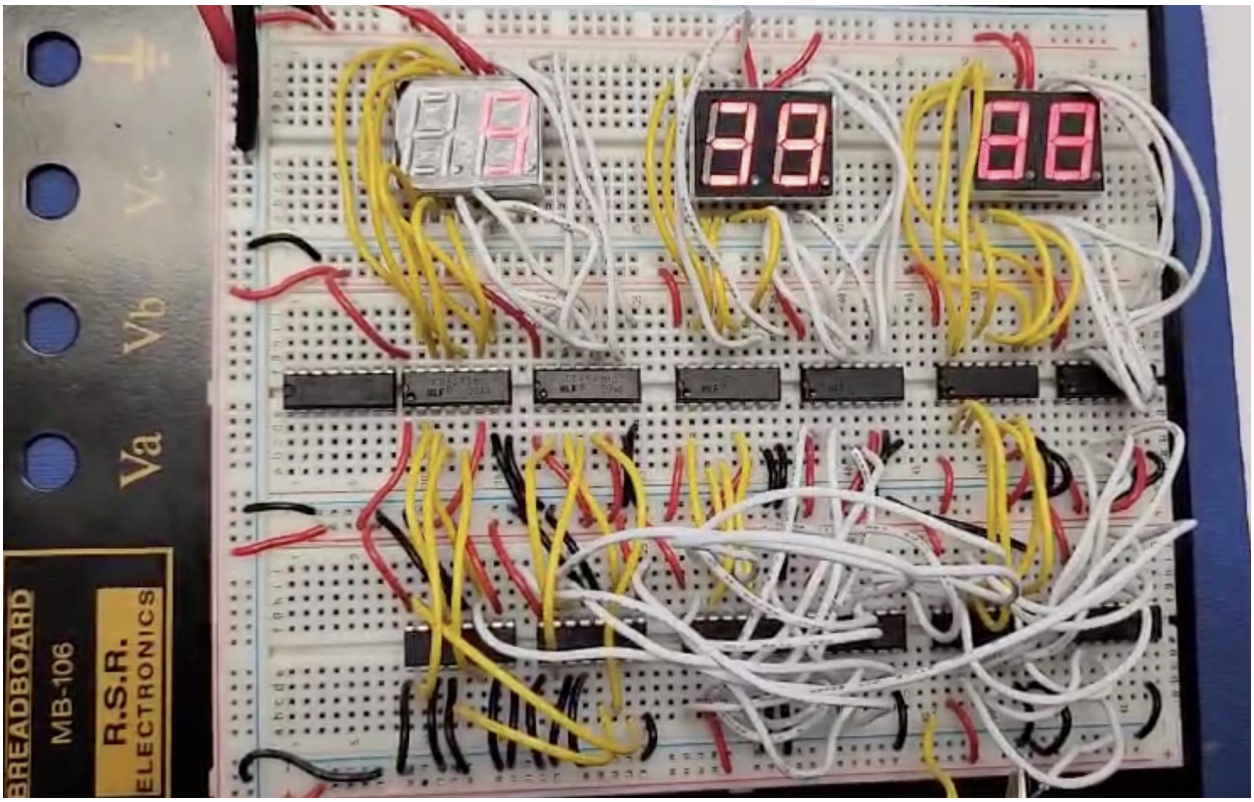


My final outcome is shown below



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Description for Hmys

After constructing the hmys circuit and performing extensive troubleshooting, the initial behavior was inconsistent and did not match the expected output. The hyms display initially counted from 0 to 9 and then remained stuck at 9, while the minutes counter continued cycling. After the minutes counter completed three full cycles, the hyms display would reset to 0 and begin counting again. The circuit utilized a seven-segment display, two CD4510 BCD counters cascaded together, a CD4543 BCD to seven-segment driver, and cascading logic connected to the minutes counter through an AND gate. During early testing, only the right side of the seven-segment display illuminated. This issue persisted despite confirming correct wiring connections and adjusting wire placement. Additional troubleshooting steps included re stripping wires, replacing wires, and verifying power and signal continuity. Although the display was partially functional, the hyms counting behavior was irregular, incrementing after extended time intervals and skipping expected values. Further investigation revealed that the irregular counting and incomplete display illumination were caused by unstable breadboard connections and wire contact issues. After re-routing signal wires, improving wire contact angles, and rechecking cascading connections between the CD4510 counters and the minutes logic, the HMYS circuit began operating more consistently. The display successfully counted in uniform increments as intended, advancing appropriately based on the minutes carry out signal. To isolate the issue further, the seven-segment display was tested independently in a separate breadboard setup, confirming that the display itself was fully functional. Once the wiring and cascading logic were corrected, the hyms

circuit demonstrated reliable counting behavior and a proper display. This process highlighted the sensitivity of digital systems to wiring integrity and emphasized the importance of systematic debugging when implementing complex cascaded counter circuits.

Results and Observations

The digital clock circuit was successfully constructed and tested through a combination of sketching, hardware implementation, and iterative troubleshooting. Initial testing revealed inconsistent counting behavior and incomplete seven-segment display activation, particularly within the hyms stage. These issues were traced to unstable breadboard connections and cascading logic sensitivity, which are common challenges in complex digital systems. After systematically verifying IC pin connections, cascading logic, clock inputs, and power distribution, the circuit achieved stable and predictable operation. The counters advanced correctly based on the applied clock signal, and carry over between stages functioned as intended. Once wiring integrity was improved, the hyms display incremented uniformly in response to the minutes counter and reset appropriately at the correct count. Overall, the hardware behavior closely matched expectations. The project demonstrated the importance of careful wiring, signal integrity, and structured debugging when working with cascaded digital logic. Minor issues encountered during implementation reinforced real world considerations.

References

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