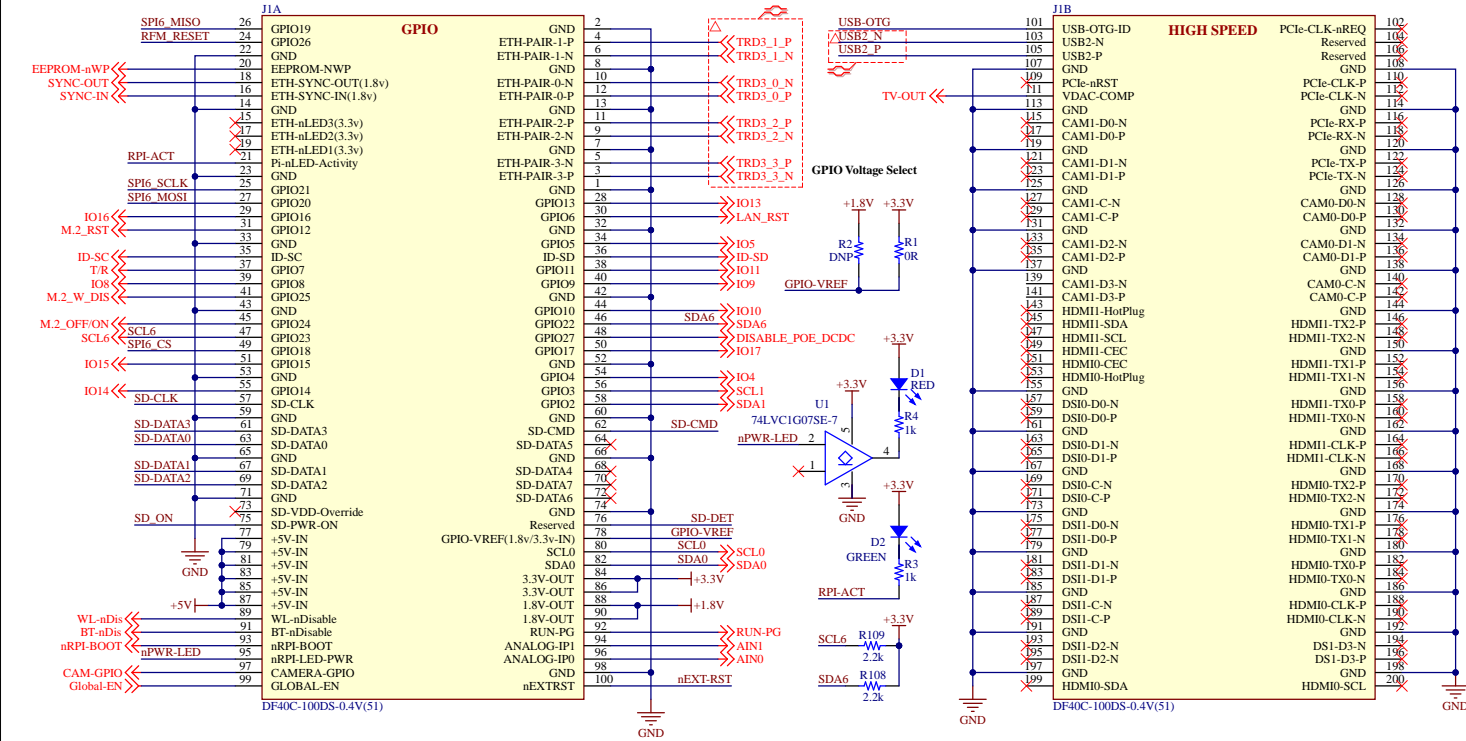


RPI-CM4



The image displays three circuit diagrams for the AP64501SP-13 buck converter, which is a 500mA, 12VDC-to-5VDC/3.3VDC converter. The diagrams are labeled 1, 2, and 3 in the top right corner.

Diagram 1: 12VDC to 5VDC
 This diagram shows the converter outputting 5VDC. The input is 12V_SYS. The output is 5V, connected to a green LED (D5) and a 330R resistor (R15). The output filter capacitor is C42 (220uF). The feedback network consists of R20 (115k) and R101 (22.1k). The output current is 5A.

Diagram 2: 12VDC to 3.3V DC #1
 This diagram shows the converter outputting 3.3VDC. The input is 12V_SYS. The output is 3V3_M2+PCIE. The output filter capacitor is C32 (220uF). The feedback network consists of R21 (47k) and R22 (15k). The output current is 5A.

Diagram 3: 12VDC to 3.3V DC #2
 This diagram shows the converter outputting 3.3VDC. The input is 12V_SYS. The output is +3.3V. The output filter capacitor is C49 (220uF). The feedback network consists of R28 (47k) and R29 (15k). The output current is 5A.

All diagrams use the AP64501SP-13 converter, which has pins VIN, EN, SS, FB, COMP, EP, and GND. The input capacitors are C12, C27, C28, and C31 (all 100uF). The output capacitors are C35, C41, and C42 (all 220uF). The feedback capacitors are C24, C34, and C51 (all 220uF). The feedback resistors are R27 (15.8k), R24 (15.8k), and R30 (15.8k). The output filter capacitors are C29, C38, and C47 (all 0.1uF). The output filter inductors are L1, L2, and L3 (all SRN6045TA-3R3Y).

The schematic diagram illustrates the LED driver circuit for the LED strip. It features two identical LED driver stages, each powered by a +3.3V supply. The first stage (top) includes a MAX33072EASA+ LED driver IC (U22), a CDSOT23-SM712 LED (D19), and a SMAJ12CAHE3/5A diode (D17). The second stage (bottom) includes a MAX33072EASA+ LED driver IC (U23), a CDSOT23-SM712 LED (D20), and a SMAJ12CAHE3/5A diode (D18). The circuit also includes a 691311500106 connector (J2) for the LED strip.

M.2 CONNECTOR

Quectel RM520N-GL Module

The diagram illustrates the M.2 connector for the Quectel RM520N-GL module. It shows the connection of the module's pins to the PCB. Key components include capacitors C71, C72, C73 (0.1uF), C121, C122, C5 (0.1uF), and C7. The module is connected to the 3V3_M2+PCIE power supply, HD7_P, HD7_N, and USIM_VDD. The module's pins are labeled P7_P, P7_N, P7_RST, P7_CLK, P7_DATA, and P7_DET. The module is also connected to the WWAN_LED1 and WWAN_LED2 LEDs. The module is connected to the 3V3_M2+PCIE power supply via a 180R resistor (R77). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R78). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R79). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R80). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R81). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R82). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R83). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R84). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R85). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R86). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R87). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R88). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R89). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R90). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R91). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R92). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R93). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R94). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R95). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R96). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R97). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R98). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R99). The module is connected to the 3V3_M2+PCIE power supply via a 10k resistor (R100).

MINI PCIE CONNECTER

SWARM M138 Modem

SWARM M138 Modem

J14

3V3_M2+PCIE

WAKE#

RESERVED

RESERVED

RESERVED

RESERVED

GND

UART_RX

UART_TX

GND

RI

RESERVED

GND

UART_CTS

UART_RTS

GND

29

GND

DTR

RESERVED

GND

GND

VCC_3V3

VCC_3V3

GND

PCM_CLK

PCM_DOUT

PCM_DI

PCM_SYNC

VCC_3V3

VCC_3V3

GND

USIM_VDD

USIM_DATA

USIM_CLK

USIM_RST

RESERVED

GND

W_DISABLE#

PERST#

RESERVED

GND

NC

I2C_SCL

I2C_SDA

GND

USB_DM

USB_DP

GND

LED_WWAN

USIM_PRESENCE

RESERVED

NC

GND

VCC_3V3

3V3_M2+PCIE

WWAN_LED2

3V3_M2+PCIE

GND

3V3_M2+PCIE

C118

C119

C120

0.1uF

10uF

10uF

GND

GND

GND

D16

GREEN

R81

180R

WWAN_LED2

679105700

MISCCELLANEOUS

The circuit generates a pulse when GLOBAL_EN when nRTC_INT goes low
GLOBAL_EN needs to be pulse low for >1ms

RTIC alarms can be used to wake up the Compute module
NB An Alarm triggering while already awake will cause a reset
This can be used as a watchdog reset

RTC Clock

IIC address : 1010_001x

U6
OSCI SCL SDA
OSCIO CLKO INT
VSS

PCF85063AT/AZ

+3.3V
BATT1 3034
GND
D6 BAT54C-7-F
C22 0.1uF
32.768KHz
X2
GND
nRTC-INT
SCL6
SDA6
RUN-PG
U8 74LVC1G07SE-7
+5V
AIN0
SYNC-OUT
TV-OUT
Global-EN
Header 2x7
J10
1 2
3 4
5 6
7 8
9 10
11 12
13 14
rRPI-BOOT
EEPROM-nWP
AIN1
SYNC-IN

Pressure & Temp. Sensor

A1
CS INT/SDO SDA/SDI SCL/SCLK
NC NC
ENS220S-BLGT
IIC address : 0x20

+3.3V
R32 R33
nf nf
SCL1
SDA1
VDD
GND
GND
GND
+1.8V
C153 0.1uF
GND

FAN Controller

U9
nALERT CLK
SCL TACH
VDD PWM
GND
EMC2301-I-ACZL-TR
IIC address : 0101_111x
Also SMBUS alert IIC address : 0001_100x

+3.3V
C30 0.1uF
GND
SDA0
SCL0
+5V
P2 MHDRIx4
1 2 3 4
+5V
SCL6
SDA6
Global-EN
RUN-PG
Header 1x3
J12
1 2 3
Header 1x3
J13
1 2 3
WL-nDis
BT-nDis

Spare GPIOs

J23 Header 2x7
1 2 3 4 5 6 7 8 9 10 11 12 13 14
ID-SC- ID-SB- IO13 CAM-GPIO
GND
3V3
J16 Header 1x3
1 2 3
+5V
12V_SYS
J11 Header 1x4
1 2 3 4
GND

I2C Out for OLED 0.96in

P2 MHDRIx4
1 2 3 4
+5V
SCL6
SDA6
Global-EN
RUN-PG
Header 1x3
J12
1 2 3
Header 1x3
J13
1 2 3
WL-nDis
BT-nDis

Global-EN Logic

nRTC-INT
R16 510k 1%
C18 0.1uF
R17 510k 1%
U7 74LVC1G07SE-7
Global-EN

Title	Size	Number	Revision
	A3		

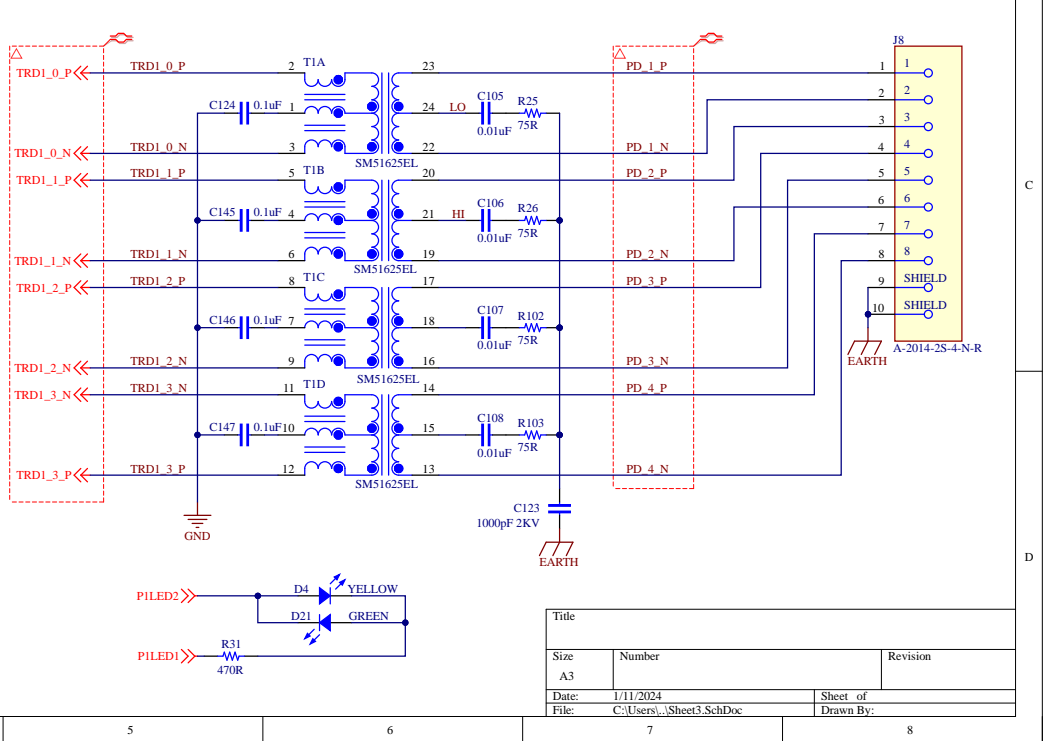
Title		
Size A3	Number	Revision
Date:	1/11/2024	Sheet of
File:	C:\Users\...Sheet2.SchDoc	Drawn By:

Ethernet 2 (Debugg)

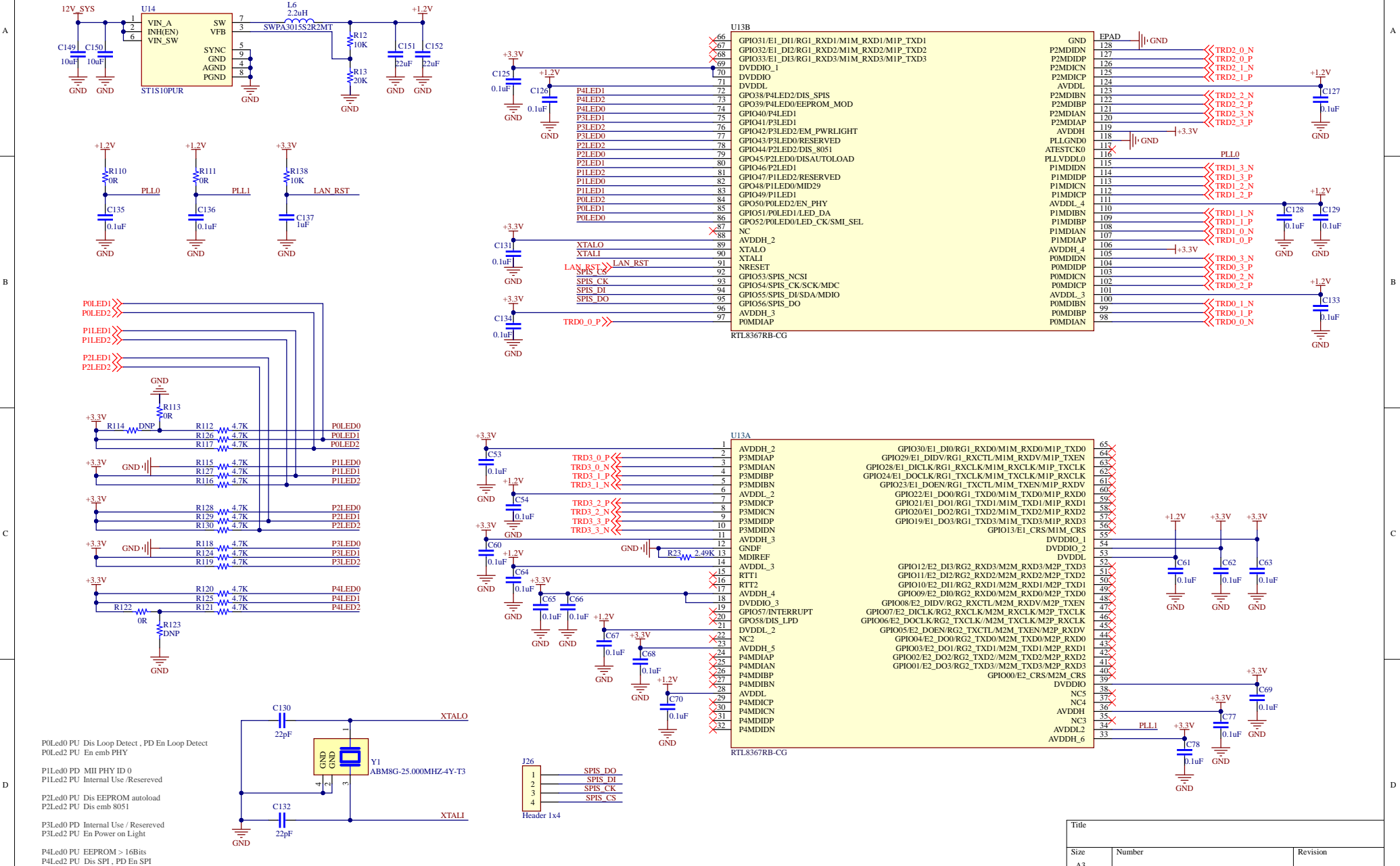
The diagram illustrates the internal wiring of a debug board for Ethernet 2. It features two USB-to-Ethernet adapters, TPD4EUSB30DQAR, connected to a central Ethernet switch, V890-1AX1-A1. The adapters are connected via D28 and D30 connectors. The switch is connected via J18. The diagram shows the internal wiring of the adapters, including the USB pins (NC_6, NC_7, NC_9, NC_10) and the Ethernet pins (TRD2_0_P, TRD2_0_N, TRD2_1_P, TRD2_1_N, TRD2_2_P, TRD2_2_N, TRD2_3_P, TRD2_3_N). It also shows the power and ground connections, a 0.1uF capacitor (C148), a 470R resistor (R106), and LEDs (P2LED1, P2LED2). The ground connection is labeled EARTH.

[illegible]

Ethernet 1 (Camera POE Out)

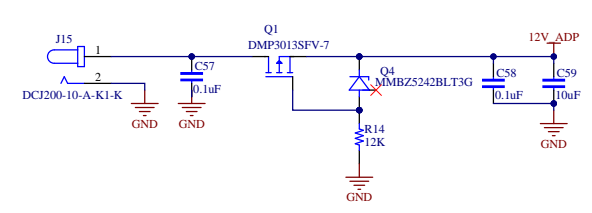


LAN Switch

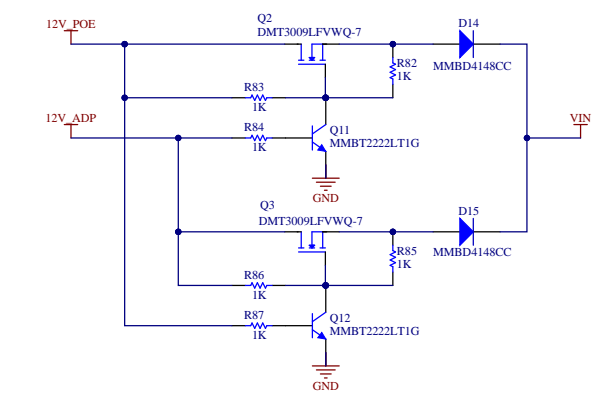


Title		
Size	Number	Revision
A3		
Date:	1/11/2024	Sheet of
File:	C:\Users\...\Sheet4.SchDoc	Drawn By:

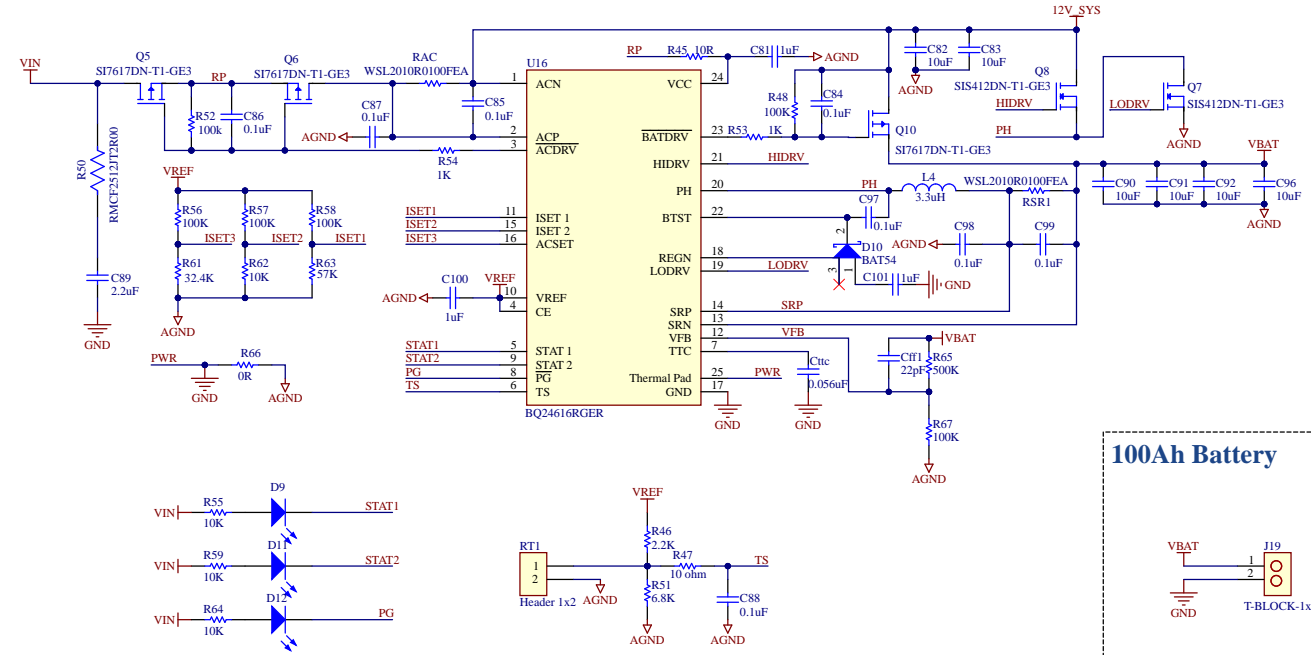
DC Adapter IN



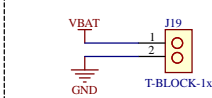
Power Selector



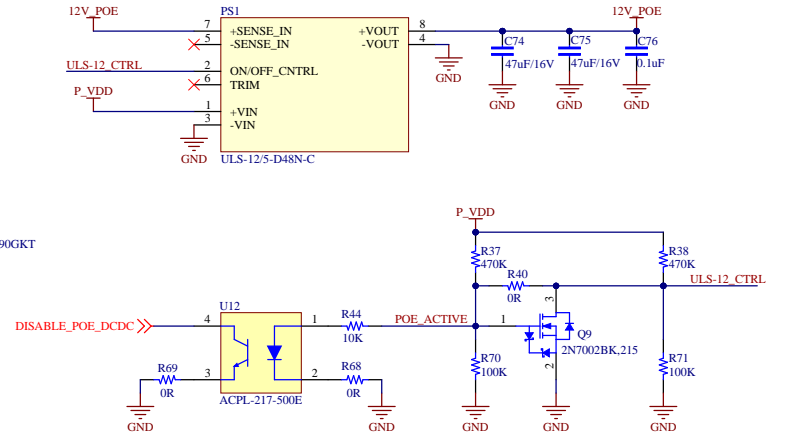
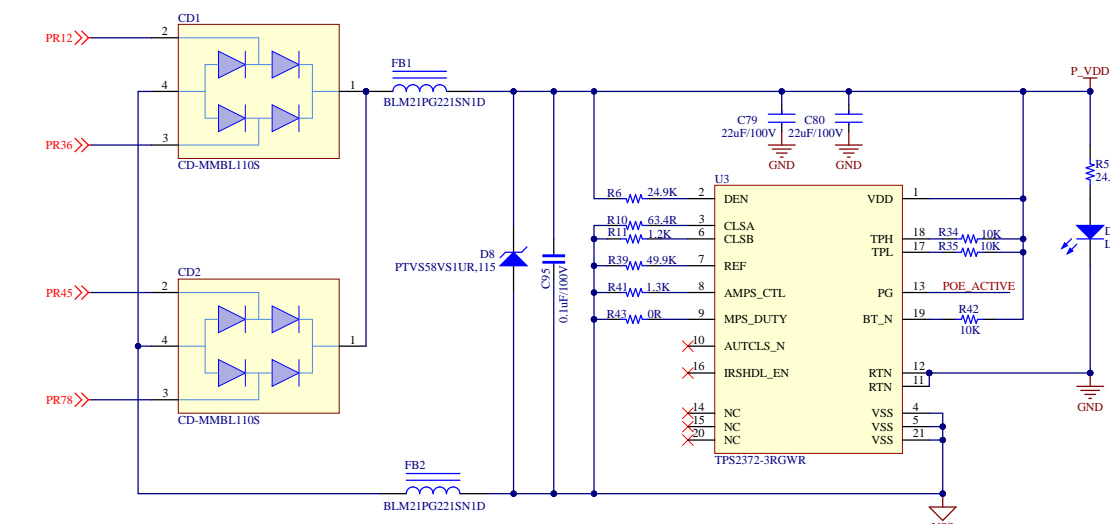
Battery Charging



100Ah Battery



POE to 12V DC DC Converter



Title		
Size	Number	Revision
A3		
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