UNIVERSITY OF TEXAS ARLINGTON

CSE 4323
Quantitative Computer Architecture

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Quiz Week 03

What is the execution time of a program with 1 million instructions with a CPI of 2 running on a processor at 2GHz?

Quiz Week 03

A program has 50% ALU, 15% Floating Point, 15% I/O, and 20% Memory operations. The Average CPI of ALU is 2, FP is 5, I/O is 20, and Memory is 50,

What is the overall CPI? Answer: [overallCPI]

What would be the new CPI if we improve the I/O and Memory CPIs to 10 and 25, respectively? Answer:[overallCPI2]

Quiz Week 03

Assume you have a fully parallelizable application. You run it on a 1 core processor at 1 GHz. It took 10 seconds to finish and consumed 100W power. You also found that the processor consumes 40W power when it is idle.

1. What will be the execution time and power consumption if you increase the processor's frequency to 4 GHz? What is the speedup? Note that only dynamic power changes with frequency change.

2. What will be the execution time and power consumption if you run the application on a 4-core processor at 1 GHz? Assume each of these processor cores is the same as the 1 core processor.

Quiz Week 03

You have a processor with two cores running at 3 GHz with 40W static power consumption per core. You run a program in one core (both cores are “ON”) and measure the total power as 140W.

1. What is the dynamic power of each core? Assume the two cores are identical. Answer: Power = _____ W
2. Assume that the initial program took 10 seconds to finish. You then improve the program; it can run in multiple cores in parallel (i.e., fully parallelizable). What is the new execution time of the program in your dual-core processor? Answer: Execution time = _____ seconds
3. For the improved program, you care more about reducing power consumption instead of execution time. You reduce the frequency to reduce the power while maintaining the initial 10 seconds execution time. At what frequency do you run the processor? What are the per-core dynamic power and total power of the processor now? Assume when you change frequency, the voltage also changes proportionally. Answer: Frequency = _____ GHz, dynamic power = _____ W, Total power = _____ W

Ouiz Week 03

You have a program that runs on I/O and a processor. On your current system, it has an execution time of 100 seconds. You need to decide which part of your system you need to invest in to improve the overall execution time. You can put a new processor that is 20X faster or a new I/O system that is 100X faster. However, you do not know the fraction of time the program spends on the processor or the I/O. But you have a 0.5X processor from your old system, and you put the old processor in the current system. You see that the execution time of your program is 160 seconds now. Using these observations answer the following.

1. Find the fraction of time the program spends on the processor of your current system? Answer: CPU fraction = _____ %

2. What is the minimum execution time you can achieve on your current system if you only improve the processor and leave the I/O as is? Answer: Minimum execution time = _____ seconds

Quiz Week 03

You have a 1 core and an 8 core processor. You also have two programs P#1 and P#2. You get the following execution time (in seconds) for the two programs on the two processors.

	1-Core	8-Core
P#1	100 s	30 s
P#2	160 s	90 s

How much of P#1 and P#2 are parallelizable?

Actual size of cache

- We need to store the tag of each cache block
- There is one extra ”valid” bit to mark if we should trust the tag
- How many total bits are needed for a direct- mapped cache with 64 KBytes of data and one-word blocks (4 bytes), assuming a 32-bit address?
  - 64 Kbytes = 16 K words = 2^14 words = 2^14 blocks
  - block size = 4 bytes => offset size = 2 bits,
  - #sets = #blocks = 2^14 => index size = 14 bits
  - tag size = address size - index size - offset size = 32 - 14 - 2 = 16 bits
  - bits/block = data bits + tag bits + valid bit = 32 + 16 + 1 = 49
  - bits in cache = #blocks x bits/block = 2^14 x 49 = 98 Kbytes

Quiz Week 04

Write the number of bits for the memory address blocks (Tag, Index, and Offset) for the below cache configurations. Also, determine the actual number of bits per block and cache sizes. Round the cache size to the nearest power of 2 (e.g., 1KB = 2^10) and assume a 32-bit memory address.

(a) 128KB cache, 32-byte block, 4-way associative

Tag: [tag1]	Block index: [idx1]	Block offset:[offset1]

Actual number of bits per block = [bits1]

Actual cache size = [size1]

(b) 256 KB cache, 128-byte block, 4-way associative

Tag: [tag2]	Block index: [idx2]	Block offset:[offset2]

Actual number of bits per block = [bits2]

Actual cache size = [size2]

Problems in the sample exam

Problem 2:

A program has 50% ALU, 20% Floating point (FP), 20% Memory, and 10% I/O operations. The average CPI of ALU, FP, Memory, and I/O is 2, 10, 25, and 50, respectively.

a) What is the overall CPI of this program? (8 points)

Overall CPI = 50%*2 + 20%*10 + 20%*25 + 10%*50 = 13

b) Assuming the CPI in the previous problem is for no cache misses for memory access, what will be the new average CPI if there are 2% misses in the instruction cache and 10% misses in the data cache with miss penalty of 50 cycles for all misses? (12 points)

Instruction miss CPI = 2% * 50 = 1
Data miss CPI = 10% * 20% * 50 = 1
New CPI = 13 + 1 +1

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Problem 3: You have a program that is 80% parallelizable (segment of code that can run on multiple processors). You run it on a single core processor at 4 GHz with an execution time of 160 seconds.

a) What is the speedup if you run this program on a 4-core processor running at 2 GHz? (6 points)

E_new_4_core = 160 * 80%/4 + 160*20% = 64 seconds
E_new_4_core_2Ghz = 64*4/2 = 128 seconds
Speedup = 160/128 = 1.25

b) If you do not care for speedup (i.e., speedup =1), but rather want to reduce the power at what frequency you run the 4-core processor? Hint: find the frequency at which the execution time remains 160 seconds. (8 points)

F_new = F_old * E_new/E_old = 4 * 64/160 = 1.6 GHz

c) What is the new dynamic power of each core of the 4-core processor if the dynamic power was 100W when running at 4 GHz? (6 points)

P_new = P_old * f_new^3/f_old^3 = 100 * 1.6^3/4^3 = 6.4 W

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Problem 4:

a) What is the cache size (for data) and actual cache size (data + cache overhead) for the following 4-way associative cache organization. Round the cache size to nearest power of 2 (e.g., 1KB = 2^10). Hint: start with finding the number of blocks utilizing the cache organization and number of bits used for Idx. (10 points)

Tag = 8	Idx = 10	Offset = 6

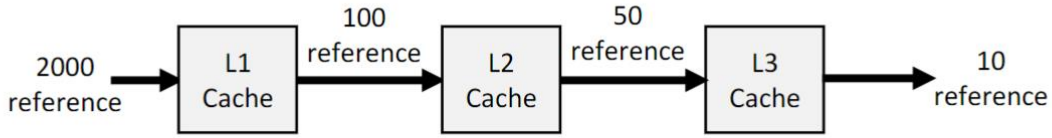
Block_size = 2^offset = 2^6 = 64 bytes

#block = ?
#sets = #block/#way
Idx = log_2(#sets) = log_2(#block/#way)
=> #block = #way * 2^(idx) = 4 * 2^(10) = 4096

cache size = #block * block_size = 4096 * 64 bytes = 262144 bytes = 256KB

actual_bits_per_block = block_size + tag + dirty_bit = 64*8 + 8 + 1 = 521
actual cache size = #block * actual_bits_per_block = 2134016 bits = 266752 bytes = 260.5 KB

a) Suppose that in 2000 memory references there are 100 misses in the first-level cache, and 50 misses in the second level, and 10 misses in the third level cache. The misses are shown in the diagram below.



Hit times for L1, L2, and L3 are 1, 5, and 10 cycles. Miss penalty for L3 is 100 cycles. What is the memory access time in clock cycles? (10 points)

Memory access time = L1_hit + L1_miss * (L2_hit + L2_miss*(L3_hit+L3_miss * L3_miss_penalty)))
= 1 + 100/2000 * (5 + 50/100 * (10 + 10/50 * 100)) = 2 cycles

Problem 5: Fill the empty places between the "< >" signs with the bit length (i.e., how many bits) for the bellow virtual memory organization with 1 GB of memory. The virtual address is **32 bits**. The page size is **4KB** (2^12). The TLB is **direct-mapped** with **256 (2^8)** entries. Note that, the number of bits for physical address is determined by the physical memory size. (20 points)