All-Analog Current Repeater for Scalable Photonic Neural Networks

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Abstract: We propose an all-analog current repeater for use in highly scalable Photonic neural networks. This circuit samples and indefinitely reproduces photodetector currents. It is fully parallelizable and compatible with constant value and spiking architectures.
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1. Introduction

Photonic neuromorphic systems have been shown to have a number of advantages over pure software neural networks and electronic neuromorphic systems [1]. These benefits are most pronounced when processing data in the optical or electrical analog domains, such as the fiber nonlinearity compensation system described in [2]. While this technology enables high speed real-time inference, it is limited in system and network size due to the signal losses that are incurred by decreasing the size of photonic waveguides. [3] demonstrated the solution that is briefly detailed in Fig. 1 to allow inferences to be computed one layer at a time, enabling both a significantly higher fan-in and the potential for much greater depth at the expense of a slowdown that grows linearly with each pass.

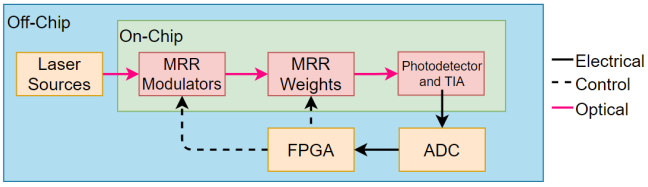

Fig. 1. Highly scalable photonic neural network proposed in [3].

This new potential for increased complexity warrants an exploration of other computational techniques, so as to ensure that inference time increases as little as possible with network size. Because [3] lists the major bottleneck of their system to be the digitization of each layer's output vector, a natural next step would be to begin nurturing the parallelization and analog-domain execution of the sampling process. These two efforts compliment each other well, as integrated analog circuitry is far smaller and easier to parallelize than digital circuitry that accomplishes the same task [4, 5].

In this paper, we propose and verify the function of an all-analog electronic circuit that is designed to replace the digitizing components of the system discussed in [3]. This circuit can be inserted between the photonic dot product engine and laser output of an integrated photonic processing network node, and is designed to be compatible with both constant value and spiking neuron architectures. The proposed circuit uses a time-integrating capacitor to sample the input current from a network node's bipolar photodetector, which is then stored as a voltage and reproduced through the network's output laser diode. By using this process, the network node's input and output are buffered, allowing the output to feed back into the input after the weight banks are changed so as to compute the output vector for the next layer in the network.

2. Experimental Setup

Fig. 2 shows a schematic of the proposed current repeater circuit. The output current from the photodiode is directed using MOSFET switches, allowing for a small sample period where it is pumped into the sample capacitor C_S. This sample period produces a voltage across the capacitor that is proportional to the time average of the input current, with the ratio of the sample time to the capacitance of C_S being the constant of proportionality. Once the sample period has finished, the latch MOSFET can be turned on, equalizing the latch capacitor voltage with that of the sample capacitor. This also changes the current being pulled through the output laser to be proportional to the stored voltage, with the resistance R_{Out} acting as the constant of proportionality. For this experiment, reciprocal constants of 100 and 1/100 were chosen so that the input current would be reproduced exactly while keeping key measurement voltages in an observable range. Once the saved output is sufficiently close to the sampled input, the latch MOSFET can be turned back off, and the drain MOSFET can be used to bring the sample capacitor voltage back to 0V to be reused. To increase the speed of operation for this circuit, it is best to drain the sample capacitor to some small negative value, such that it is capable of reaching 0V rather than asymptotically approaching it.

To verify the function of this circuit, a laser diode can be made to drive the input photodetector, and the resulting current can be reproduced and measured. In order to ensure that the input currents being examined are evenly

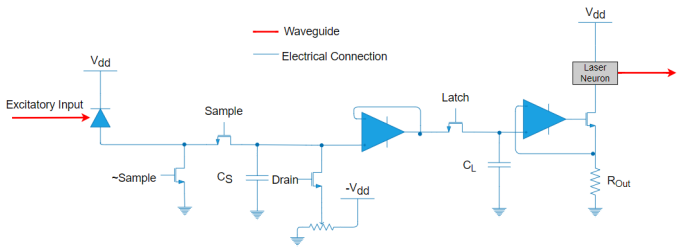

Fig. 2. Schematic for current sampling and repeating circuit.

distributed throughout the domain of possible values, a control system can be made to let this optical input circuit supply a constant current value. This constant current can then be randomly modulated before each cycle of the latching and reproduction process.

3. Results and Analysis

Fig. 3 shows the time domain behavior of the current repeater circuit. Between each interaction, the input current is set to a random value between 0 and 4mA. The current is then given time to settle before being sampled and reproduced. This delay is a result of the test circuitry, and should not be taken as evidence of low execution speeds for the circuit. Once the input current has stabilized, it is routed to the sample capacitor for a sample period. After the sample period is finished, the latching capacitor and output current are both changed to be equal with the sample capacitor's value, and the sample capacitor is drained for reuse.

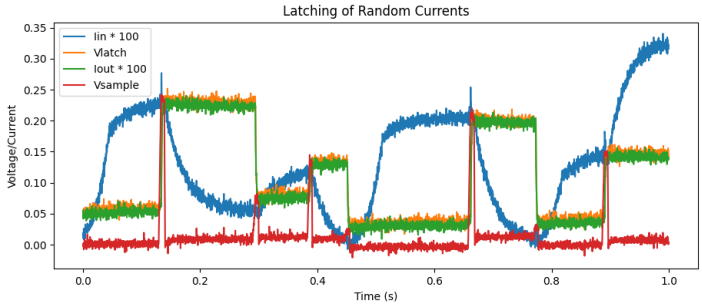

Fig. 3. Time-domain behavior of the design under test.

Statistically analyzing 491 of these interactions shows with 95% confidence that, excluding extreme outliers, the circuit is able to reproduce an input current with between 4.93% and 7.74% of the input current's amplitude in error. While some of this error may be due to device non-idealities, it is likely that using faster control circuitry and fine-tuning the sample time would decrease this error significantly, as the distribution of errors collected is negatively skewed. This test also showed with 95% confidence that the circuit is able to save and reproduce a current within 8.5322ms. This time can be dramatically decreased by constructing the circuit with the lower resistances and capacitances that are achievable in integrated electronics.

4. Conclusion

We propose and verify the function of an all-analog current repeater for use in highly scalable photonic neural networks. This circuit samples and indefinitely reproduces photodetector currents with between 4.93% and 7.74% error in less than 8.5322ms during testing. It is fully parallelizable and compatible with constant value and spiking architectures. This, along with the inherent speed of analog execution over digital, could stand to decrease the rate of growth in inference time with respect to cycle count of scalable photonic neural networks.

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