# **James Garofolo**

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in /in/james-garofolo/ | D James Garofolo | D James-Garofolo

### **EDUCATION**

**Rowan University** 

Candidate for Master of Science in Electrical and Computer Engineering GPA 4.0/4.0

Sep. 2022 – Present Glassboro, NJ

**Rowan University** 

Bachelor of Science in Electrical and Computer Engineering GPA 3.831/4.0

Sep. 2018 – 2022 Glassboro, NJ

### **PUBLICATIONS**

- J. Garofolo, Y. Qi, T. Shi, G. Tian and B. Wu, "Photonic Interference Cancellation for LiDAR Sensors," in IEEE Photonics Technology Letters, doi: 10.1109/LPT.2023.3316592.
- J. Garofolo, Y. Qi, T. Shi, and B. Wu, "Jamming-Resilient LiDAR based on Photonic Blind-Source Separation," in Frontiers in Optics + Laser Science 2022 (FIO, LS), Technical Digest Series (Optica Publishing Group, 2022), paper JW5A.47.
- J. Garofolo and B. Wu, "All-Analog Current Repeater for Scalable Photonic Neural Networks," in Frontiers in Optics + Laser Science 2022 (FIO, LS), Technical Digest Series (Optica Publishing Group, 2022), paper JW5A.30.

#### **SKILLS**

Embedded Software: Verilog HDL, C, C++, and Coridium Basic

Scripting Software: Matlab, Simulink, Python, Numpy, SKLearn, Pytorch, Tensorflow

Machine Learning: Statistical Analysis, Linear/Logistic Regression, Clustering, Deep Learning

Hardware Design: Spice Circuit Simulators, Keysight Advanced Design System, VLSI Design with Cadence

Hardware Testing: Oscilloscopes, Electrical and Optical Spectrum Analyzers, Optical Fiber Communications Equipment

**PROJECTS** 

## Surface Electromyography Pattern Recognition for Robotic Prostheses

 Designed a multilayer perceptron to classify patterns in surface electromyography time series data for use in actuating a robotic prosthetic arm

#### Silicon-Level Digital Circuit Design

• Designed a dynamic D-Flip-Flop for high-throughput using logical effort delay estimation, implemented the design using Cadence Design Systems Virtuoso platform, and evaluated the design with the Spectre X circuit simulator

### **Computer Architecture using Field-Programmable Gate Arrays**

Programmed a DE10-Lite FPGA development board to function as a 64-Bit Microprocessor using Verilog HDL

#### **EXPERIENCE**

## **Rowan University**

Research Fellow and Teaching Assistant

Sept. 2022 - Present

Glassboro, NJ

- Gave lectures on AM and FM communication standards, circuit designs, and common practices
- Demonstrate the assembly and testing of LF and VLF band AM and FM receivers using waveform generators and oscilloscopes
- Designed and tested several electro-optical analog computing systems
- · Published one journal article and two conference papers on the topics of electro-optical analog computing

# QEI Corporation

May 2020 - Sept. 2020, Feb. 2022 - Sept. 2022

Embedded Systems and Software Engineer

Williamstown, NJ

- Designed stepper motor driver and position tracker boards using optical quadrature encoders for automated variable impedance matching networks
- Designed firmware to interface with stepper motor drivers, detect mechanical stopping points, and use voltage-current phase and magnitude sensors to minimize reflected power in a radio frequency power delivery system
- Created a code base for efficient, intuitive and maintainable user-interface design based off of python and the Pygame GUI package
- Designed and modified several graphical user interfaces for various models of HF and VHF band RF power supplies, and deployed them on touch-pad displays using Linux-based single-board computers