VLSI Mini-Project 4

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For this mini-project, we combined three major components: a supply voltage–independent bias current generator; a 7-bit DAC based on the recommended IEEE paper, and a low-voltage output current mirror to make the output current stable at a wide range of voltages.

We worked heavily on the input current generator for the DAC M-2M ladder network. We initially got the system running with an ideal current source, but couldn't figure out how to maintain low INL and DNL values when we added the bias current generator circuit. We tried various options for the input current but couldn't find a solution that worked. In hindsight we should've switched which DAC ladder configuration we were using when we ran into way too many issues. We did make the files for the other DAC configuration, but didn't get much better results, so we stuck with the IEEE paper configuration. We included one of the current mirrors we were looking into for the other ladder configuration in this paper.

We think the bad INL and DNL results are from the wrong width and length ratios in the DAC ladder. We initially thought it was an error with the voltage movement at the Ibias node connecting the ladder to the current generator, but after various attempts and recommended circuits by Brad we couldn't get the Monte Carlo simulations, without the ideal sources, back down to a reasonable INL and DNL. We did test multiple width and length ratios for the DAC ladder, but the errors worsened.

We did not get robust simulation results for the entire circuit under all of the specified conditions (monte carlo, robustness to input voltage, and output voltage swing) simultaneously. Instead, we have simulation results that show

1. The bias current generator produces a current output with less than 0.5% variation per volt which is fed through a pMOS cascoded current mirror into the DAC ladder. There is also no visible variation in the input current when the input node of the DAC ladder (into which the bias current is fed) varies between 0 and 0.5V. See Figure 3.
2. The output stage simulated in isolation has less than 0.5% variation per volt of output voltage swing, due to the pMOS cascoded current mirror on the output. See Figure 14.
3. When the DAC ladder was simulated in isolation with an ideal current source as the bias input and grounded outputs, it had extremely linear properties, with less than 0.2 LSB of differential or integral non-linearity after 10 monte carlo simulations. See Figures 10 and 11.
4. When we had the complete schematic with all the subcircuits included and ran Monte Carlo simulations there was a large current offset, but the output current still followed a linear equation with appreciable slope. See Figures 18 and 19.

Supply voltage–independent bias current generator

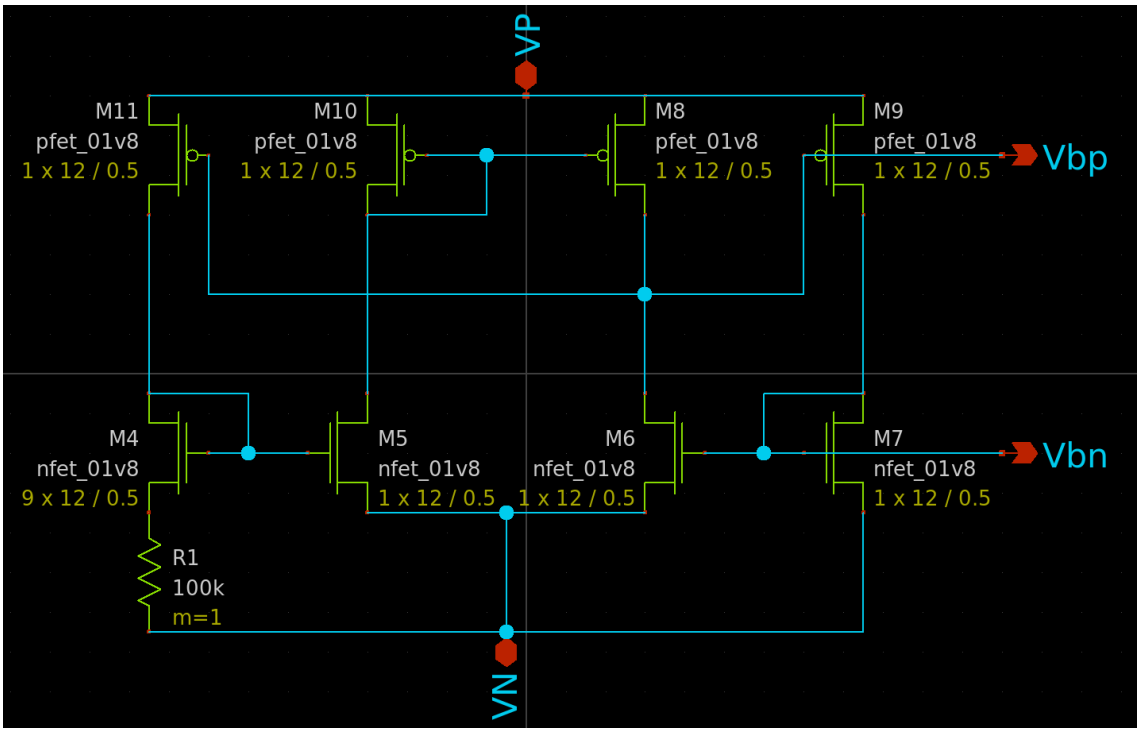

Figure 1. Bias current generator with pMOS and nMOS gate voltage output for current mirroring.

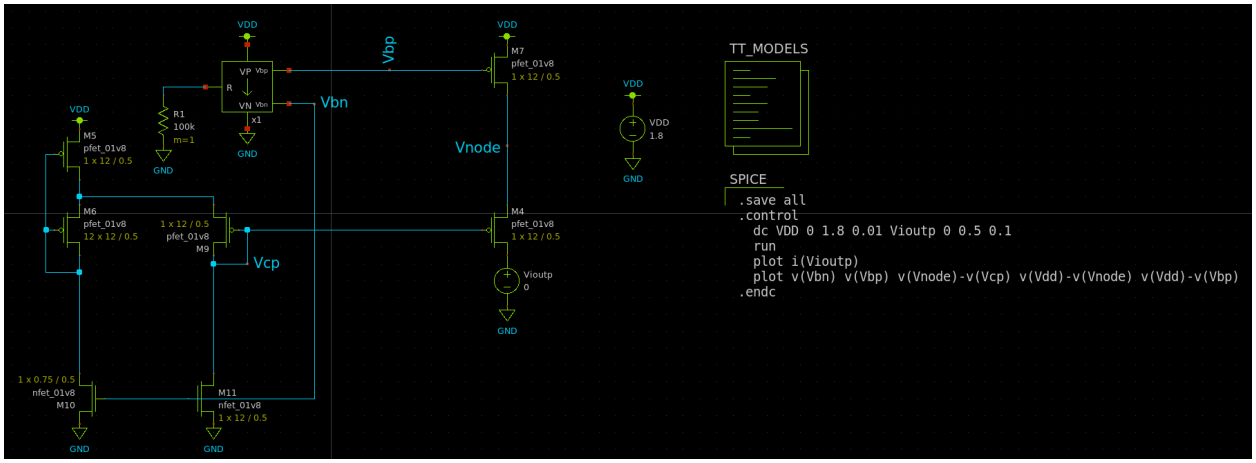

Figure 2. Current generator simulation schematic.

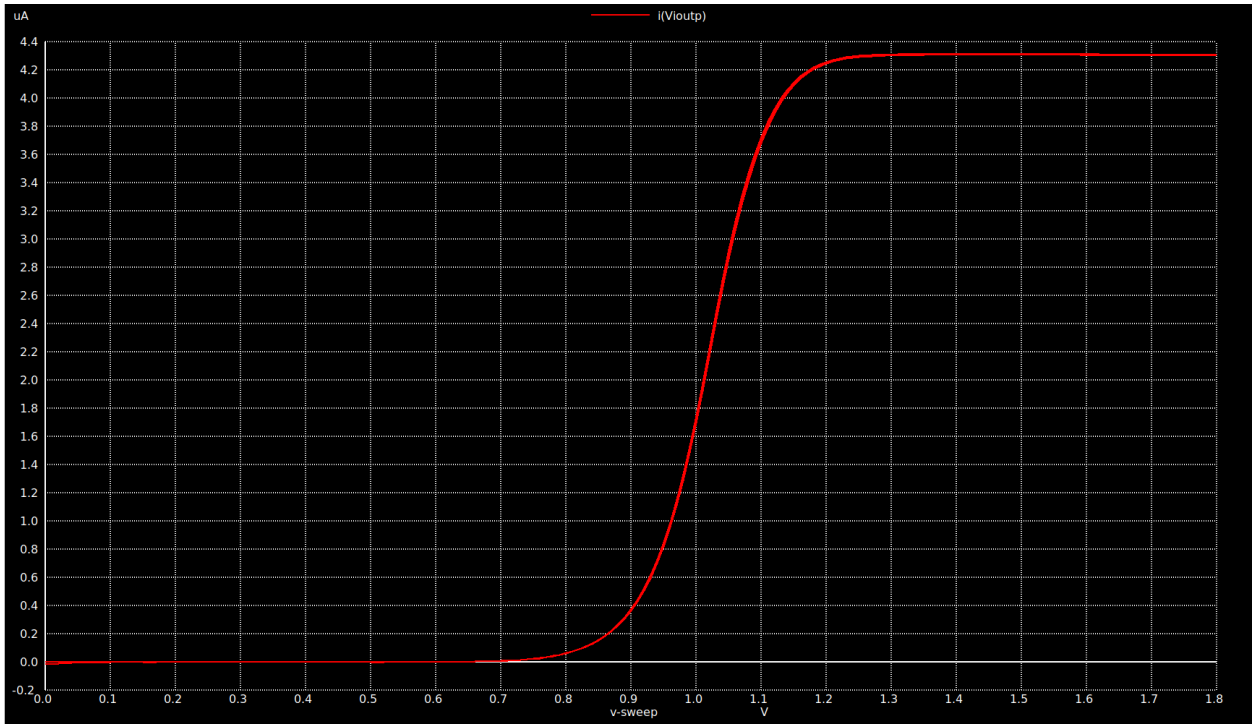

Figure 3. Current generator current output as we sweep VDD.

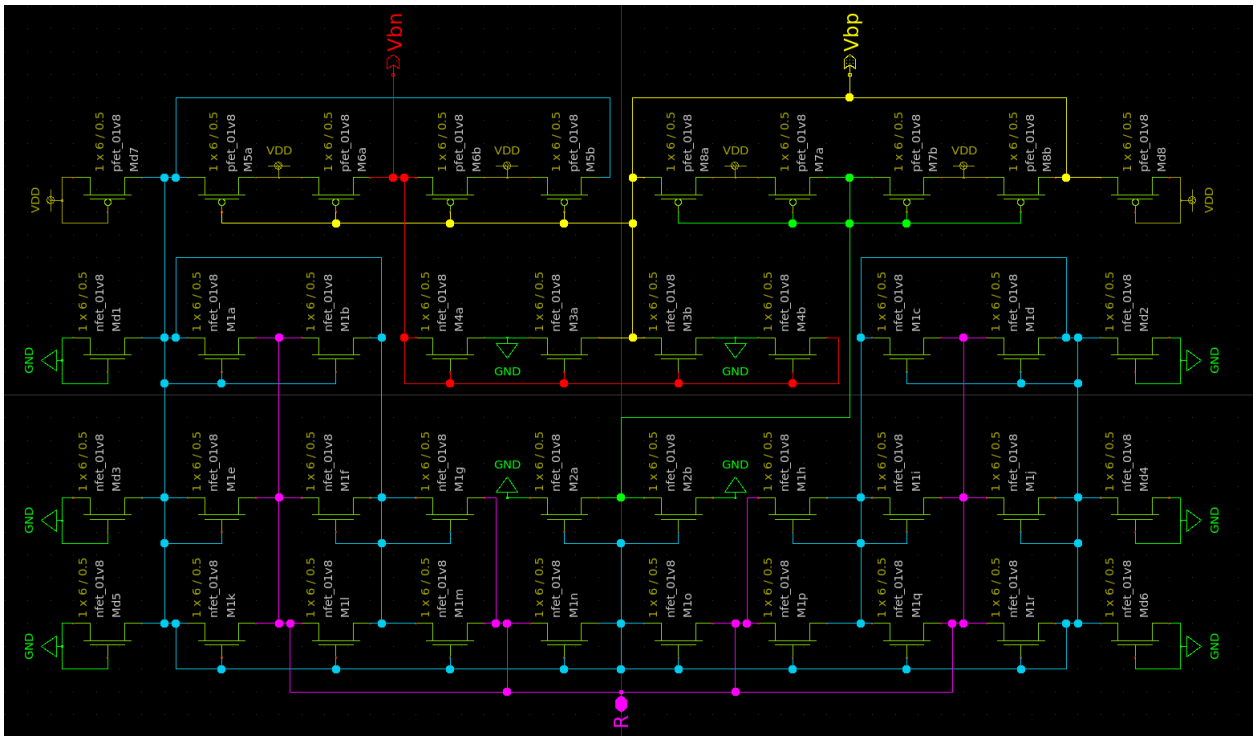

Figure 4. Layout-driven schematic for bias current generator.

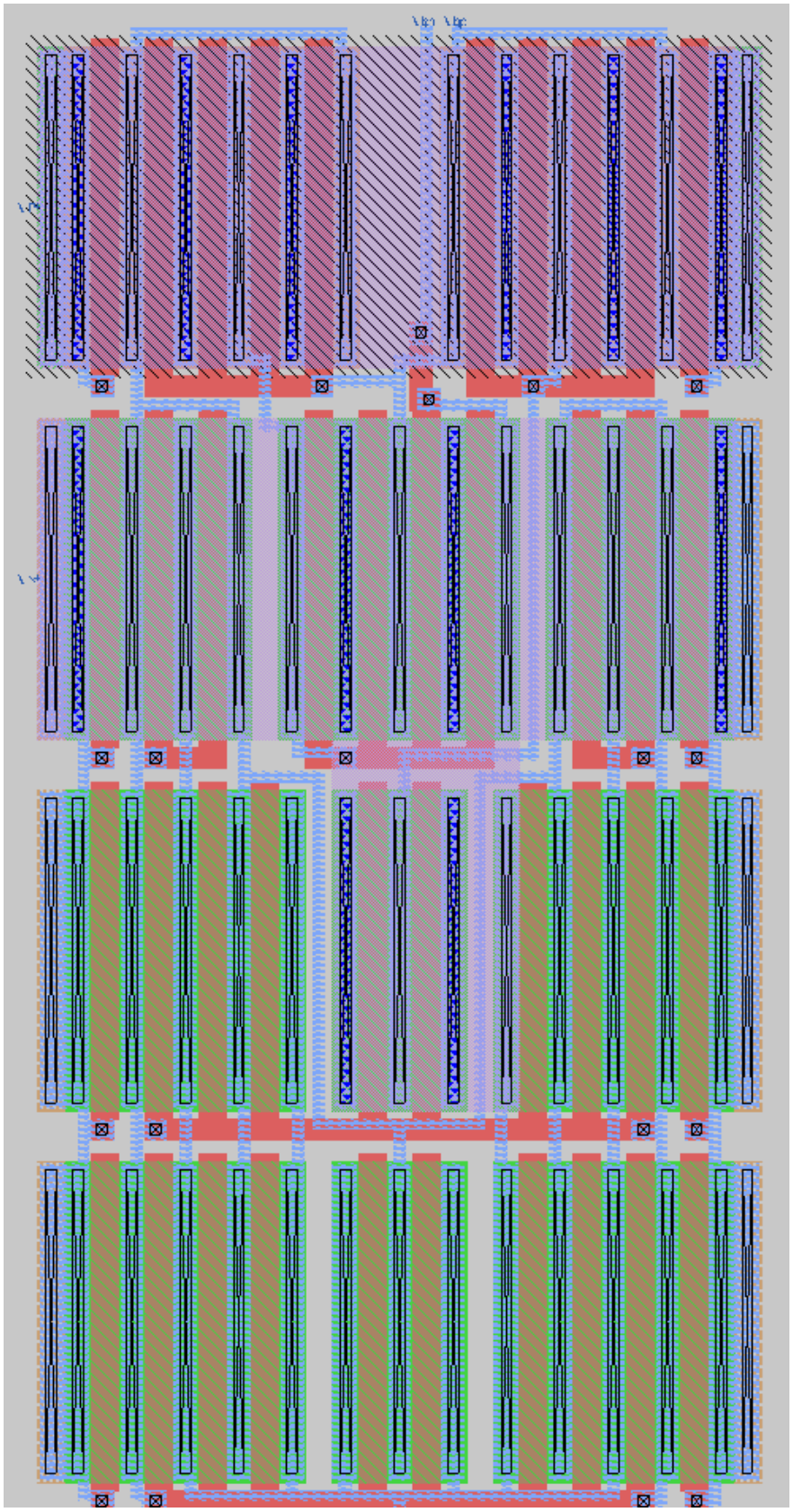

Figure 5. Magic layout for bias current generator.

Netgen LVS for bias current generator.

```
Netgen 1.5.257 compiled on Mon Sep  4 10:56:11 AM EDT 2023
Warning: netgen command 'format' use fully-qualified name '::netgen::format'
Warning: netgen command 'global' use fully-qualified name '::netgen::global'
Reading netlist file current_bias_magic.spice
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Reading netlist file current_bias_layout_driven.spice
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Cell current_bias_layout_driven.spice:  Net VDD changed to global
Cell current_bias_layout_driven.spice:  Net GND changed to global

Reading setup file
/home/madvlsi/skywater/open_pdks/sky130/sky130A/libs.tech/netgen/sky130A_setup
.tcl

Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__nfet_01v8
No property sa found for device sky130_fd_pr__nfet_01v8
No property sb found for device sky130_fd_pr__nfet_01v8
No property sd found for device sky130_fd_pr__nfet_01v8
No property nf found for device sky130_fd_pr__nfet_01v8
No property nrd found for device sky130_fd_pr__nfet_01v8
No property nrs found for device sky130_fd_pr__nfet_01v8
No property area found for device sky130_fd_pr__nfet_01v8
No property perim found for device sky130_fd_pr__nfet_01v8
No property topography found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property area found for device sky130_fd_pr__nfet_01v8
No property perim found for device sky130_fd_pr__nfet_01v8
No property topography found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__pfet_01v8
No property sa found for device sky130_fd_pr__pfet_01v8
No property sb found for device sky130_fd_pr__pfet_01v8
No property sd found for device sky130_fd_pr__pfet_01v8
No property nf found for device sky130_fd_pr__pfet_01v8
No property nrd found for device sky130_fd_pr__pfet_01v8
No property nrs found for device sky130_fd_pr__pfet_01v8
No property area found for device sky130_fd_pr__pfet_01v8
No property perim found for device sky130_fd_pr__pfet_01v8
No property topography found for device sky130_fd_pr__pfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property area found for device sky130_fd_pr__pfet_01v8
No property perim found for device sky130_fd_pr__pfet_01v8
No property topography found for device sky130_fd_pr__pfet_01v8
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
```

```
Circuit sky130_fd_pr__pfet_01v8 contains no devices.
Circuit sky130_fd_pr__nfet_01v8 contains no devices.

Contents of circuit 1:  Circuit: 'current_bias_magic.spice'
Circuit current_bias_magic.spice contains 40 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  30
  Class: sky130_fd_pr__pfet_01v8 instances:  10
Circuit contains 7 nets.
Contents of circuit 2:  Circuit: 'current_bias_layout_driven.spice'
Circuit current_bias_layout_driven.spice contains 40 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  30
  Class: sky130_fd_pr__pfet_01v8 instances:  10
Circuit contains 7 nets.

Circuit was modified by parallel/series device merging.
New circuit summary:

Contents of circuit 1:  Circuit: 'current_bias_magic.spice'
Circuit current_bias_magic.spice contains 11 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   5
  Class: sky130_fd_pr__pfet_01v8 instances:   6
Circuit contains 7 nets.
Contents of circuit 2:  Circuit: 'current_bias_layout_driven.spice'
Circuit current_bias_layout_driven.spice contains 11 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   5
  Class: sky130_fd_pr__pfet_01v8 instances:   6
Circuit contains 7 nets.

Circuit 1 contains 11 devices, Circuit 2 contains 11 devices.
Circuit 1 contains 7 nets,     Circuit 2 contains 7 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

7-bit DAC based on recommended IEEE paper

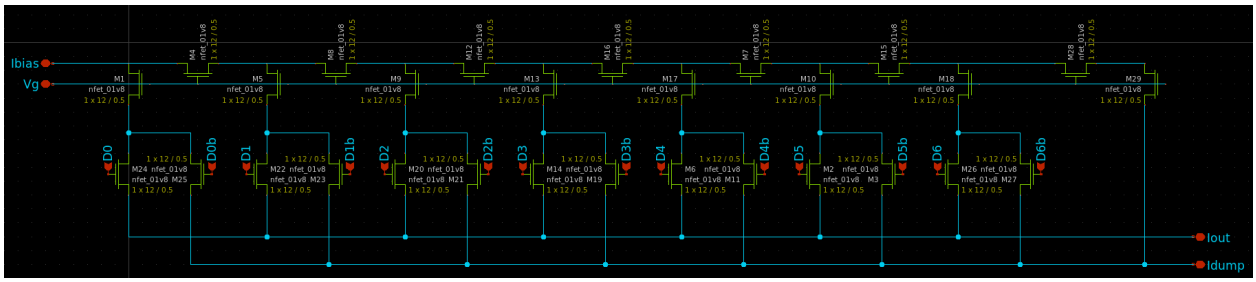

Figure 6. Schematic for 7-bit DAC.

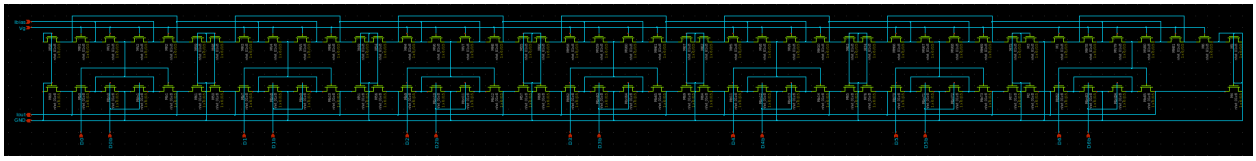

Figure 7. Layout-driven schematic for 7-bit DAC.

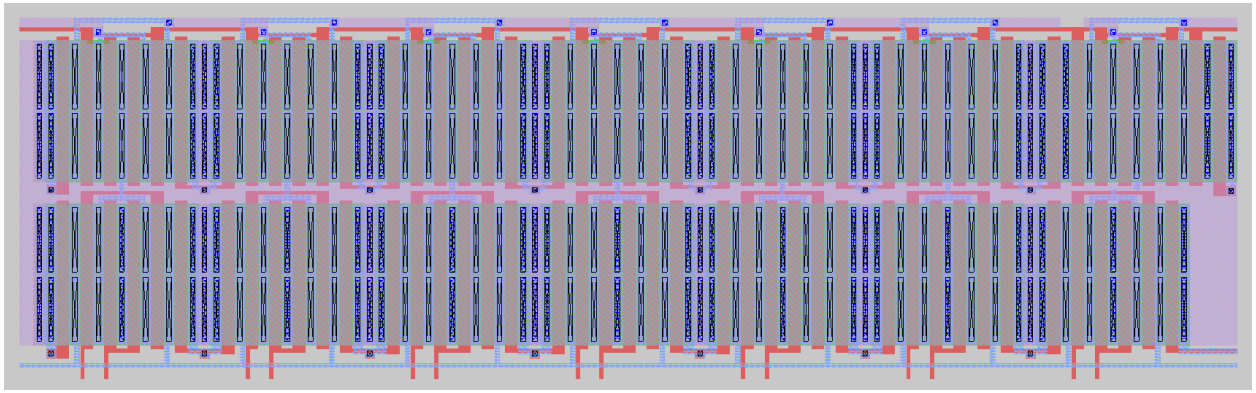

Figure 8. Magic layout for 7-bit DAC.

Netgen LVS for DAC Ladder Network.

```
Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell
sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are
equivalent.

Class ieee_DAC_ladder.spice (0):  Merged 49 parallel devices.
Class LDS_ieee_DAC.spice (1):  Merged 49 parallel devices.
Subcircuit summary:
Circuit 1: ieee_DAC_ladder.spice           |Circuit 2: LDS_ieee_DAC.spice

-------------------------------------------|-----------------------------------
---------
sky130_fd_pr__nfet_01v8 (86->37)           |sky130_fd_pr__nfet_01v8 (86->37)

Number of devices: 37                      |Number of devices: 37

Number of nets: 32                         |Number of nets: 32

-------------------------------------------------------------------------------
---------
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes ieee_DAC_ladder.spice and LDS_ieee_DAC.spice are equivalent.

Final result: Circuits match uniquely.
```

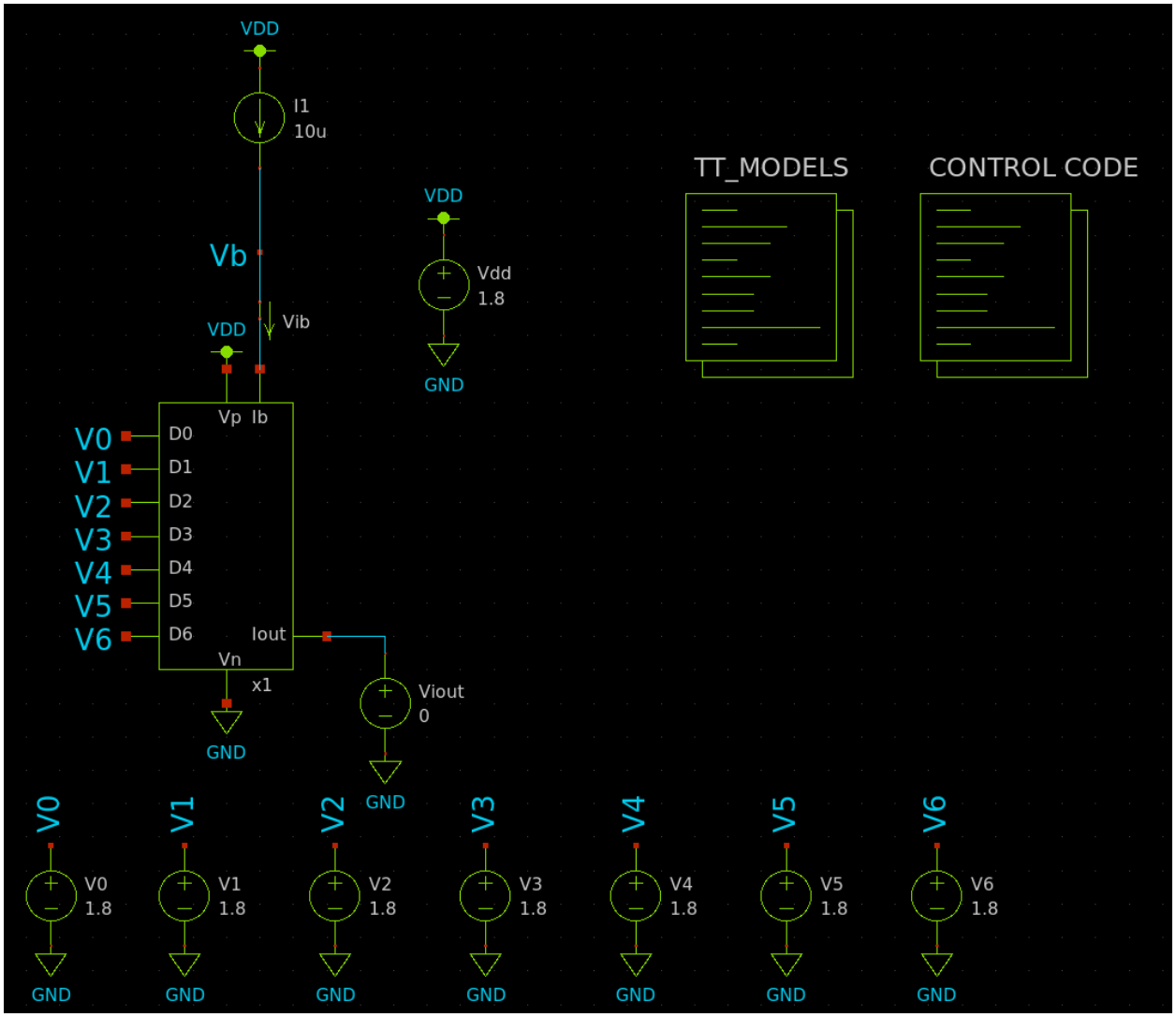

Figure 9. Simulated ideal DAC system.

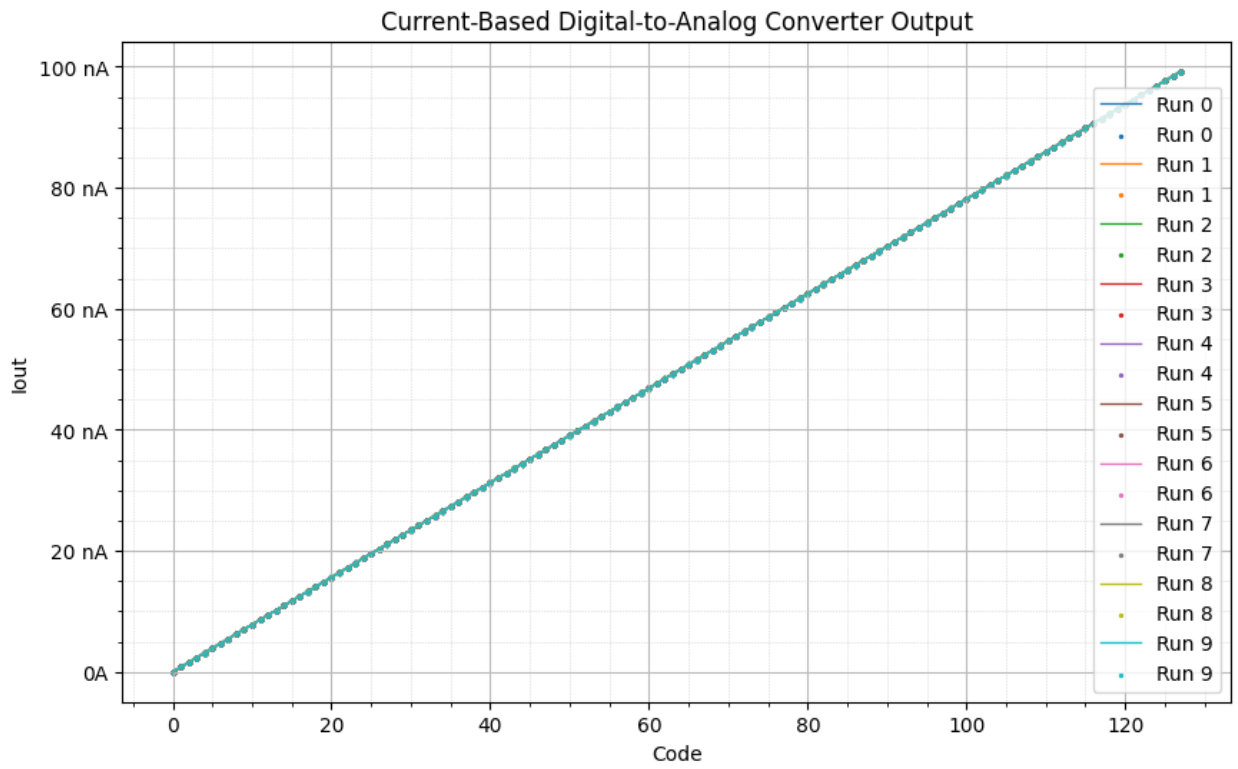

Figure 10. Current output from the DAC ladder from our ideal system.

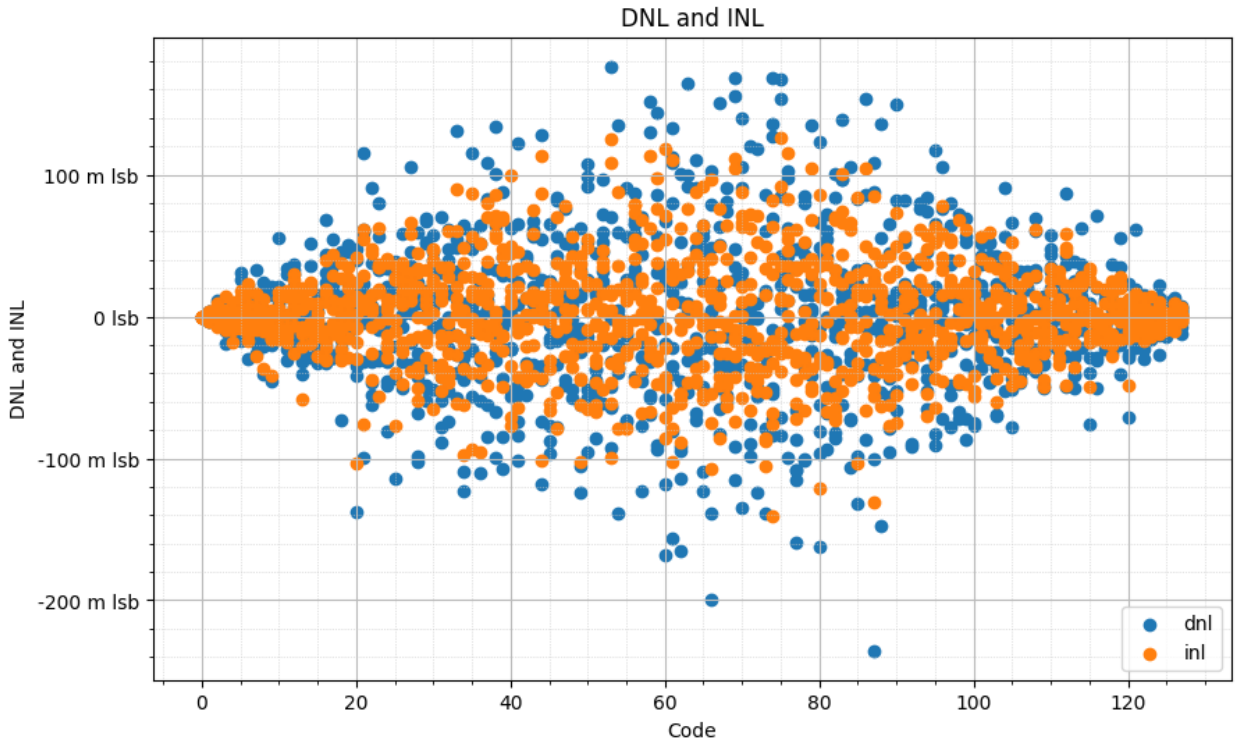

Figure 11. INL and DNL graph of the circuit we used with ideal current and voltage sources

Output stage for the IEEE DAC

Schematic for flipped voltage follower.

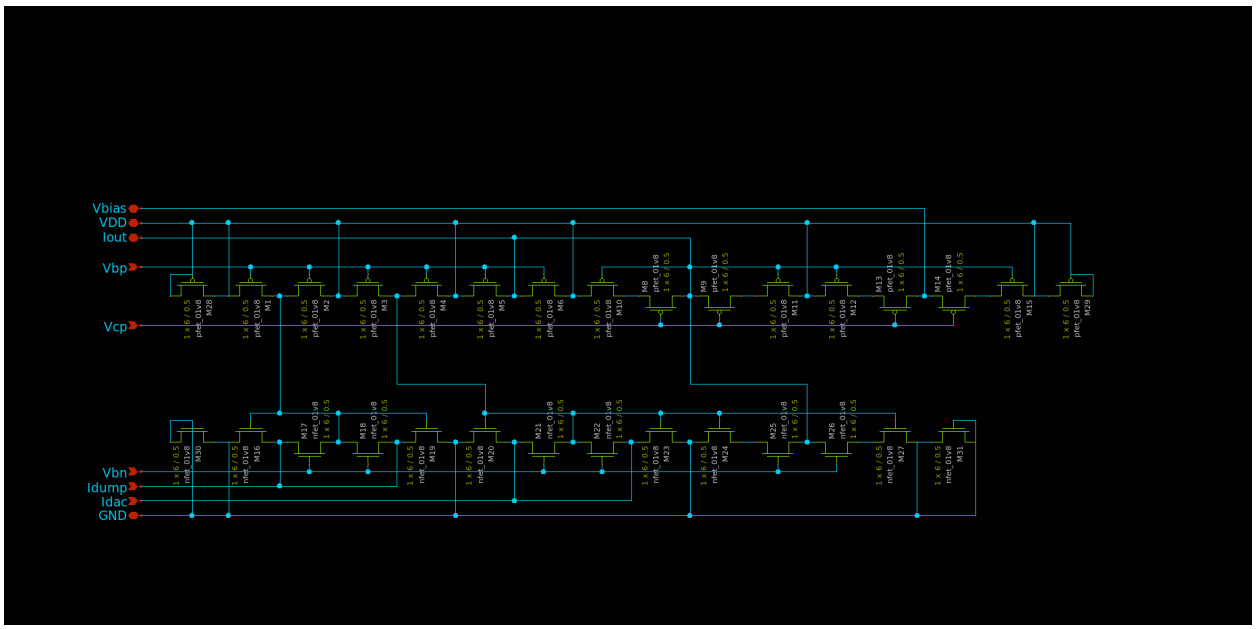

Figure 12. Output stage, which keeps Iout and Idump from the DAC ladder at the same potential and acts as a low voltage current mirror to combat any voltage changes on the output node.

Layout for the output stage

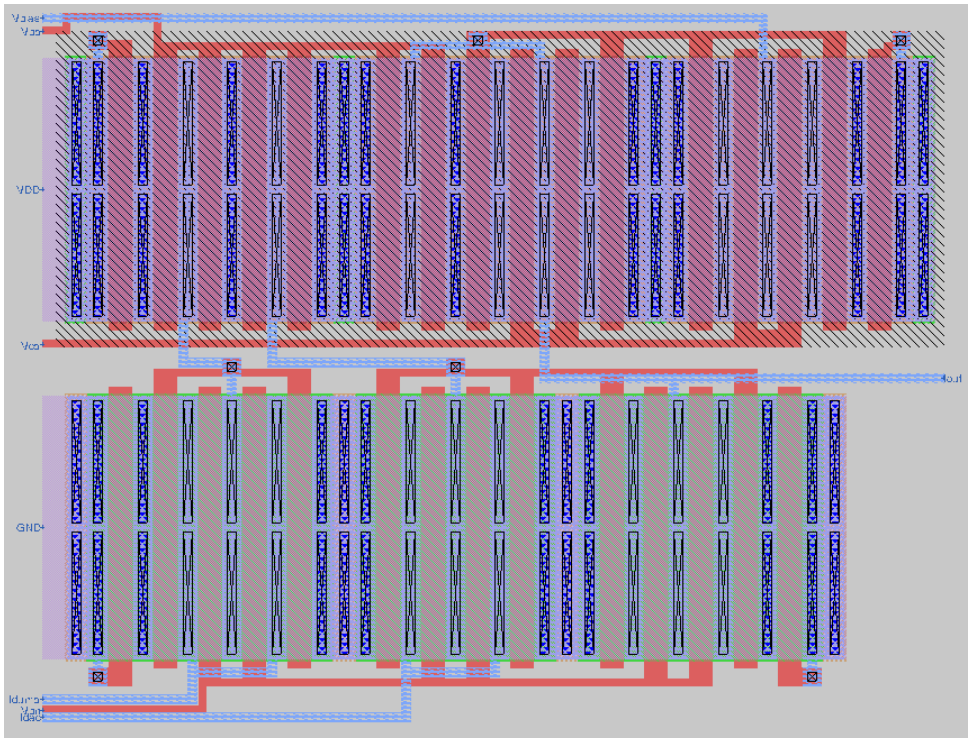

Figure 13. Magic layout of the output stage of the DAC ladder.

Netgen LVS for output stage flipped voltage follower.

```
1
2 Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes.
3 Equate elements:  no current cell.
4 Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.
5
6 Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes.
7 Equate elements:  no current cell.
8 Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.
9
10 Class Output_stage.spice (0):  Merged 9 parallel devices.
11 Class LDS_Output_stage.spice (1):  Merged 9 parallel devices.
12 Subcircuit summary:
13 Circuit 1: Output_stage.spice              |Circuit 2: LDS_Output_stage.spice
14 ------------------------------------------|------------------------------------------
15 sky130_fd_pr__nfet_01v8 (14->9)            |sky130_fd_pr__nfet_01v8 (14->9)
16 sky130_fd_pr__pfet_01v8 (16->12)           |sky130_fd_pr__pfet_01v8 (16->12)
17 Number of devices: 21                      |Number of devices: 21
18 Number of nets: 17                         |Number of nets: 17
19 -----------------------------------------------------------------------------------------
20 Resolving symmetries by property value.
21 Resolving symmetries by pin name.
22 Netlists match with 9 symmetries.
23 Cells have no pins;  pin matching not needed.
24 Device classes Output_stage.spice and LDS_Output_stage.spice are equivalent.
25
26 Final result: Circuits match uniquely.
27 .
```

LVS comp.out file of the flipped voltage follower

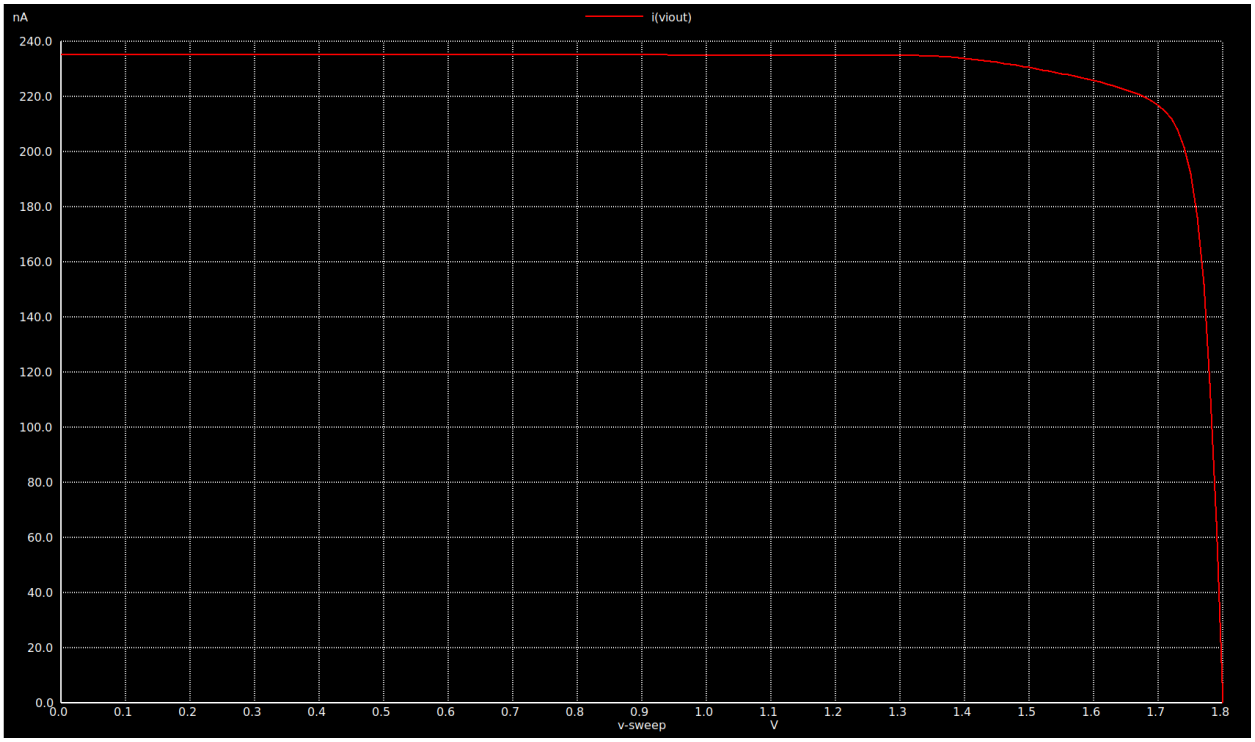

Figure 14. Results of output current vs. voltage sweep

This shows the output current is steady for more than 80% of the power supply range. We are looking for 1.44V on the output where the current is steady.

Low-voltage current mirror

Schematic for low-voltage current mirror.

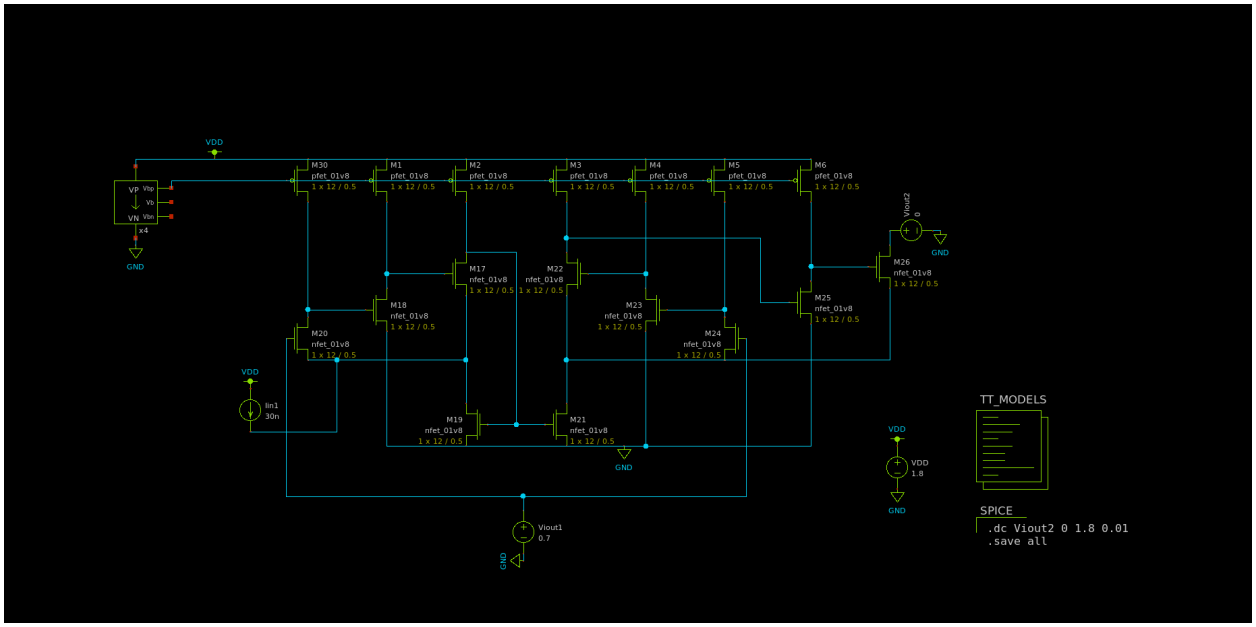

Figure 15. Simulation results of the current mirror

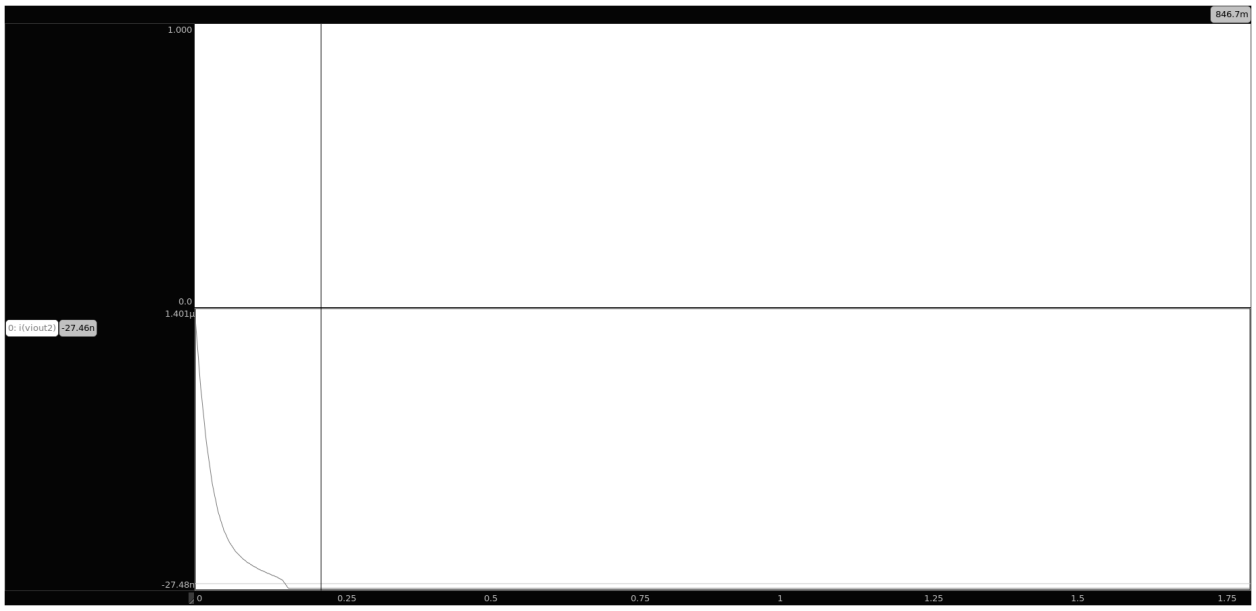

Figure 16. Graph of the current as we sweep the output nodes voltage.

```
lsb = 781.25 pA
max error (INL) = 98.13 pA = 0.126 lsb
max difference (DNL) = 176.34 mA = 0.176 lsb
```

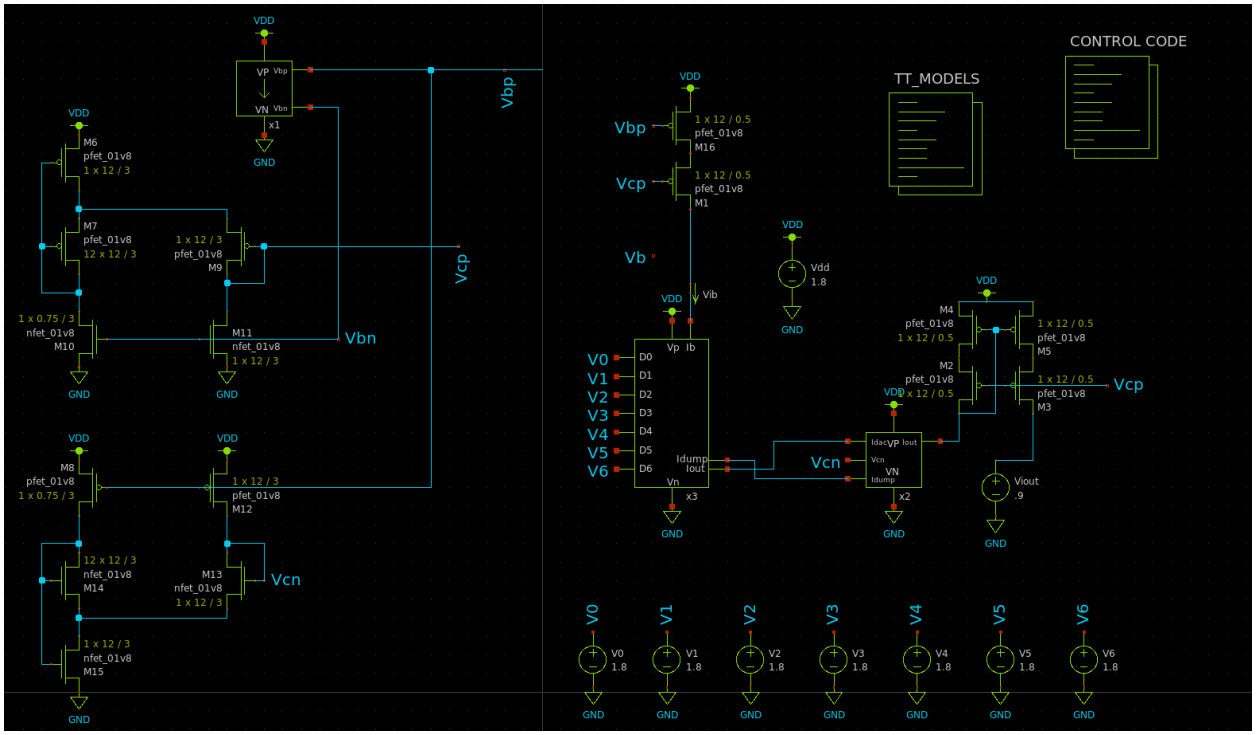

Figure 17. Schematic of the full rigged system.

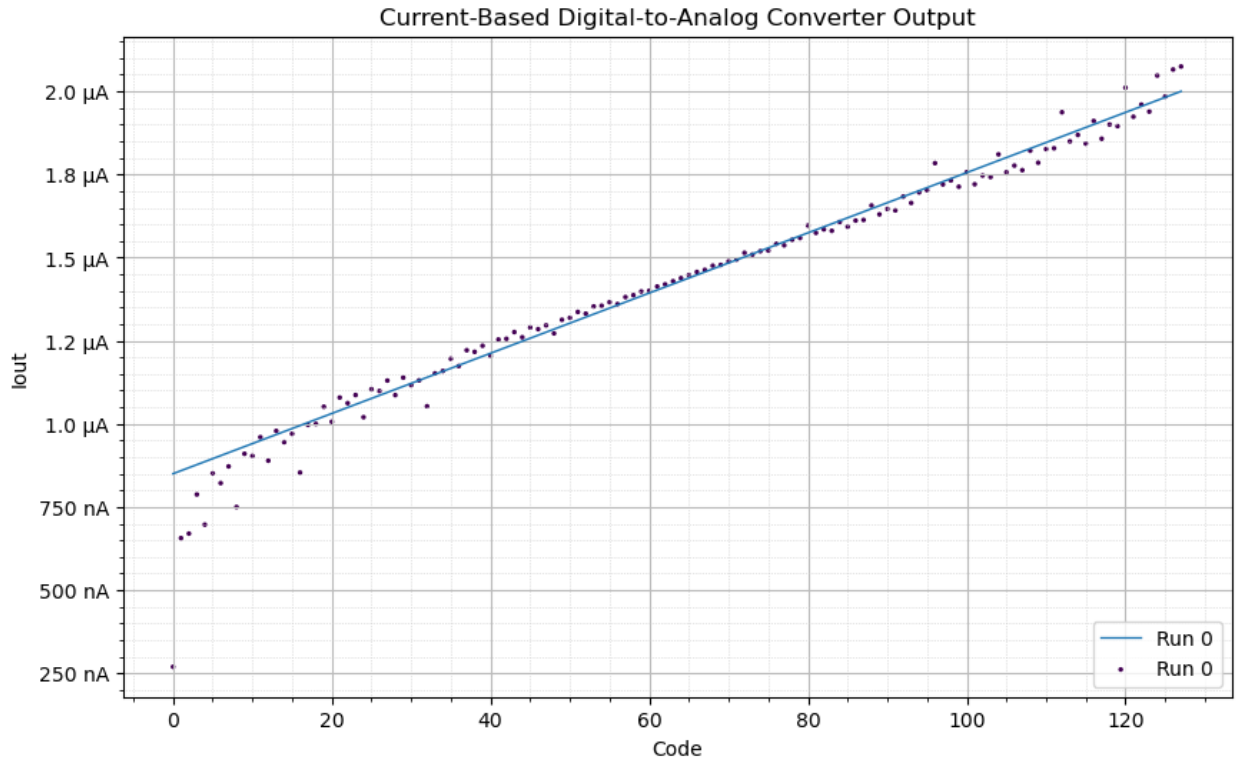

Figure 18. Current output of the DAC as we sweep through different bit inputs.

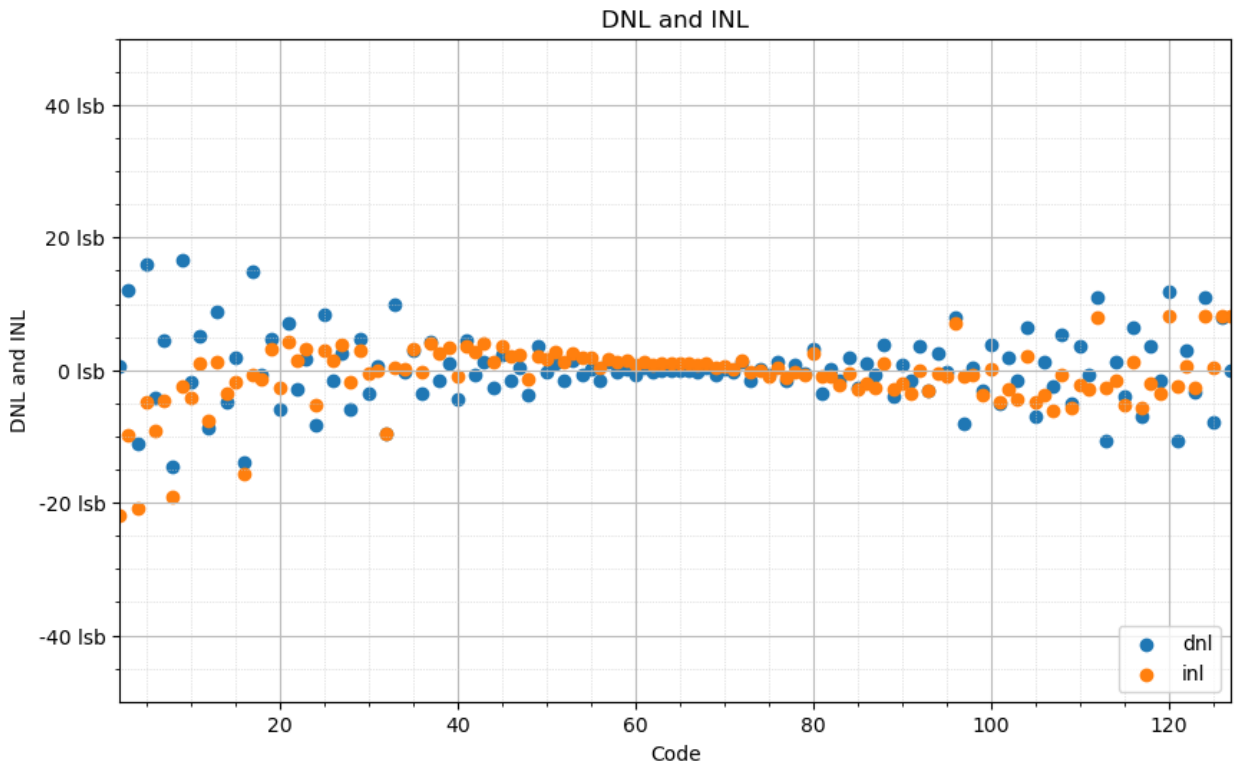

Figure 19. Graph of the DNL and INL Monte Carlo simulations for the full DAC schematic with no ideal current or voltage sources.

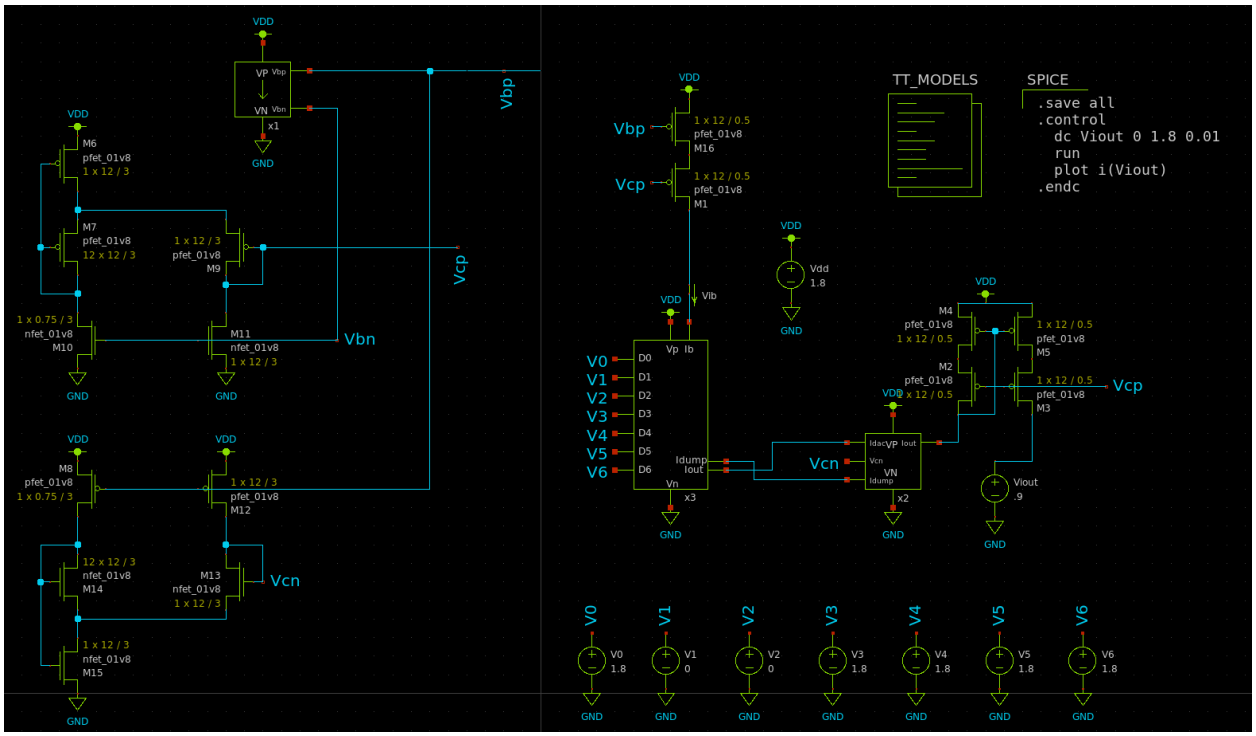

Figure 20. Test harness for output current sweep vs. code word.