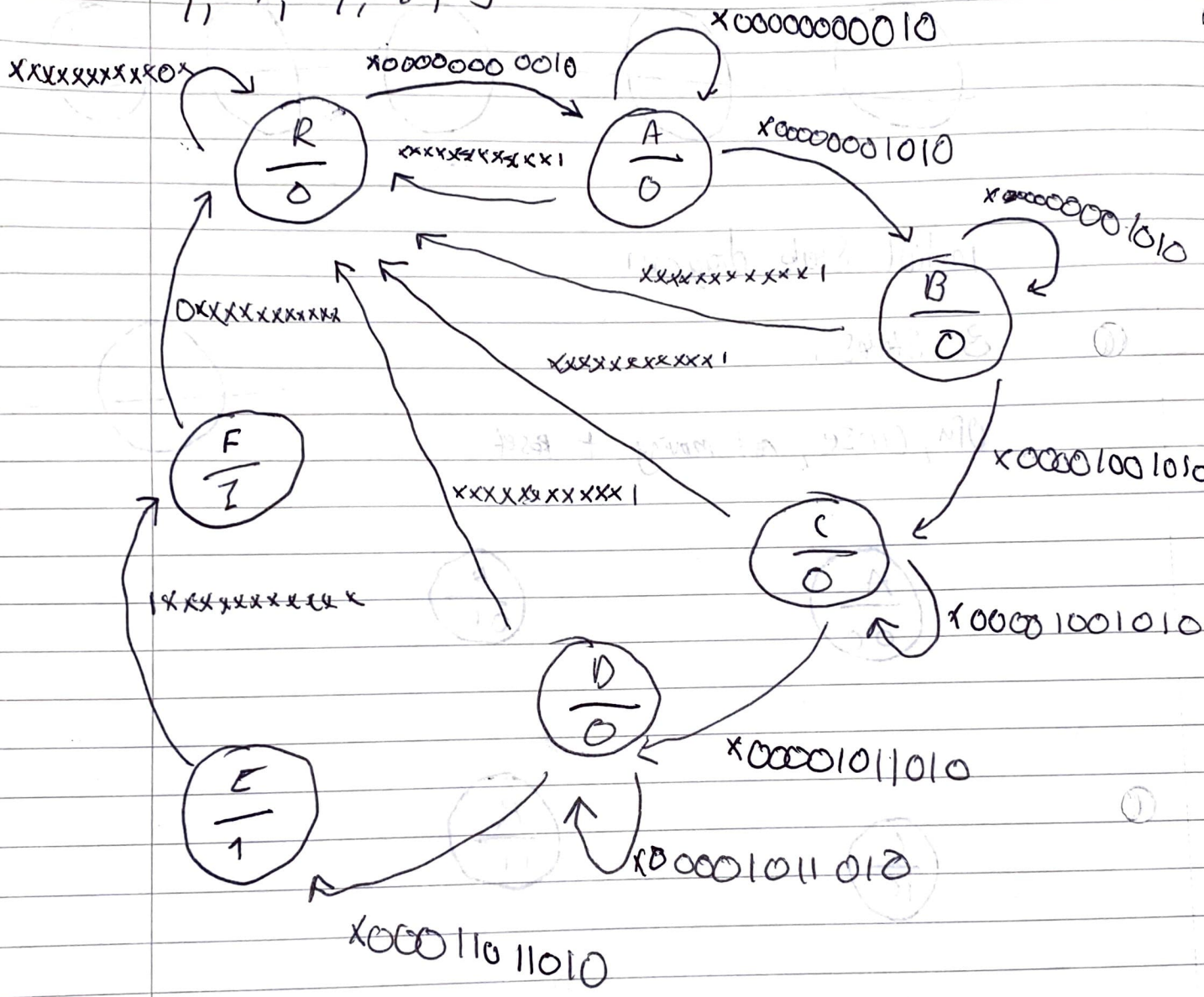
Lab 5 6th december

9, 7, 4, 6, 3



$QA = \overline{k0} \cdot \overline{k1} \cdot \overline{k2} \cdot \overline{k3} \cdot \overline{k4} \cdot \overline{k5} \cdot \overline{k6} \cdot \overline{k7} \cdot \overline{k8} \cdot k9 \cdot \overline{Reset}$

$QB = QA \cdot k0 \cdot \overline{k1} \cdot k2 \cdot \overline{k3} \cdot \overline{k4} \cdot \overline{k5} \cdot k6 \cdot k7 \cdot \overline{k8} \cdot k9 \cdot \overline{Reset}$

$QC = QA \cdot QB \cdot \overline{k0} \cdot \overline{k1} \cdot \overline{k2} \cdot \overline{k3} \cdot \overline{k4} \cdot \overline{k5} \cdot \overline{k6} \cdot \overline{k7} \cdot \overline{k8} \cdot k9 \cdot \overline{Reset}$

$QD = QA \cdot QB \cdot QC \cdot \overline{k0} \cdot \overline{k1} \cdot \overline{k2} \cdot \overline{k3} \cdot \overline{k4} \cdot \overline{k5} \cdot k6 \cdot k7 \cdot \overline{k8} \cdot k9 \cdot \overline{Reset}$

$QE = QA \cdot QB \cdot QC \cdot QD \cdot \overline{k0} \cdot \overline{k1} \cdot \overline{k2} \cdot k3 \cdot k4 \cdot \overline{k5} \cdot k6 \cdot k7 \cdot \overline{k8} \cdot k9 \cdot \overline{Reset}$

$Z = QE$

$\overline{Z} = QE \cdot Q1$

- implemented equations onto FPGA
- device works as intended with testing and simulating completed.