Lab 4 8/11/21

Using Same Sequence as Lab 3 implemat onto FPGA Machine:

Present				Next			
Q_d	Q_c	Q_b	Q_a	Q_d	Q_c	Q_b	Q_a
0	0	1	1	1	0	1	1
1	0	1	1	0	1	0	0
0	1	0	0	1	0	1	0
1	0	1	0	0	1	0	1
0	1	0	1	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	1	1	1	1
1	1	1	1	1	1	1	0
1	1	1	0	1	0	0	1
1	0	0	1	1	1	0	1
1	1	0	1	0	1	1	0
0	1	1	0	0	0	1	1

Using the final Simplified equations from Lab 3:

$$Q_d = Q_d \bar{Q}_c \bar{Q}_b Q_a + \bar{Q}_d \bar{Q}_b \bar{Q}_a + Q_d Q_c Q_b + \bar{Q}_d \bar{Q}_c Q_b$$

$$Q_c = Q_d Q_a + \bar{Q}_c Q_b \bar{Q}_a + Q_d Q_c \bar{Q}_b$$

$$Q_b = \bar{Q}_d \bar{Q}_c + \bar{Q}_d \bar{Q}_a + Q_d Q_c Q_a$$

$$Q_a = Q_b \bar{Q}_a + \bar{Q}_d Q_c + Q_a + \bar{Q}_d Q_b + Q_d \bar{Q}_c \bar{Q}_b$$

2nd Nov.

- encountered an error whilst generating bitstream
- added 'reg' to module definition fixed error
- implemented code onto FPGA device works as expected, when tested with all values