

Table 1: Instruction Translation

MIPS Instruction	Equivalent iDEA	Resolution
Arithmetic/ Logical		
add rd, rs, rt	add rd, ra, rb	none
addi rd, rs, #imm16	add rd, ra, #imm11	immediate value has to be limited to 11 bits or less
addiu rt, rs, #imm16	add rd, ra, #imm11	immediate value has to be limited to 11 bits or less
addu rd, rs, rt	add rd, ra, rb	none
sub rd, rs, rt	sub rd, ra, rb	none
sll rd, rt, #imm5	mul rd, ra, rb	none
mult rs, rt	mul rd, ra, rb	several iterations of multiply
div rs, rt	not supported	none
Program Control		
j #target	b #target	none
jal #target	b #target; mov rd, pc	none
jr rs	no equivalent inst	change in hardware needed
slt rd, rs, rt	mov rd, ra	none
beq rs, rt, #offset	cbeq ra, rb, #target	resolve the difference between #target and #offset
bne ra, rt, #offset	cbne ra, rb, #target	resolve the difference between #target and #offset
bltz ra, rt, #offset	cblt ra, rb, #target	resolve the difference between #target and #offset
bgez ra, rt, #offset	cbgez ra, rb, #target	resolve the difference between #target and #offset
Data Transfer		
lw rt, #offset (rs)	ldr rd, [ra, rb]	offset has to be stored in a register
sw rt, #offset (rs)	str rd, [ra, rb]	offset has to be stored in a register

Table 2: Composite iDEA Instructions

iDEA Instruction	Equivalent MIPS
cbeq ra, rb, #target	slt rd, rs, rt; beq rs, rt, #offset