Mob 13510032582 QQ 316224953 Mail fred@gold-luck.com

CellWise

CW2015

Low-Cost Fuel Gauge IC with Low-SOC Alert

Features

- System-Side or Pack-Side Fuel Gauging
- 3% Maximum Total SOC Measurement Error
- 14-bit Delta Sigma ADC for Temperature and Cell Voltage Measurement
- Precision Voltage Measurement
- No Offset Accumulation During Life Time
- No Full-to-Empty Battery Learning Cycles Necessary
- No Sense Resistor Required
- SOC and RRT available
- External Alarm/Interrupt for Low-Battery Warning Available
- Patented "FastCali" gas gauging algorithm
- Calibration After Quick Soft-Reset
- Very Low Active and Sleep Power Consumption
    - Normal mode 15uA
    - Sleep mode <1uA
- General I^2C interface
- Tiny, Lead(Pb)-Free, TDFN and CSP Package

Applications

- Smartphone
- Tablet PCs
- Handheld and Portable Applications

General Description

The CW2015 is an ultra-compact, low-cost, host-side/pack-side, sensing resistor free, fuel gauging system IC for Lithium-ion(Li+) based batteries in handheld and portable devices.

CW2015 tracks Li+ battery's operational condition and uses state-of-art algorithm to report the relative State-of-Charge (SOC) of very different battery chemistry systems (LiCoOx, polymer Li-ion, LiMnOx etc.).

CW2015 includes a 14-bit Sigma-Delta ADC, a precision voltage reference and build-in accurate temperature sensor. The IC allows the end-user to eliminate the expensive sensing resistor which occupies large board area. And the IC also sends out the alarm signal if the battery SOC level reaches pre-programmed threshold.

Quick start function offers the possibility to make an initial estimation of the battery's SOC, which also enables the IC to be located on system side or pack side, giving the flexibility to system maker on pack selection.

CW2015 uses a 2-wire I^2C compatible serial interface that operates in standard (100 kHz), fast (400 kHz).

Order Information

Name	Operation Temperature	Package	Package Mark
CW2015CSAD	-20℃ to 70℃	TDFN8	2015CSAD
CW2015CSAC	-20℃ to 70℃	CSP9	2015CSAC

Type number

CW2015 X X X X

— Package type   D: TDFN8; C: CSP9

— Parameter generation   A: Standard firmware and parameter, A version

— Embedded Battery profile type   S: CellWise Li-Polymer profile*

— Function and revision   C: C generation product

*This is only means the embedded profile for test is Li-polymer, not means the CW2015 is only used for Li-polymer battery. The CW2015 is compatible with Li-ion, Li-polymer and other type Li batteries
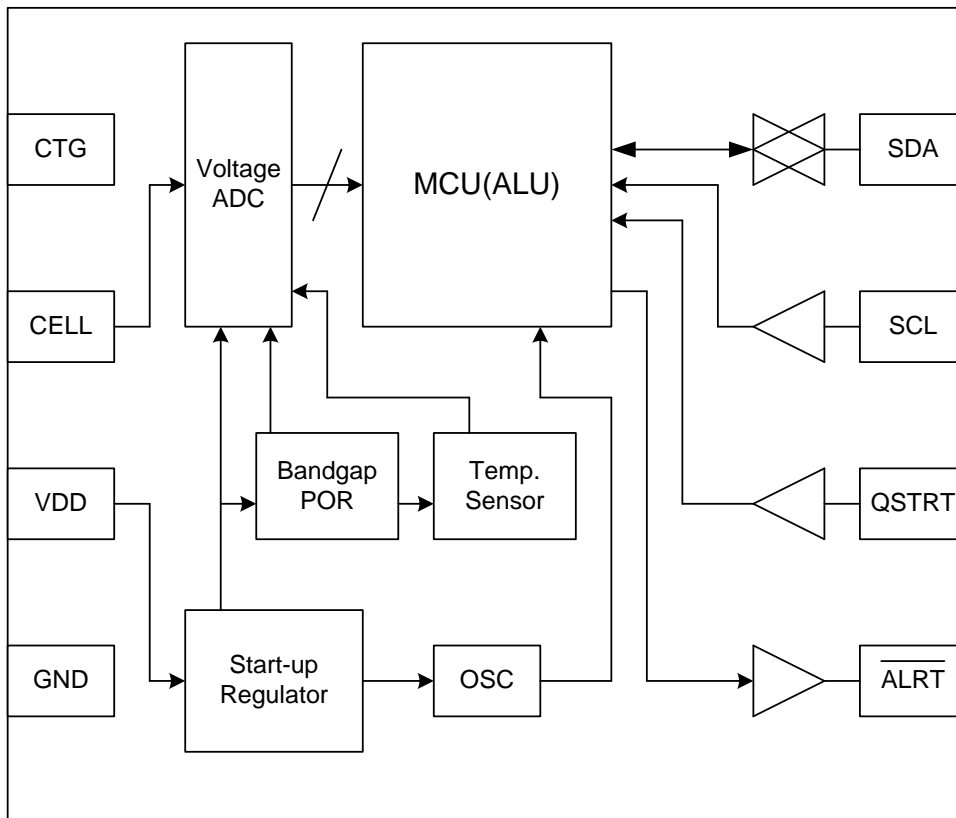
Function Block Diagram

Fig1. Block diagram

Absolute Maximum Ratings

Voltage on Supply VDD Pin Relative to GND	····································	-0.3 to +6V
Voltage on All Other Pins Relative to GND	····································	-0.3 to +6V
Operating Temperature Range	····································	-20℃ to 70℃
Junction Temperature	····································	150℃
Store Temperature Range	····································	-55℃ to 125℃

Caution:

Stresses beyond "Absolute Maximum Ratings" condition may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics Recommended DC Operating Conditions

(2.5≤VDD≤4.5, T_A= -20 to 70°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNITS
Supply Voltage	VDD		+2.5		+4.5	V
Data I/O Pins	SCL, SDA QSTRT, $\overline{ALRT}$		-0.3		+5.5	V
Analog I/O	CELL, CTG		-0.3		+5.5	V

Table1. Electrical Operating Parameters

DC Electrical Characteristics

(2.5≤VDD≤4.5, T_A= -20 to 70°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNITS
Active Current	I_{ACTIVE}	Normal Operation		15	20	µA
Sleep-Mode Current	I_{SLEEP}	VDD≤2.0V		0.5	1.0	µA
Time-Based Accuracy	t_{ERR}	VDD=3.7V	-3		+3	%
ADC input resistor	R_{ADIN}	VDD=Vcell=3.7V	10			MΩ
ADC resolution				14		bits
ADC conversion time	t_{ADCON}	VDD=Vcell=3.7V		10		ms
Battery Voltage update time	$t_{VUPDATE}$	VDD=Vcell=3.7V		250		ms
Input Logic-High SCL, SDA, QSTRT	V_{IH}	VDD=3.7V	1.4			V
Input Logic-Low SCL, SDA, QSTRT	V_{IL}	VDD=3.7V			0.6	V
Input Hysteresis	V_{IHYS}		0.2			V
Output Logic-Low: SDA, $\overline{ALRT}$	V_{OL}	I_{OL}=4mA		0.2	0.4	V
Pull down current: SDA, $\overline{ALRT}$				4		mA

Table2. DC Electrical Characteristics

Pin Arrangement and Description

TDFN Package Top view
2mm*3mm – 8pin
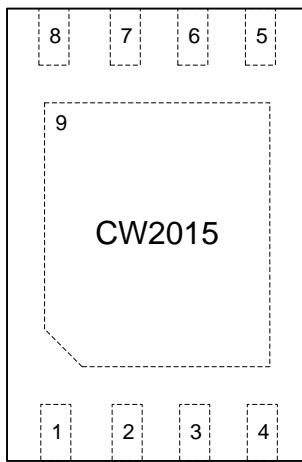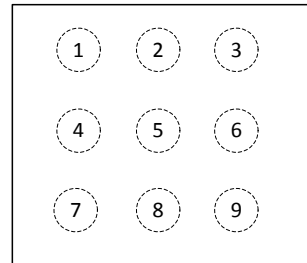
CSP Package Top view
1.48mm*1.41mm – 9pin

Fig2. Pin arrangement

TDFN Pin No.	CSP Pin No.	Pin Name	Description
1	9	CTG	Connect to ground
2	6	CELL	Battery voltage monitor I/O
3	3	VDD	System power supply
4	8	GND	General purpose ground connection
5	2	$\overline{\text{ALRT}}$	Low SOC alarm signal for MCU interrupt controller
6	7	QSTRT	Quick start, allows to do a quick SOC estimate
7	4	SCL	Serial clock input
8	1	SDA	Serial data Input/output
9		EP	Exposed pad, connect to GND or let floating

Table3. Pin description

Function

CW2015 is an ultra-compact, high precise gas gauging IC that embed new generational battery SOC estimate algorithm.

CW2015 provide the battery voltage, SOC and RRT estimate to user by measuring the cell voltage and temperature.

FastCali algorithm

From battery OCV (open circuits voltage), we deduce the SOC (state of charge) of this battery. Obtains OCV from two ways: idle battery voltage that has been relaxed at least half an hour; battery voltage adds the internal resistor voltage drop when charging or discharging.

Creative "equipment current track" technology precisely calculates the present voltage drop of the internal resistor, combine with the FastCali algorithm, CW2015 promptly infer the OCV value no matter the battery in charging, relaxing, or different current varying state.

First SOC Estimate after Power Up

CW2015 considers the battery as a free one that has been relaxed more than 0.5 hour when power up.

CW2015 treats the battery voltage measured by the 14bits ADC as an OCV voltage. According to this voltage, CW2015 deduces the first SOC value.

Error in the first SOC value will be calibrated during the normal use.

RRT

RRT offers the system remaining run time to user for reference. RRT is determined by the present SOC and battery discharging current, i.e. total system power dissipation. Battery remaining capacitor divide the current is the run time. Base on the "equipment current track" technology, CW2015 obtains the discharging current only through measure the battery voltage.

RRT updates all the time and vary according to the present current. Minimum scale of the RRT is 1min.

Quick Start

Quick start allows CW2015 to restart fuel gauge calculations in the same manner as an initial power-up by pull up the quick start pin or set the MODE register [0x0A].

This action used to reduce the large error in the SOC value.

Low SOC Alert

When battery SOC lower than or equal to the setting threshold [0x06~0x07], low SOC alert triggered. CW2015 set the ALRT flag to 1, and pull down the ALRT pin to inform the external host. The ALRT pin remains logic-low until the host reset the ALRT flag to

logic 0 by I²C bus.

Cleared ALRT don't generate another alert signal while the SOC remains below the alert threshold. The SOC must rise above and then fall below or equal to the alert threshold value before another interrupt is generated.

Sleep Mode

All the function will be halt in the sleep mode, power dissipation of CW2015 reduced to the lowest level.

Set the MODE register bit Sleep to 11 to enter into the sleep mode. All the data update stop, when recover from sleep mode, SOC algorithm begins from the stop point. When the battery voltage lower than 2.5V, CW2015 enter into the sleep mode automatically.

POR

Power on reset. Set the MODE register bit POR to 1111 to reset the device, all the registers and date except flash will reset to zero.

Register Map

Below table shows the I²C register map for the CW2015.

Register Name	Address	Description	Read/Write*	Default Value
VERSION	0x00	Returns IC version, software version	R	0x6F
VCELL	0x02-0x03	Report 14-bit A/D measurement of battery voltage	R	0x00
SOC	0x04-0x05	Report 16-bit SOC result calculated	R	0x00
RRT_ALRT	0x06-0x07	13 bits remaining run time and low SOC alert bit	W/R	0x00
CONFIG	0x08	Configure register, alert threshold set	W/R	0x18
MODE	0x0A	Special command for IC state	W/R	0xC0

Table4. Register map

*Read/Write means they can be read from application processor outside our IC

VCELL Register

The VCELL register is a read-only register that updates continuously the battery terminal voltage. Battery voltage is measured at the CELL pin with GND pin as a ground reference. A 14bit sigma-delta A/D converter is used and the voltage resolution is 305uV for CW2015. This A/D converter updates the cell voltage for a period of <10ms after IC POR and then four times a second afterwards.
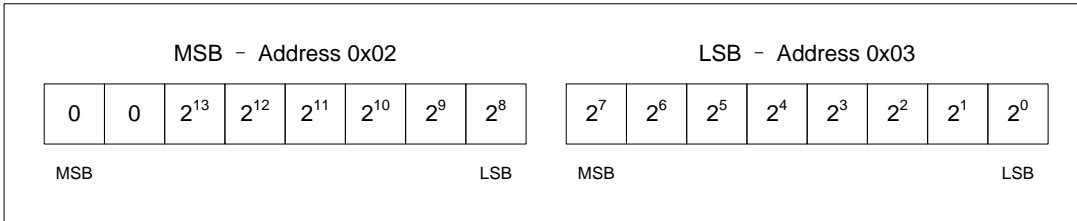
	MSB – Address 0x02								LSB – Address 0x03							
0	0	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}		2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSB							LSB		MSB							LSB

Fig 3.VCELL Register Format

SOC Register

The SOC register is also a read-only register that indicates the State-of-Charge of the battery cell. SOC value is a relative concept which display as a percentage of the cell's total capacity. This register intrinsically adjusts itself to the change of battery cell's parameter due to aging, poor cell parameter distribution control or rapid change in total capacity.

In this register, the high 8bit part contains the SOC information in % units which can be directly used by end user if this accuracy is already good enough for application. The low 8bit part provides more accurate part of the SOC information until 1/256%.
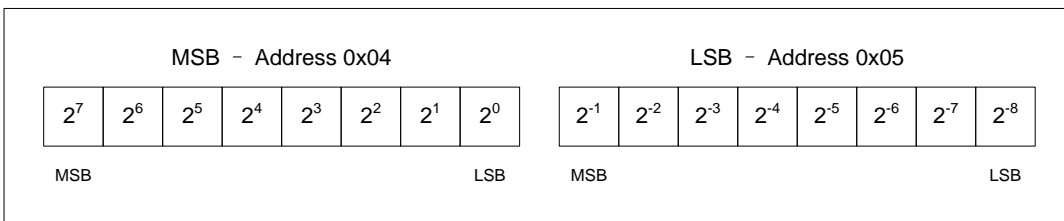
MSB – Address 0x04									LSB – Address 0x05							
2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}		2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
MSB							LSB		MSB							LSB

Fig 4.SOC Register Format

RRT_ALRT Register

ALRT, Flag register bit. This bit is set by the IC when the SOC register value falls below or equal to the alert threshold setting and an interrupt is generated. This bit can only be cleared by the host through I^{2}C bus . The power-up default value for ALRT is logic 0.

The read-only register RRT indictors the remaining run time of the battery according to the present the SOC and discharging current. RRT is not a linear variation value, and update per 1s.

Register RRT provide 13bits to record the remaining time, 1 LSB represents 1 minute.
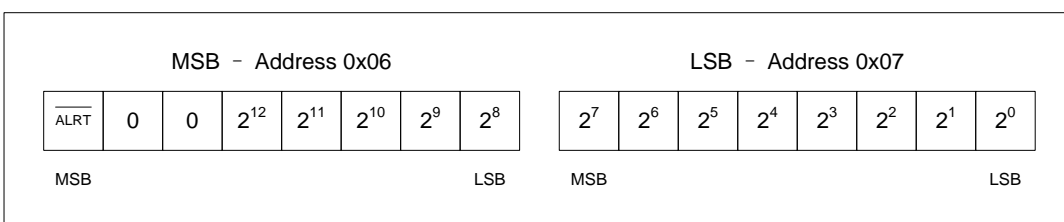
MSB – Address 0x06									LSB – Address 0x07							
$\overline{ALRT}$	0	0	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}		2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSB							LSB		MSB							LSB

Fig 5.RRT_ALRT Register Format

CONFIG Register

ATHD is low SOC alert threshold setting register. The alert threshold is a 5-bit value that sets the state of charge level where an interrupt is generated on the ALRT pin. The alert threshold has an LSB weight of 1% and can be programmed from 0% up to 31%. The power-up default value for ATHD is 3%.

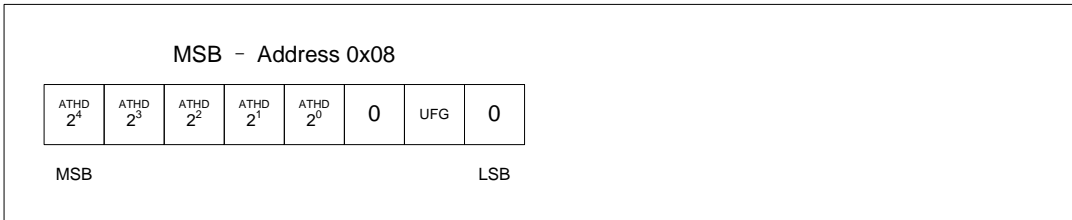UFG is a flag bit used to indicator the battery information update state.

MSB – Address 0x08

ATHD 2^4	ATHD 2^3	ATHD 2^2	ATHD 2^1	ATHD 2^0	0	UFG	0

MSB   LSB

Fig 6.CONFIG Register Format

MODE Register

Mode register is used for Master to control the IC.

Sleep mode, two bits to control. Default value 11, write 11 to force the CW2015 enter the sleep mode; write 00 to wake up.

QSTRT, quick start, two bits to control. Default value 00, write 11 to start.

Quick-start allows the IC to restart fuel-gauge calculations in the same manner as initial power-up of the IC. For example, if an application's power-up sequence is exceedingly noisy such that excess error is introduced into the IC's "first guess" of SOC, the host can issue a quick-start to reduce the error. A quick-start is also initiated by a rising edge on the QSTRT pin.

POR, power of reset, four bits to control. Default value 0000, write 1111 to completely restart the IC as if power removed.

MSB – Address 0x0A

Sleep 2^1	Sleep 2^0	QSTRT 2^1	QSTRT 2^0	POR 2^3	POR 2^2	POR 2^1	POR 2^0

MSB   LSB
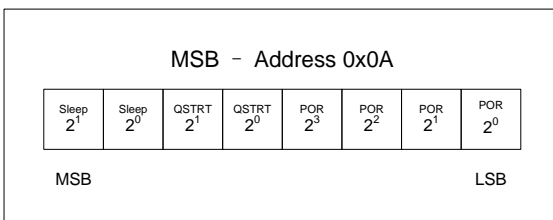
Fig7. MODE Register Format

I^{2}C Interface

The CW2015 communicates through an I^{2}C interface. I^{2}C is a two-wire open-drain interface supporting multiple devices and masters on a single bus. Some I^{2}C devices can act as masters or slaves, but the CW2015 can only act as a slave device that only pull the bus wires LOW and never drive the bus HIGH. Data on the I^{2}C-bus can be transferred at rates of up to 100kbit/s in standard mode or fast (400 kHz) or fast mode plus (1 MHz) modes.

Device Address

I^{2}C device address is consist of 7bits slave address and 1 read/write control bit.

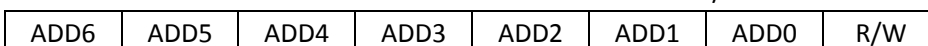| ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R/W

Fig8. I^{2}C address structure

Address of CW2015 is fixed on 0b1100010. Combine with de R/W bit:

Read command of CW2015 is 0xC5;

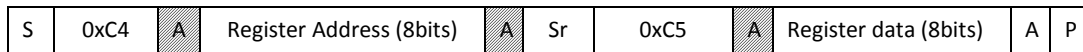Write command of CW2015 is 0xC4.

START and STOP Conditions

When the bus is idle, both SCL and SDA must be HIGH. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from HIGH to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Read and Write Command

Figure 11 shows an overview of the read and write command on the I^{2}C bus.

Read

| S | 0xC4 | A | Register Address (8bits) | A | Sr | 0xC5 | A | Register data (8bits) | A | P |

Write

| S | 0xC4 | A | Register Address (8bits) | A | Write data (8bits) | A | P |

☐ From Master to Slave   S   Start

▨ From Slave Master   A   Acknowlage
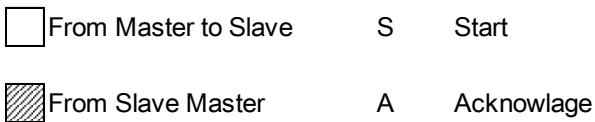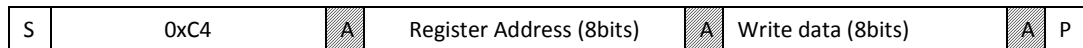
Fig9. Read and write command

Typical Operation Parameter

CW2015 VOLTAGE ADC ERROR vs. TEMPERATURE
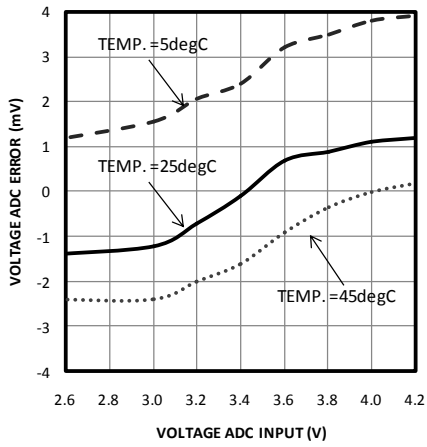
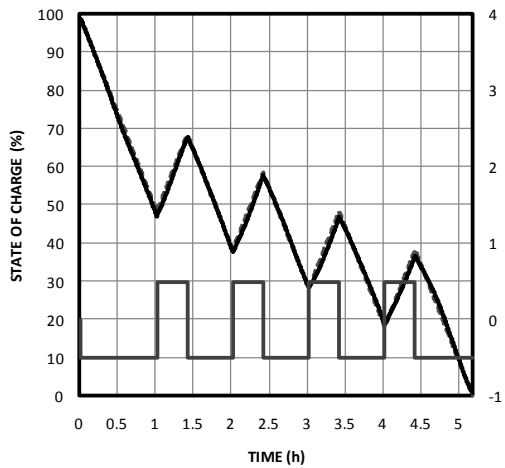**QUIESCENT CURRENT vs. SUPPLY VOLTAGE**
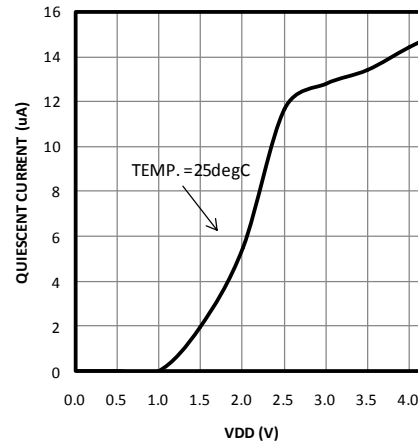
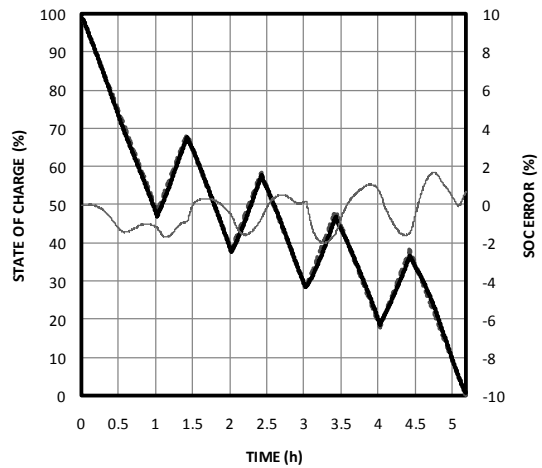**SIMPLE C/5 RATE DISCHARGE SOC ACCURACY**
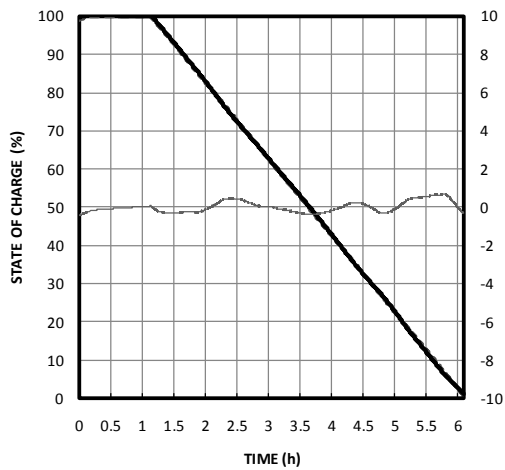
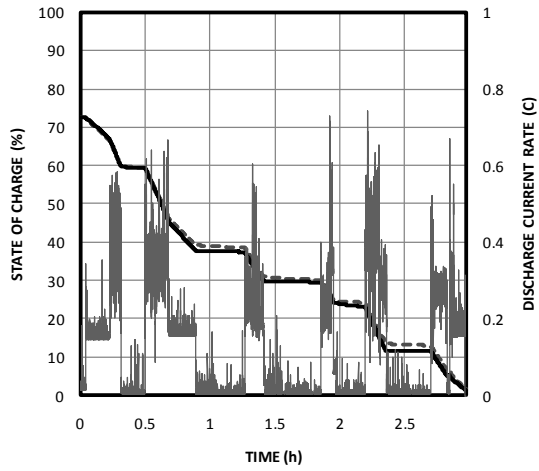**SIMPLE C/2 RATE DISCHARGE SOC ACCURACY**
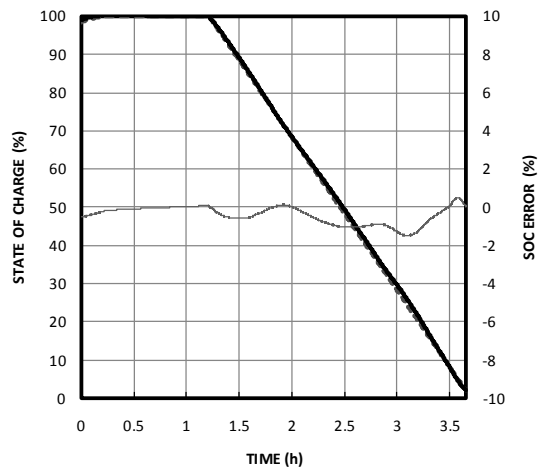
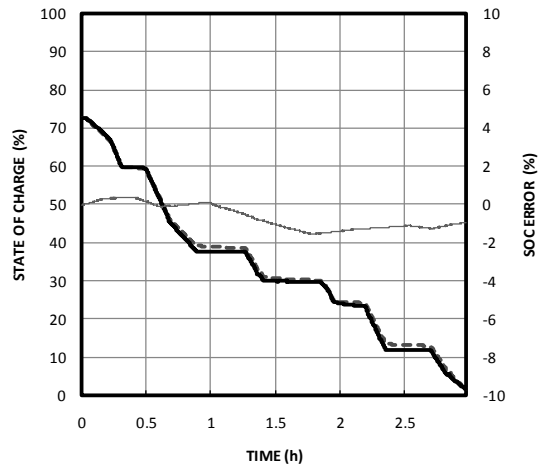**C/2 RATE ZIGZAG PATTERN SOC ACCURACY 1**
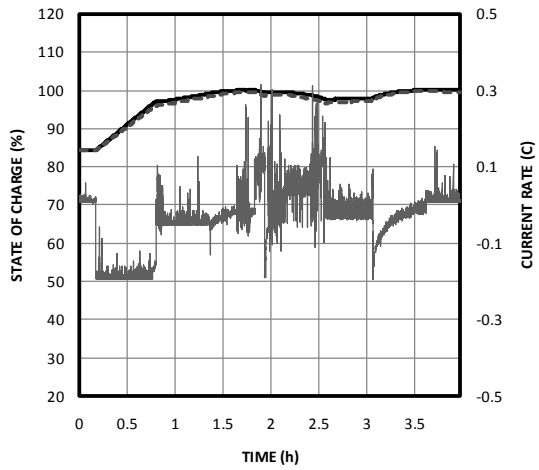

C/2 RATE ZIGZAG PATTERN SOC ACCURACY 2

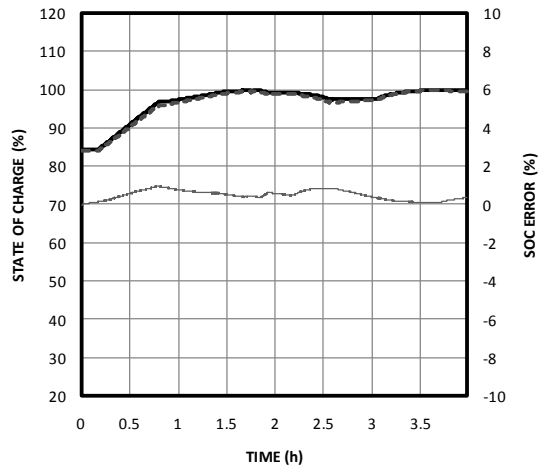**REAL APPLICATION/DISCHARGE SOC ACCURACY 1**

REAL APPLICATION/DISCHARGE SOC ACCURACY 2

REAL APPLICATION UNDER CV MODE SOC ACCURACY 1

REAL APPLICATION UNDER CV MODE SOC ACCURACY 2
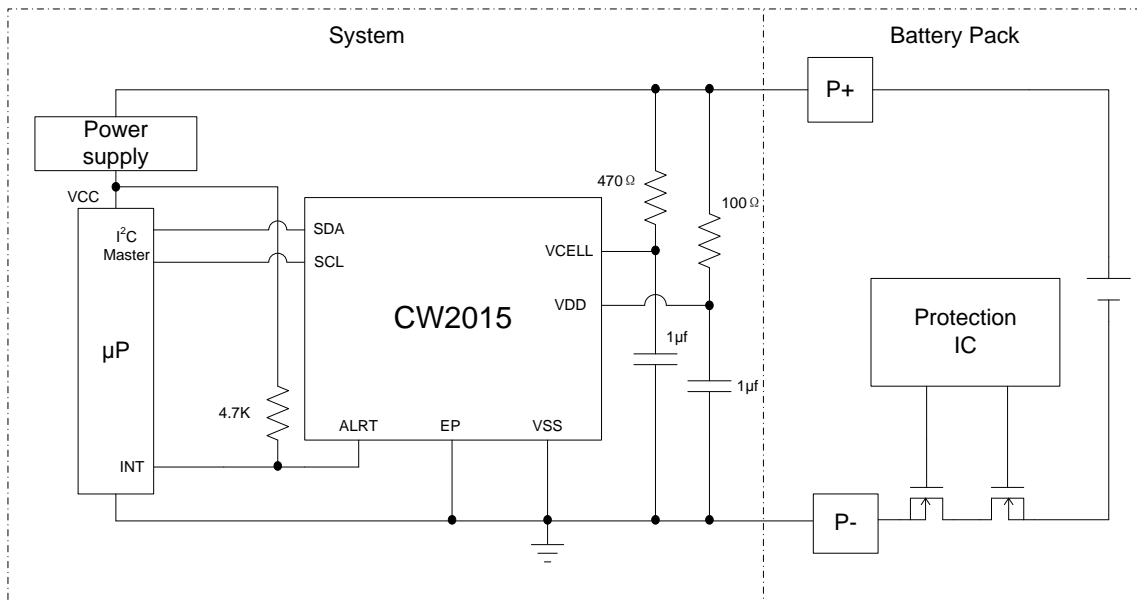
Application Diagram

Fig10. Application diagram (system side)

Fig10 is a typical application diagram of CW2015 used in system side, recommended value of the external components is mark on the figure.
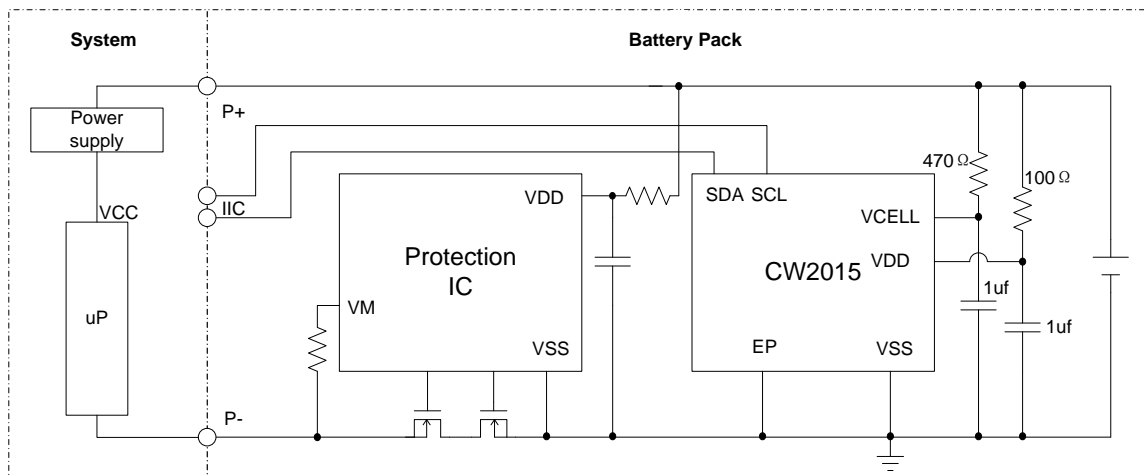

Fig11. Application diagram (pack side)

Fig11 is a typical application diagram of CW2015 used in pack side, recommended value of the external components is mark on the figure.

CW2015 can be also used in the 2 batteries connected in series, or several cells connected in parallel.
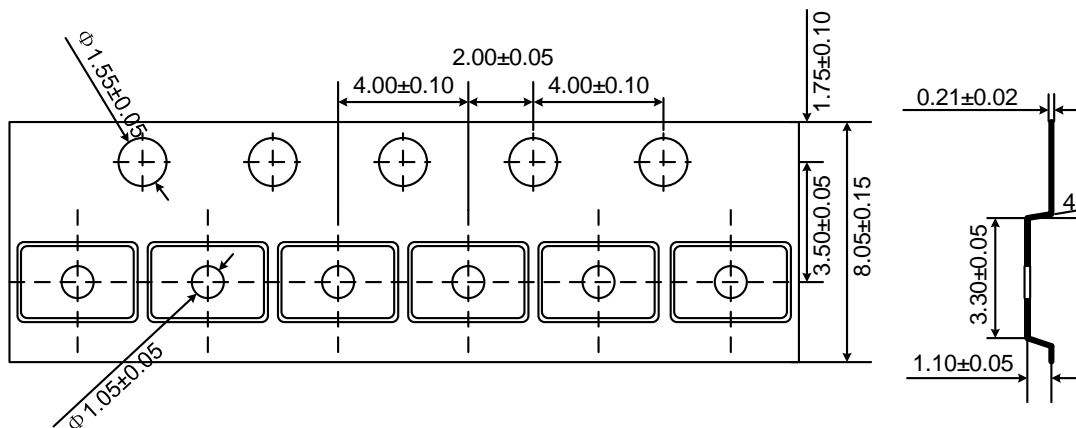
More detailed application information please refers to the application notes or connects CellWise for more support.

CellWise

Tape and Reel Information
TDFN Package Reel Information
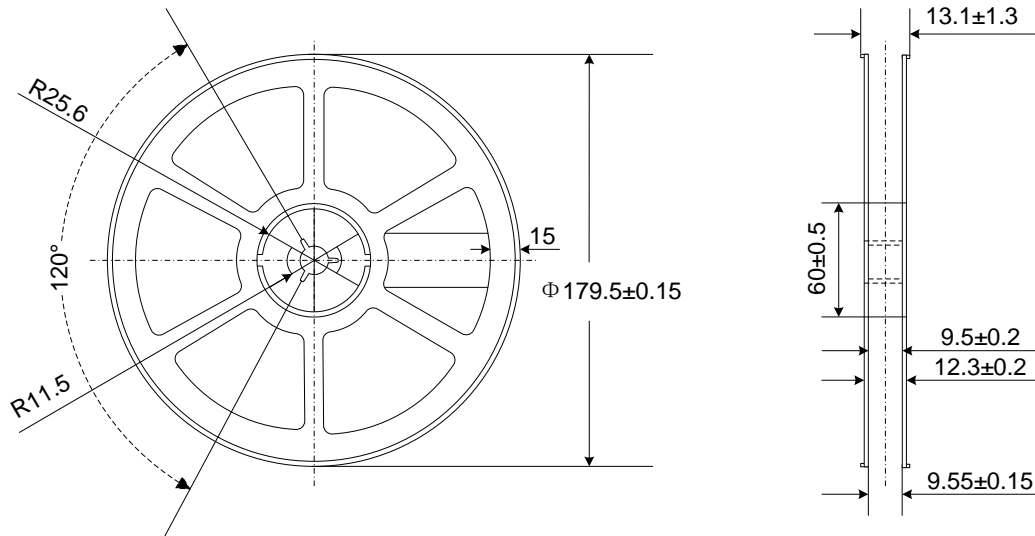
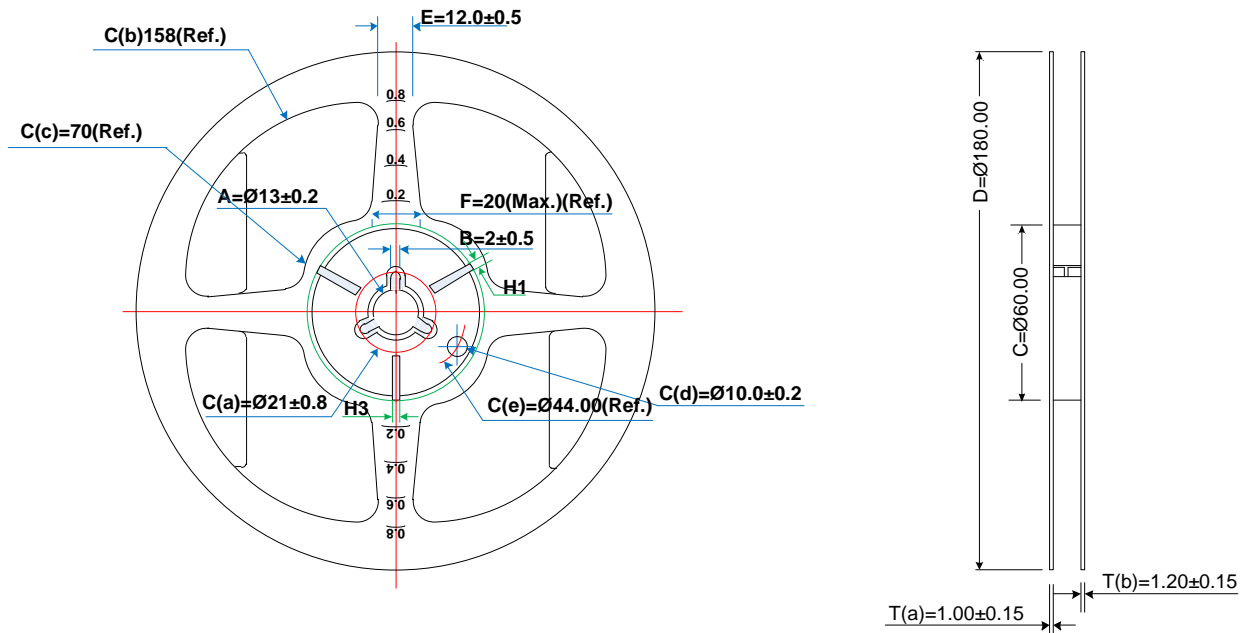Color: Blue
All DIM in mm

TDFN Package Tape Information

Carrier Tape Color: Black
Cover Tape Width: 5.30±0.10
Cover Tape Color: Transparent
All DIM in mm
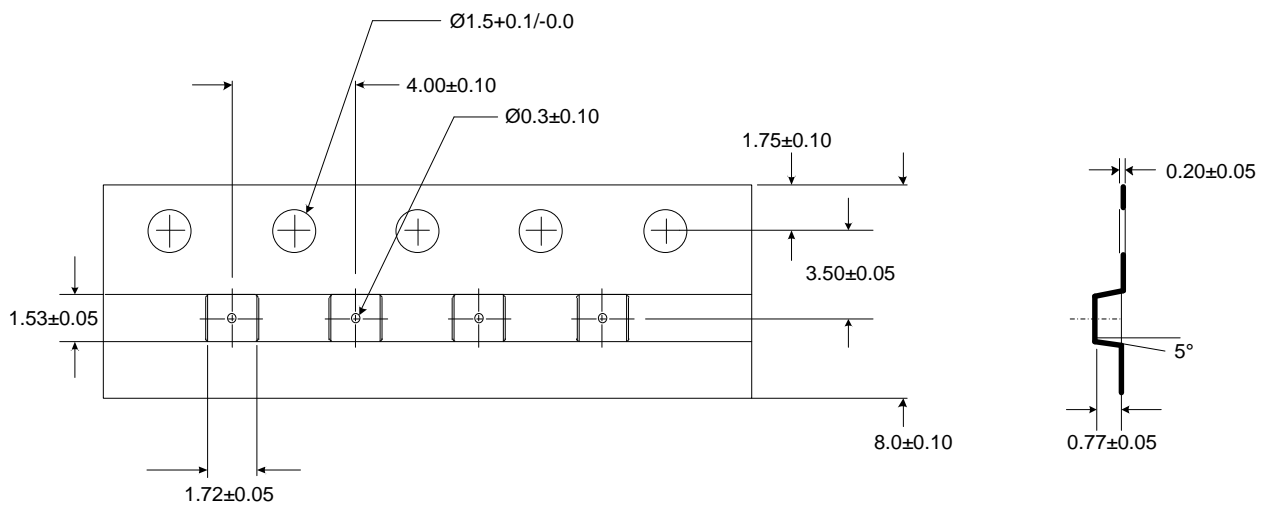
All the package materials are Pb free and Halogen free.

Tape and Reel Information
CSP Package Reel Information

All DIM in mm

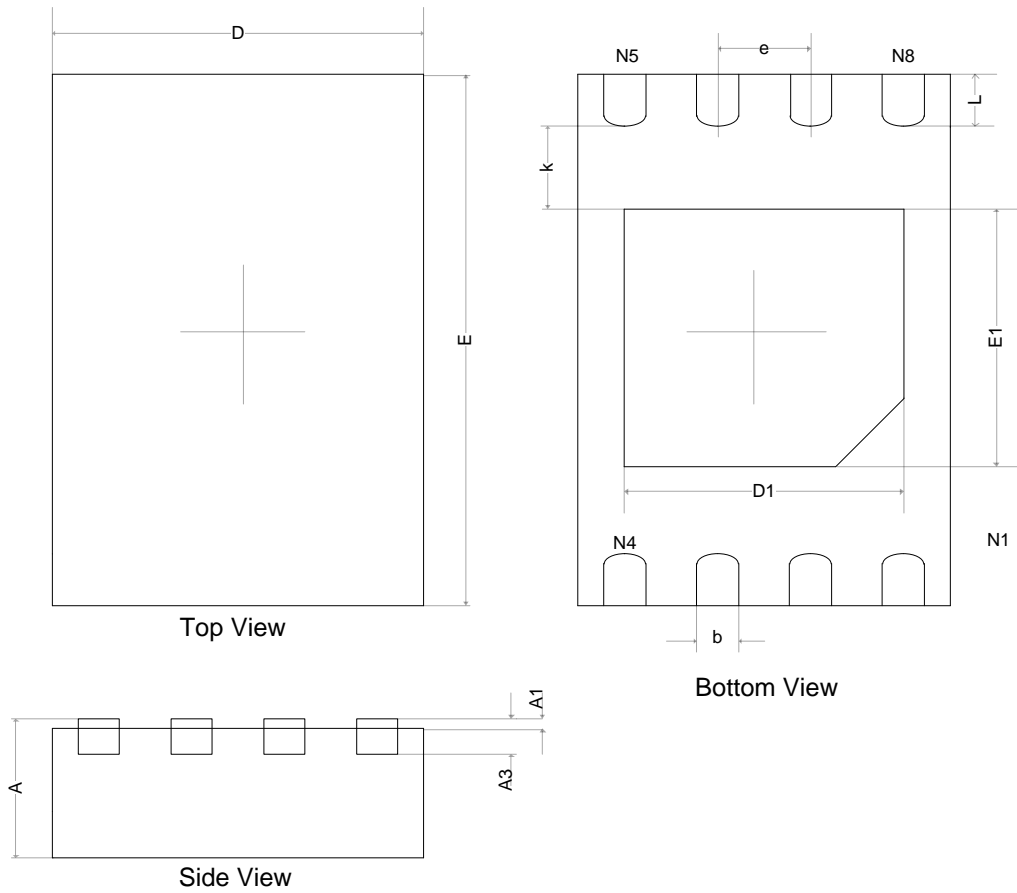## CSP Package Tape Information

All DIM in mm

All the package materials are Pb free and Halogen free.

Package Information

TDFN2 x 3-8L(P0.50T0.75/0.85) PACKAGE OUTLINE DIMENSIONS

Top View

Bottom View

Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
K	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

CSP9 PACKAGE OUTLINE DIMENSIONS

Top View(BGA side)

Ball center=(25,10)

Package center=(0,0)
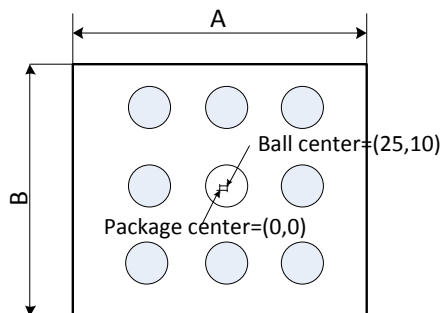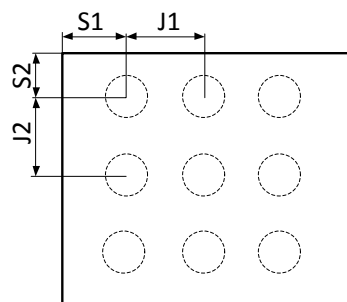
Bottom View(Back cover)

Cross Section

Unit: um
Package Size:1450*1380
Min ball pitch:400
Ball diameter:200

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	1.4500	1.4250	1.4750	0.0571	0.0561	0.0581
Package Body Dimension Y	B	1.3800	1.3550	1.4050	0.0543	0.0533	0.0553
Package Height	C	0.6000	0.5550	0.6450	0.0236	0.0219	0.0254
Silicon +Back cover Thickness	C2	0.4850	0.4700	0.5000	0.0191	0.0185	0.0197
Ball Height	C1	0.1000	0.0700	0.1300	0.0039	0.0028	0.0051
Ball Diameter	D1	0.2000	0.1700	0.2300	0.0079	0.0067	0.0091
Total Ball Count	N	9(1NC)					
Ball Count X axis	N1	3.0000					
Ball Count Y axis	N2	3.0000					
Pins Pitch X axis	J1	0.4000			0.0157		
Pins Pitch Y axis	J2	0.4000			0.0157		
BGA ball center to package center offset in X-direction	X	0.0250	0.0000	0.0500	0.0010	0.0000	0.0020
BGA ball center to package center offset in Y-direction	Y	0.0010	-0.0240	0.0260	0.0000	-0.0009	0.0010
BGA ball center to chip center offset in X-direction	X1	0.0250	-0.0140	0.0140	0.0010	-0.0006	0.0006
BGA ball center to chip center offset in Y-direction	Y1	0.0010	-0.0140	0.0140	0.0000	-0.0006	0.0006
Edge to Ball Center Distance along X	S1	0.3000	0.2700	0.3300	0.0118	0.0106	0.0130
Edge to Ball Center Distance along Y	S2	0.2800	0.2500	0.3100	0.0110	0.0098	0.0122

CW2015 Revision Record

Date	Version	Changed Item	Written by	Approved by
2012-06-13	0.4	1. Add test result curve 2. Remove CRC and Factory register definition 3. Update the register type to Visio picture	Jun	Bob
2012-06-15	0.5	1. Correct IC number on P7	Jun	Bob
2012-08-09	0.6	1. Update register map	Jun	Bob
2012-08-19	0.7	1. Update package picture 2. Add test curve	Jun	Bob
2012-09-02	0.8	1. Update test result curve	Jun	Bob
2012-09-04	0.9	1. Update test waveform 2. Update part number 3. Update block diagram	Jun	Bob
2012-11-02	1.0	1. Add type number explanation 2. Release formal version	Jun	Bob
2012-11-06	1.1	1. Delete CNAD type number 2. Explain the connection of EP pad 3. Update application circuits	Jun	Bob
2013-01-30	1.2	1. Re-explain the C/S/A/D 2. Change the operation temperature	Jun	Bob
2013-02-01	1.3	1. Add ADC electrical parameter 2. Delete auto power save function and related PD 3. Delete absolute ADC conversion accuracy	Jun	Bob
2013-04-26	1.4	1. Correct the description of Alert flag clear action 2. Change I2C character to I^2C 3. Rename the application circuits to application diagram 4. Add the application diagram for pack side 5. Add the description of application for 2-cells in series or several cells in parallel	Jun	Bob
2013-05-02	1.5	Add tape and reel information	Jun	Bob
2013-06-05	1.6	1. Remove single cell application description 2. Change the RC filter parameter	Jun	Bob
2013-07-21	1.7	1. Change default value of Mode register 2. Change website address character	Jun	Bob
2013-12-29	1.8	1. Change default value of Config register from 0x50 to 0x18 2. Uniform ℃ character type	Jun	Bob
2014-9-10	2.0	Rotate the package orientation in the tape	Jun	Bob
2015-7-13	2.1	1. Add CSP package information 2. Revised the default value of version register	Jun	Bob