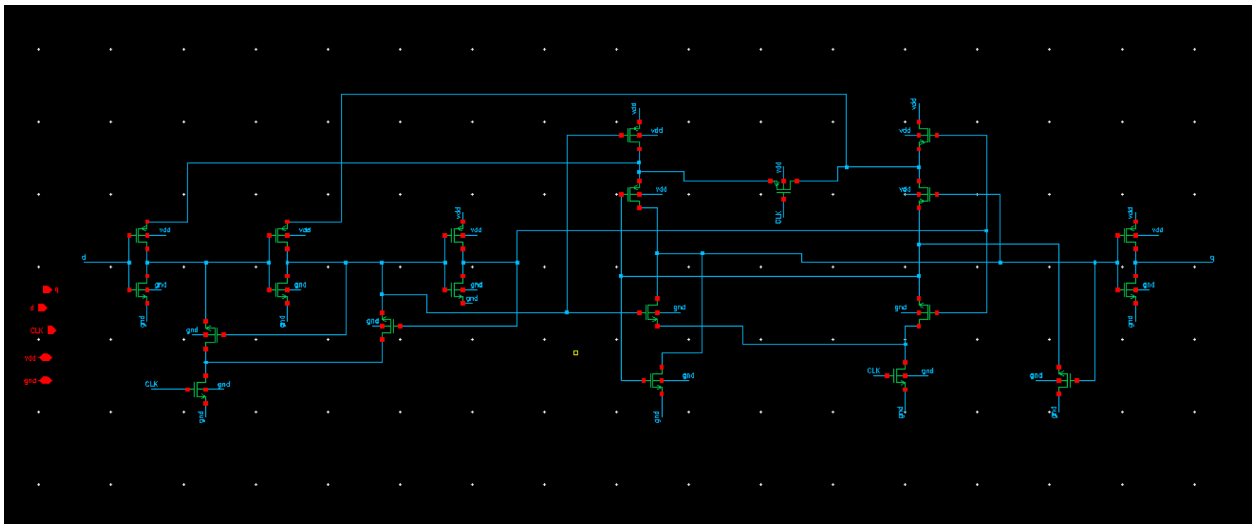
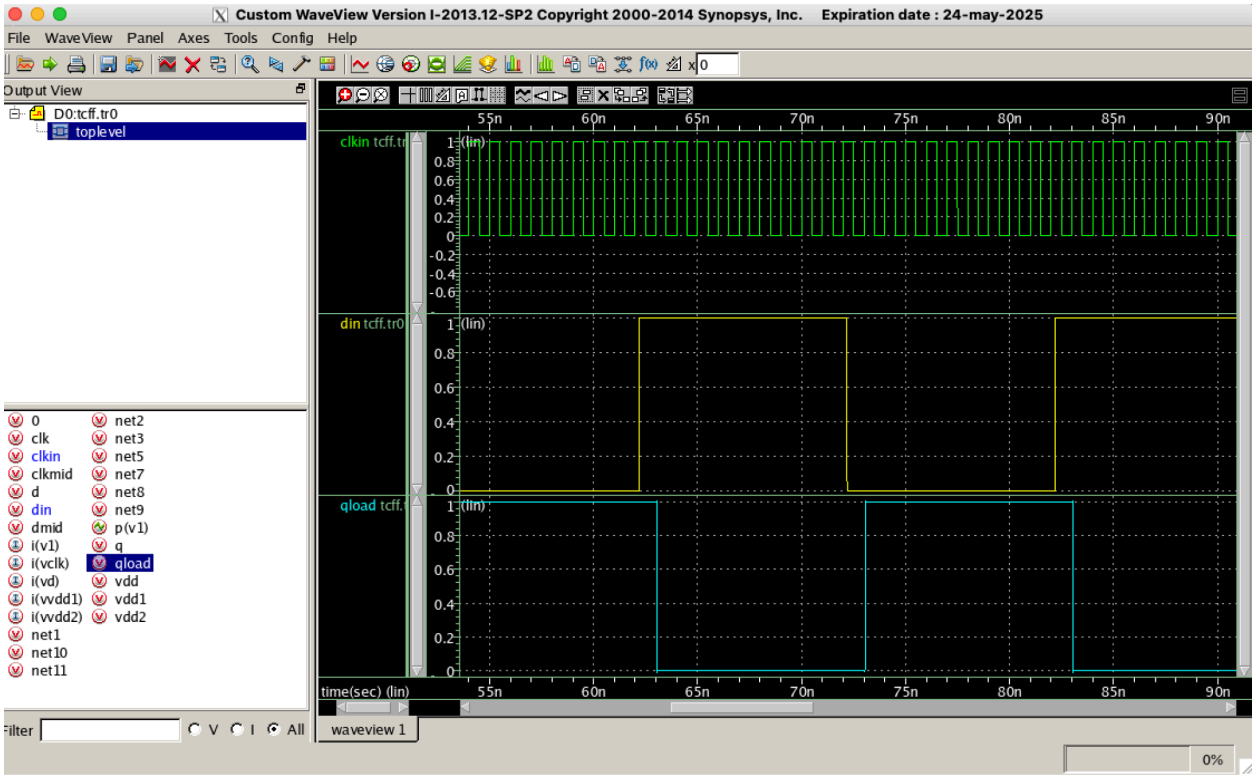
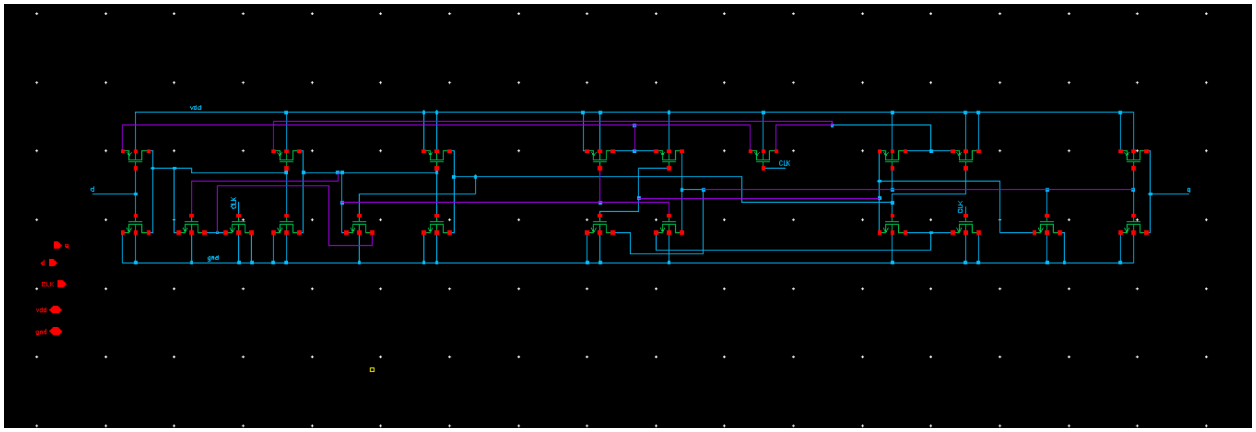
James Holt
TCFF, Topologically compressed flip flop
"A Fully Static Topologically-Compressed 21-Transistor Flip-Flop With 75% Power Saving" by Kawai

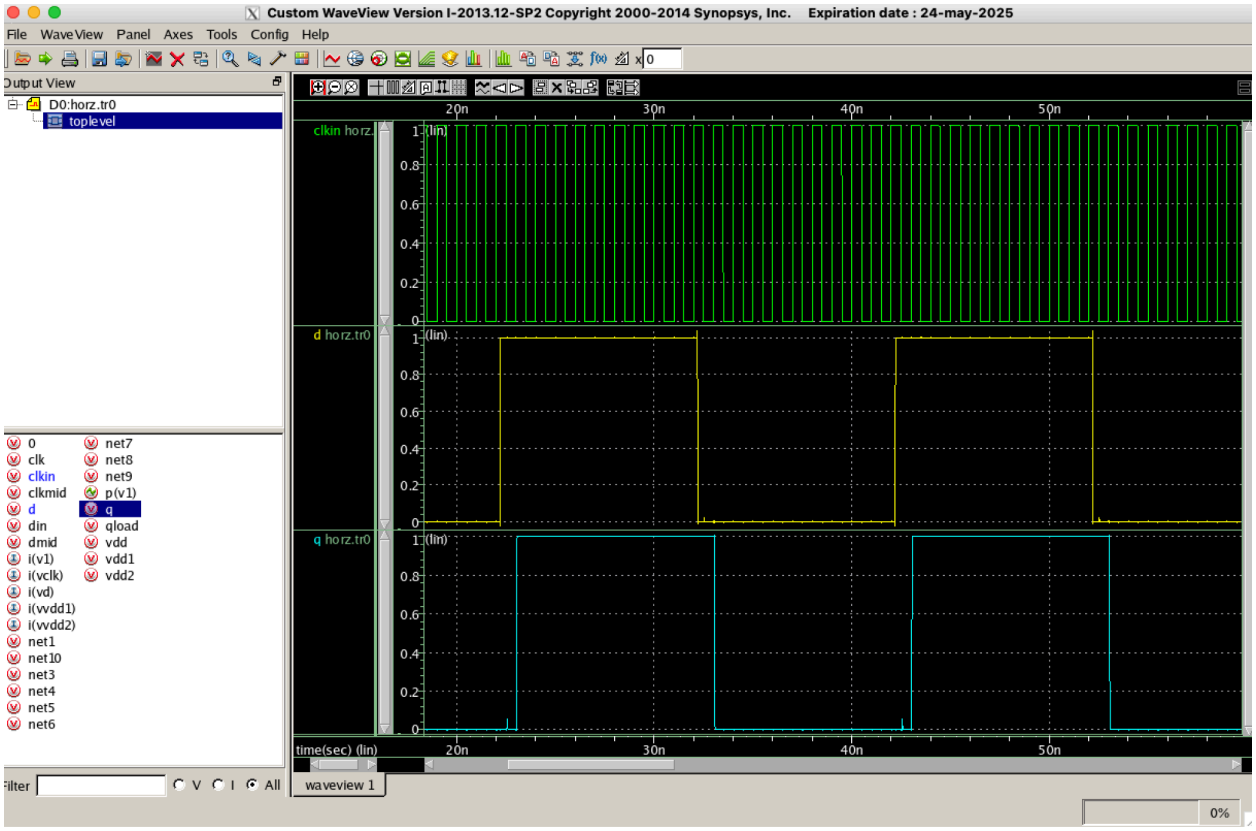
Vertical schematic:





Horizontal Schematic:

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clkin horz.tr0
d horz.tr0
q horz.tr0
(lin)
20n
30n
40n
50n
time(sec) (lin)
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net7 net8 net9 p(v1) q qload vdd vdd1 vdd2
Filter
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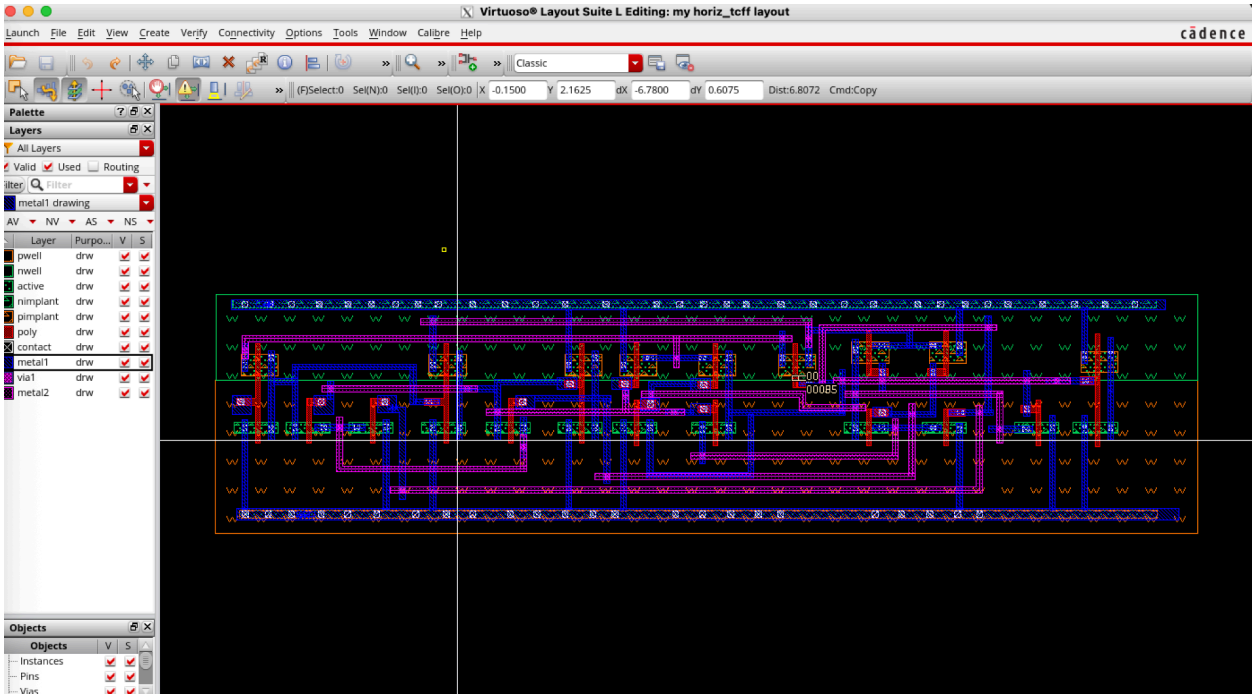
Layout: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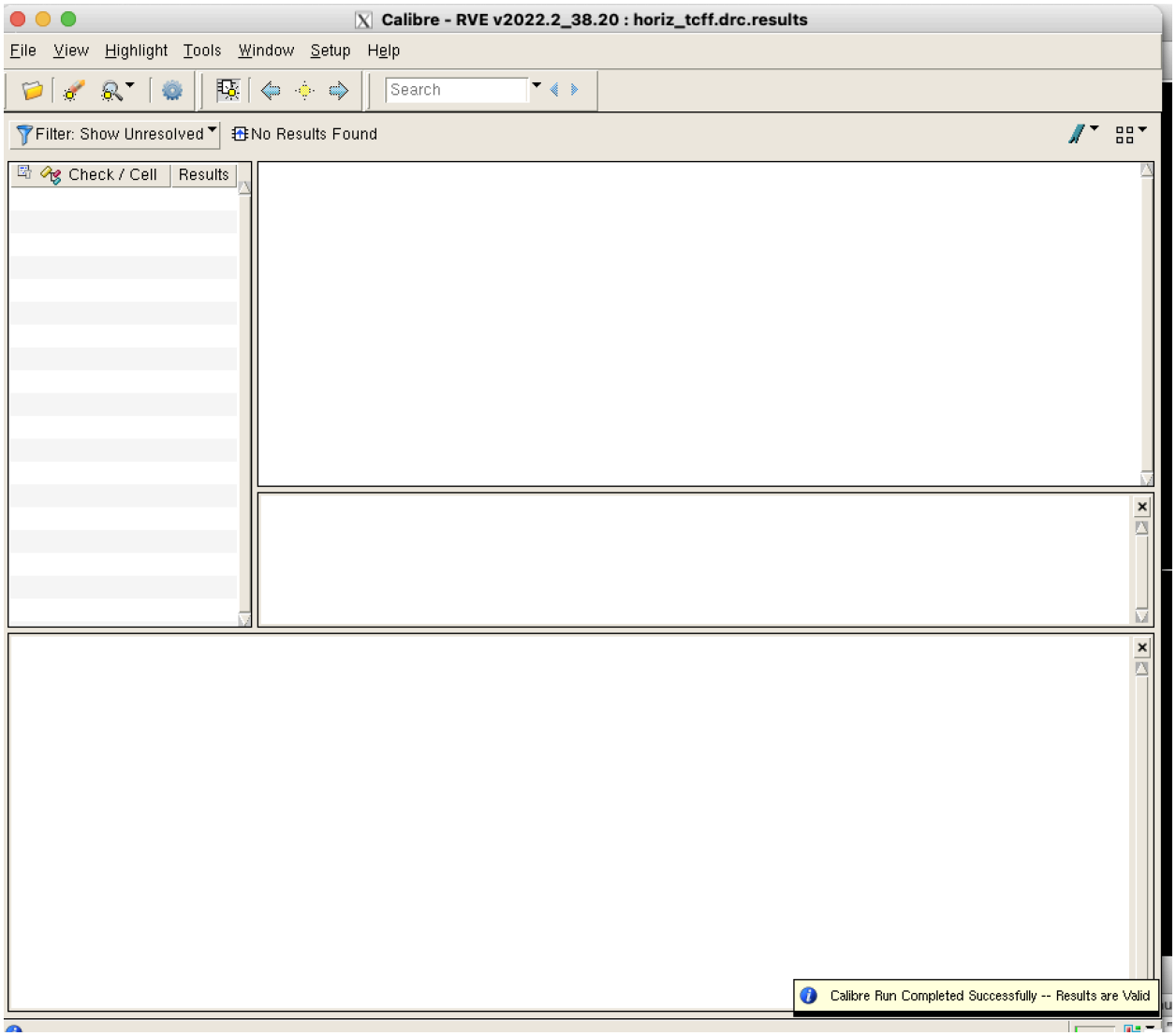
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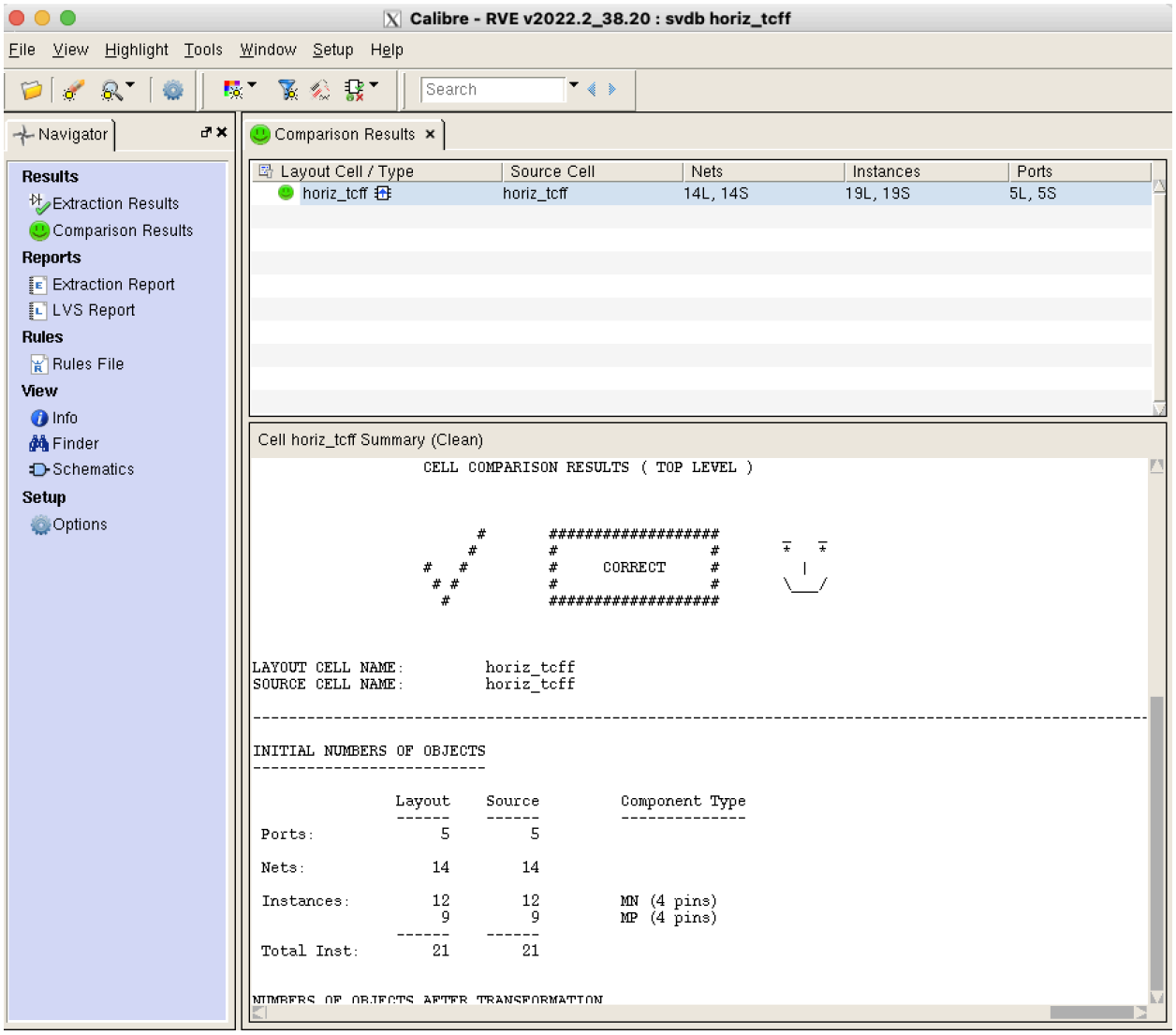
Calibre Run Completed Successfully -- Results are Valid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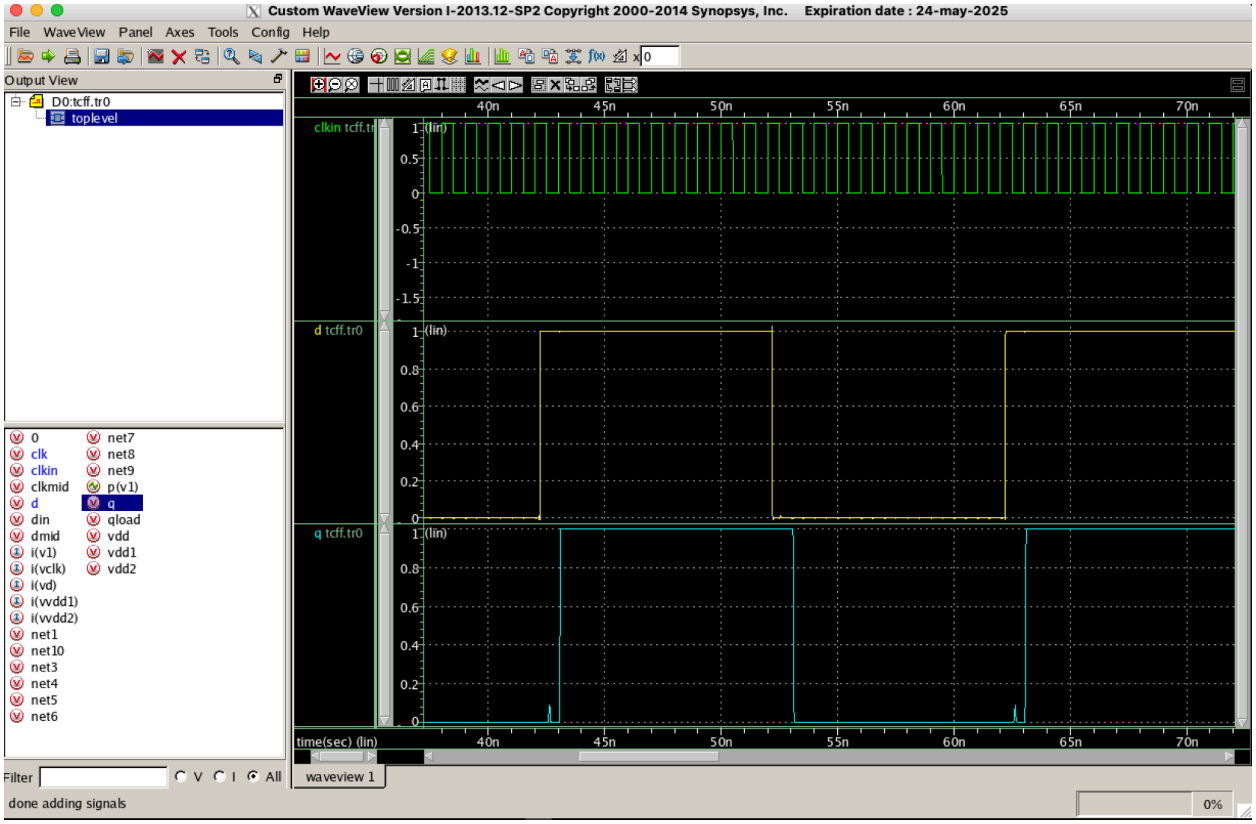
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
horiz_tcff
horiz_tcff
14L, 14S
19L, 19S
5L, 5S
Cell horiz_tcff Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: horiz_tcff
SOURCE CELL NAME: horiz_tcff
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 5 5
Nets: 14 14
Instances: 12 12 MN (4 pins)
9 9 MP (4 pins)
Total Inst: 21 21
NUMBERS OF OBJECTS AFTER TRANSFORMATION

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What went wrong:

I didn't have too much issues with this project as it was similar to lab 7 and I had learned small things to avoid like width and distance restrictions so that my DRC didn't have too many errors to go back and fix. I think the hardest part was making sure everything was connected correctly when I was doing my layout from my horizontal schematic. I know my layout could have been designed better to waste less space and resources but due to time constraints I chose to go the most direct route.

Note: sorry in my tar file my vertical schematic is in TCFF and my horizontal schematic is in horiz_TCFF