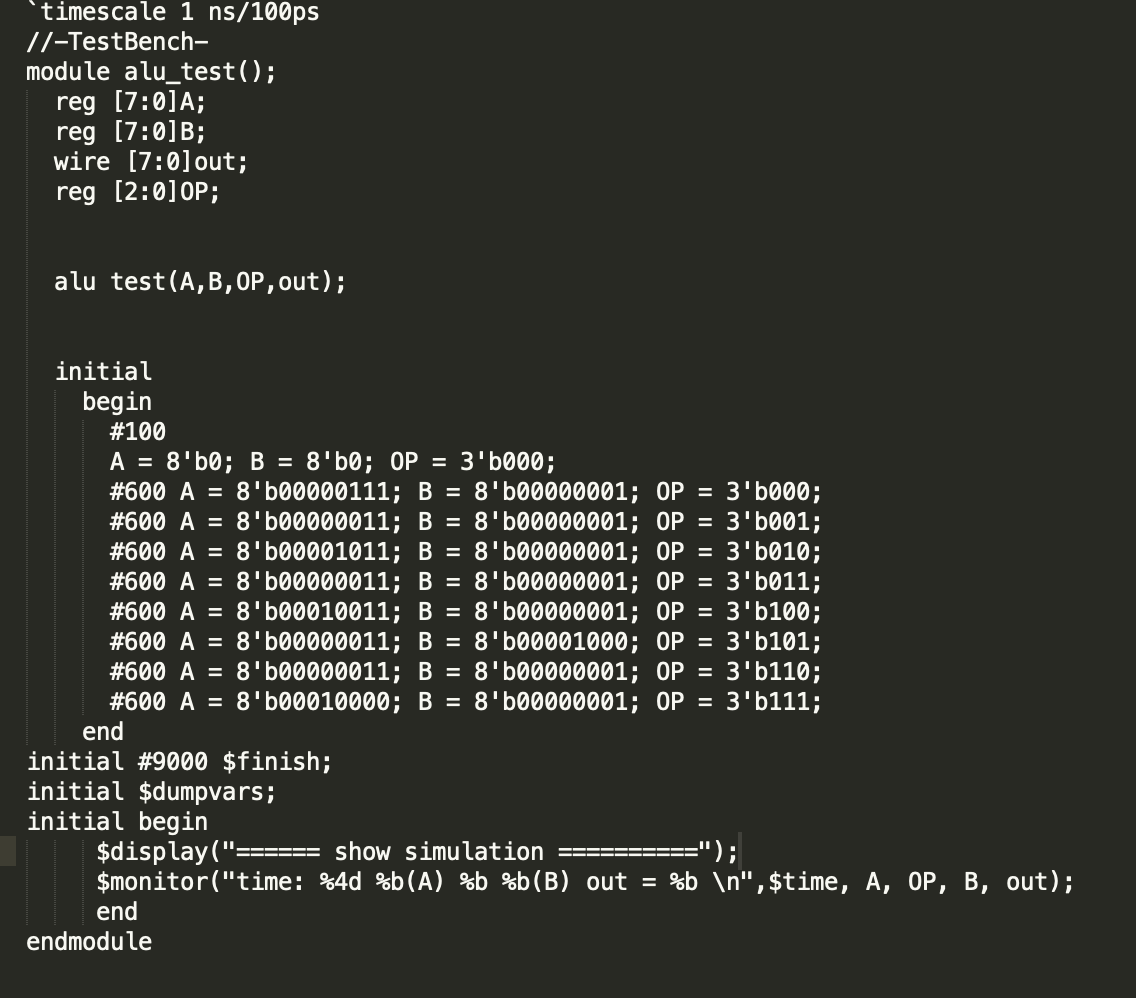
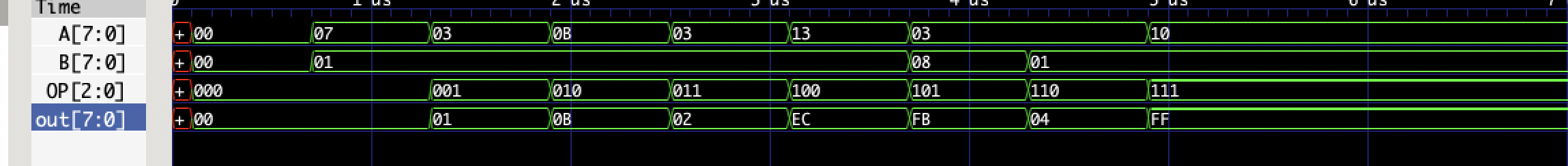
Verilog project3 b10601002 廖品捷

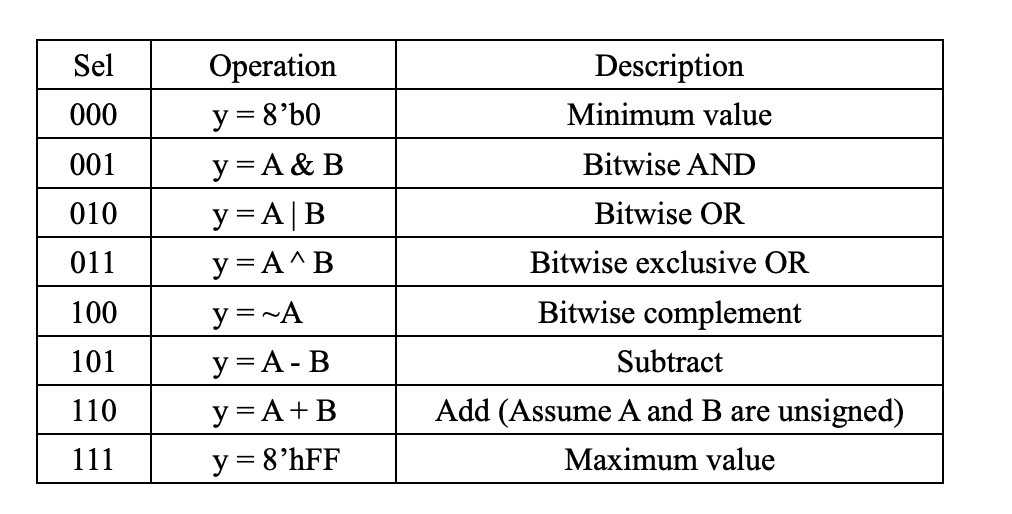
Github: <https://github.com/JamesLiao714/DLD-verilog>

Test bench:

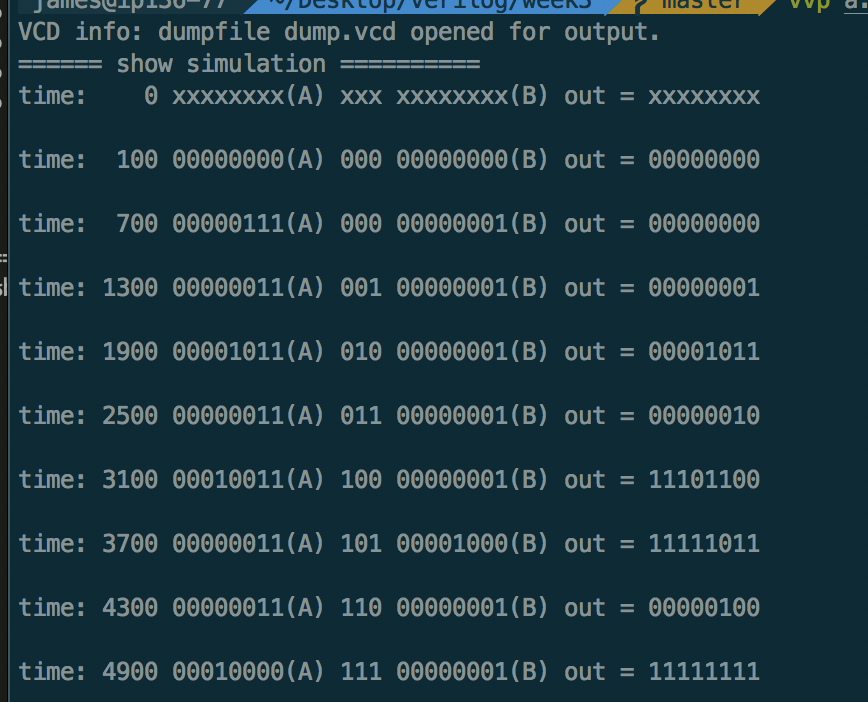


ALU Waveform:





implementation of $monitor, $display and $time:



ALU Model source code:

