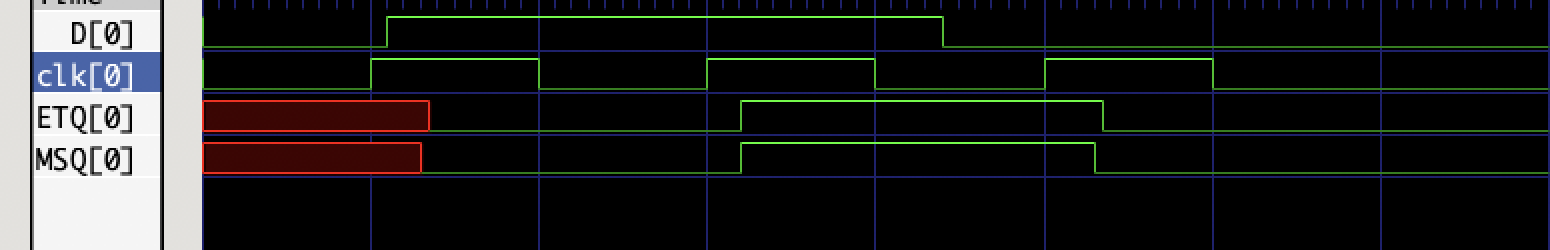
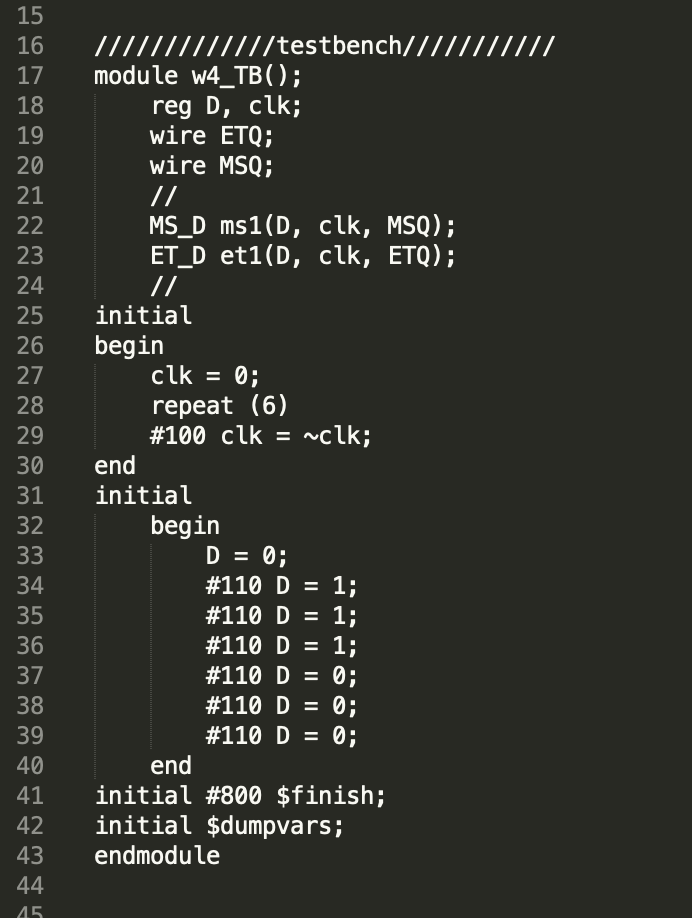
Verilog project4 b10601002 廖品捷

Github: <https://github.com/JamesLiao714/DLD-verilog>

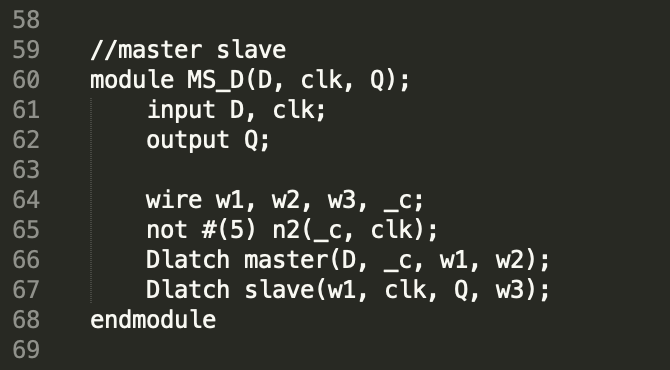
Waveform:



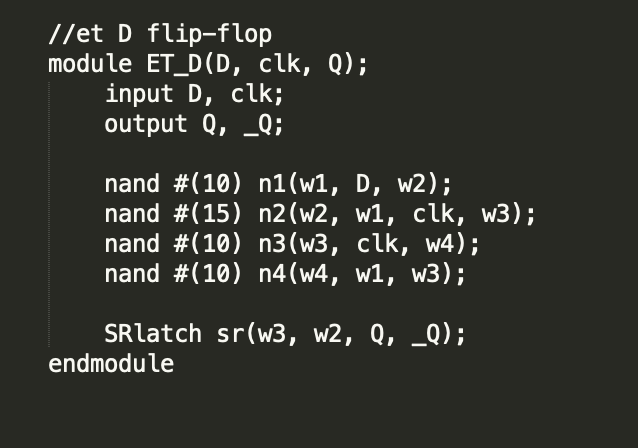
Test bench:



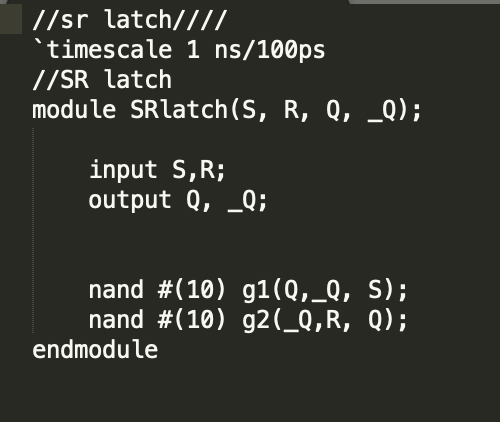
1. the gate-level description of master-slave D flip-flop（positive edge trigger）



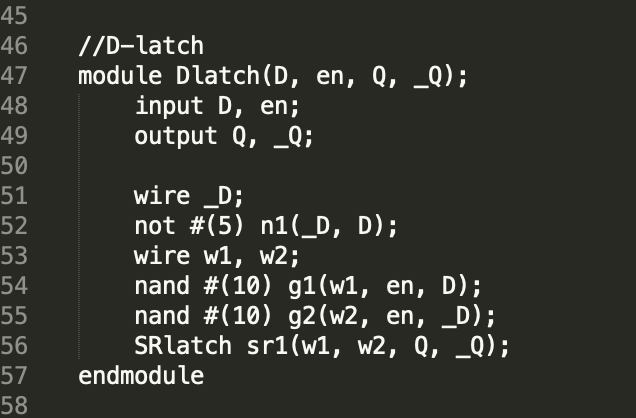
1. the gate-level description of edge-triggered D flip-flop



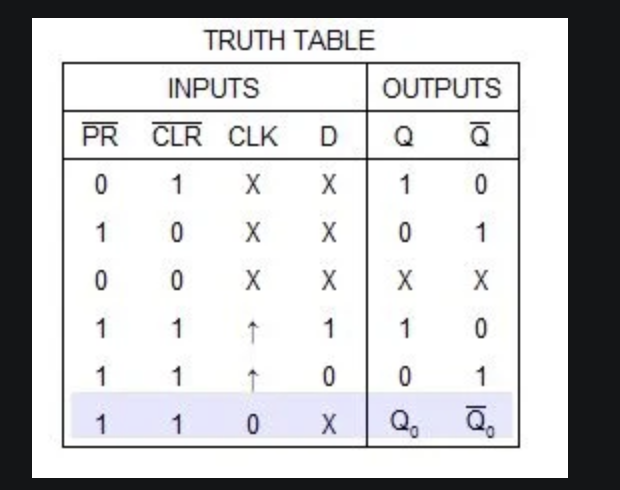
SRlatch:

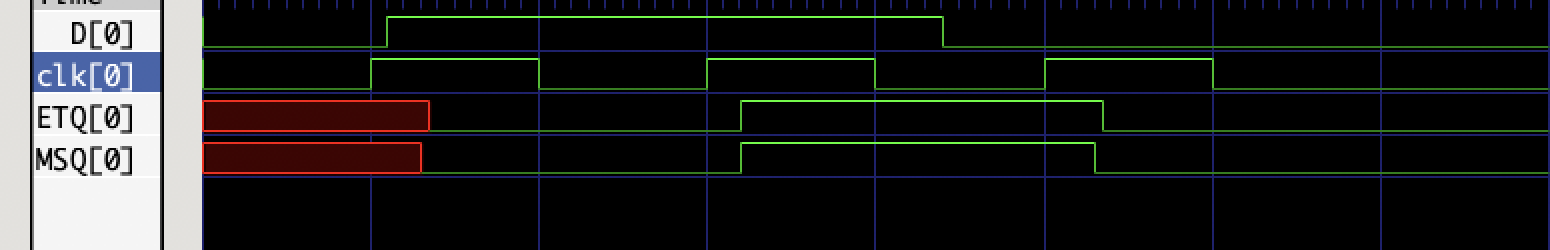


Dlatch:



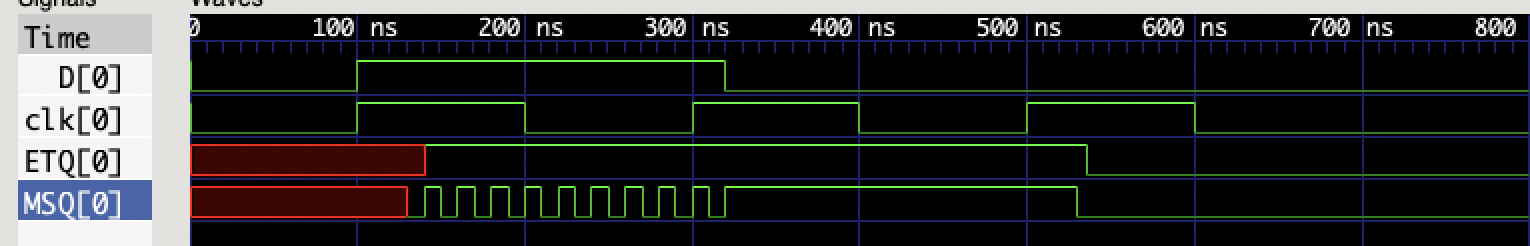
1. the behavior description (i.e., use always block) of D flip-flop





這是d-flip flop的真值表，我將masterslave範例的negative-edge trigger轉成positive,所以當clk從0變1時，Q的值會變成Ｄ。

一開始在實作testbench時沒把clock跟D的時間錯開，沒注意到setup time and hold time ，根據分析顯示holdup time如果小於11ns的時候master-slave會出現類似glitch的電路異常，最後我將clock的時間調早一點後解決了這個問題。而相較起來edge-trigger的實作則相當理想



this is the testbench that cause the violation