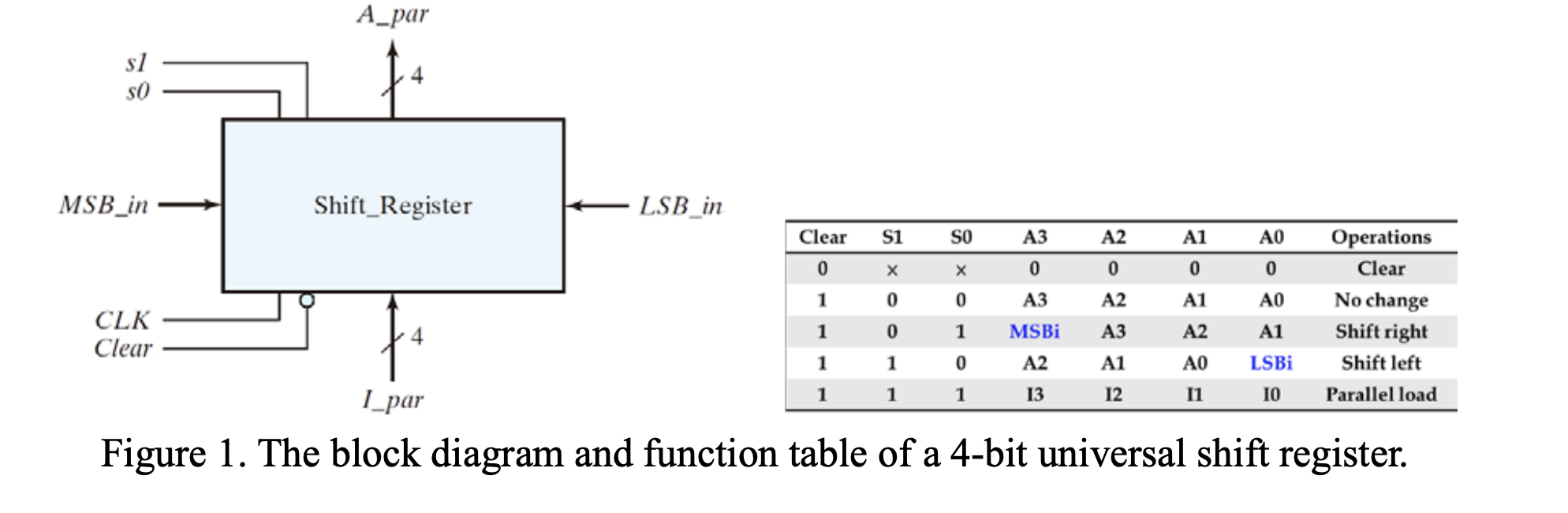
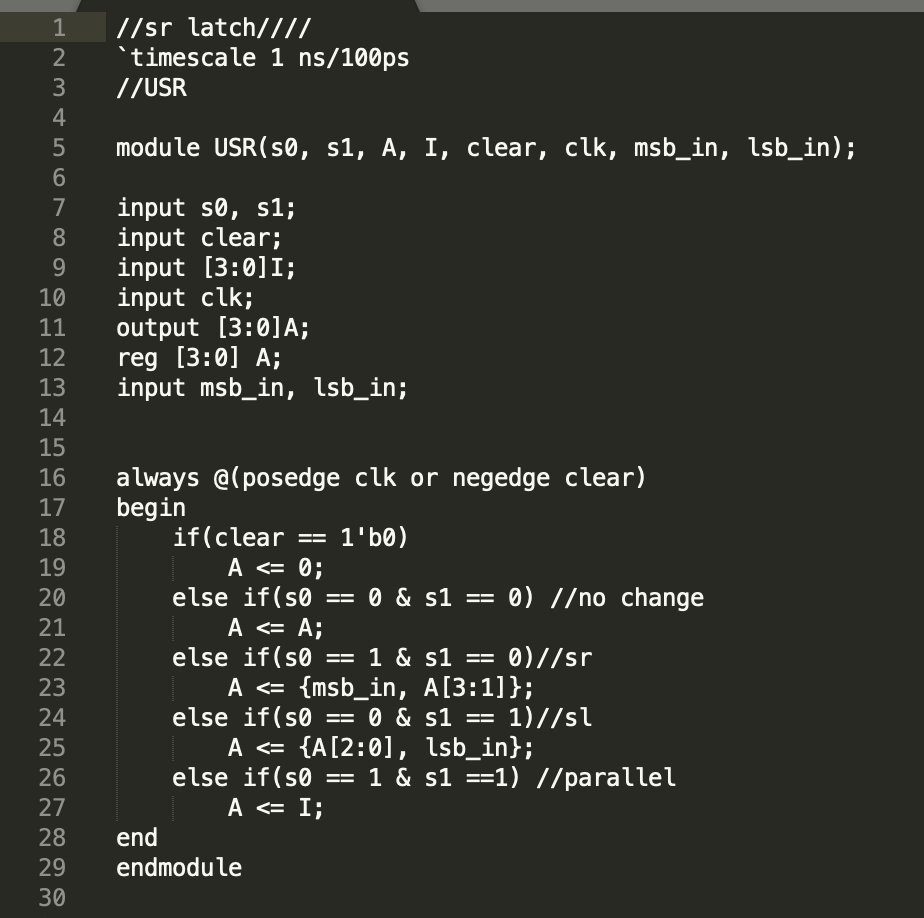
Verilog project4 b10601002 廖品捷

Github: <https://github.com/JamesLiao714/DLD-verilog>

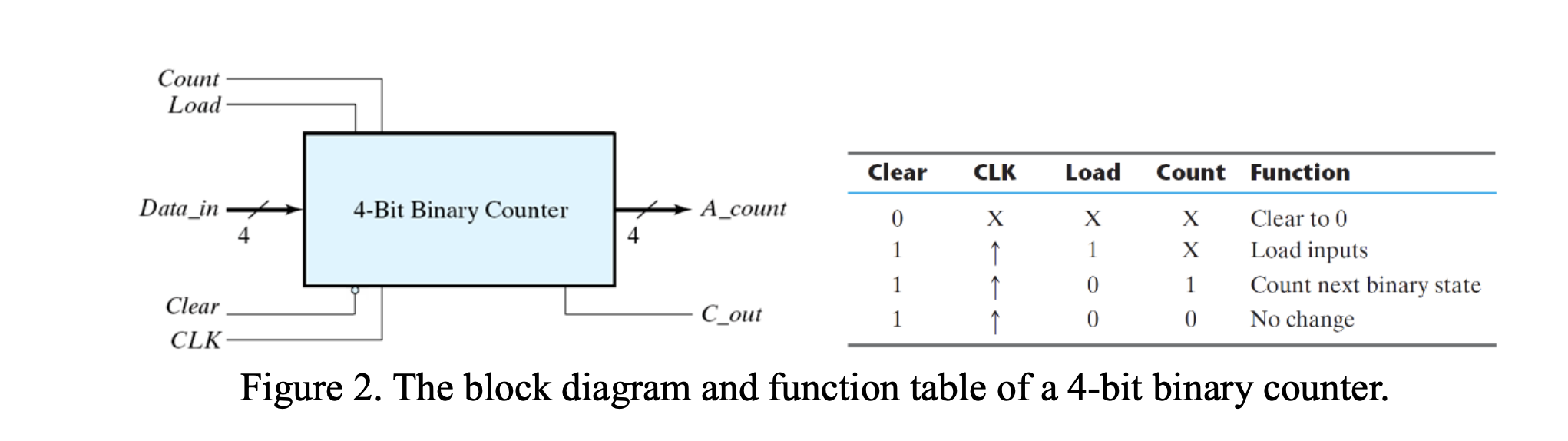
4-bit universal shift register



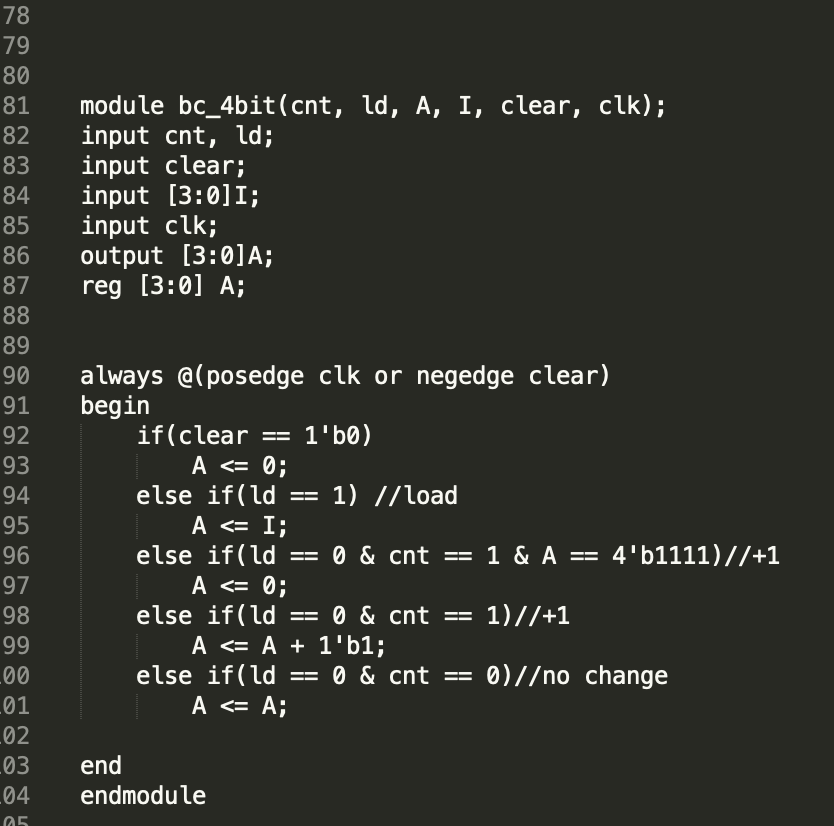
code:

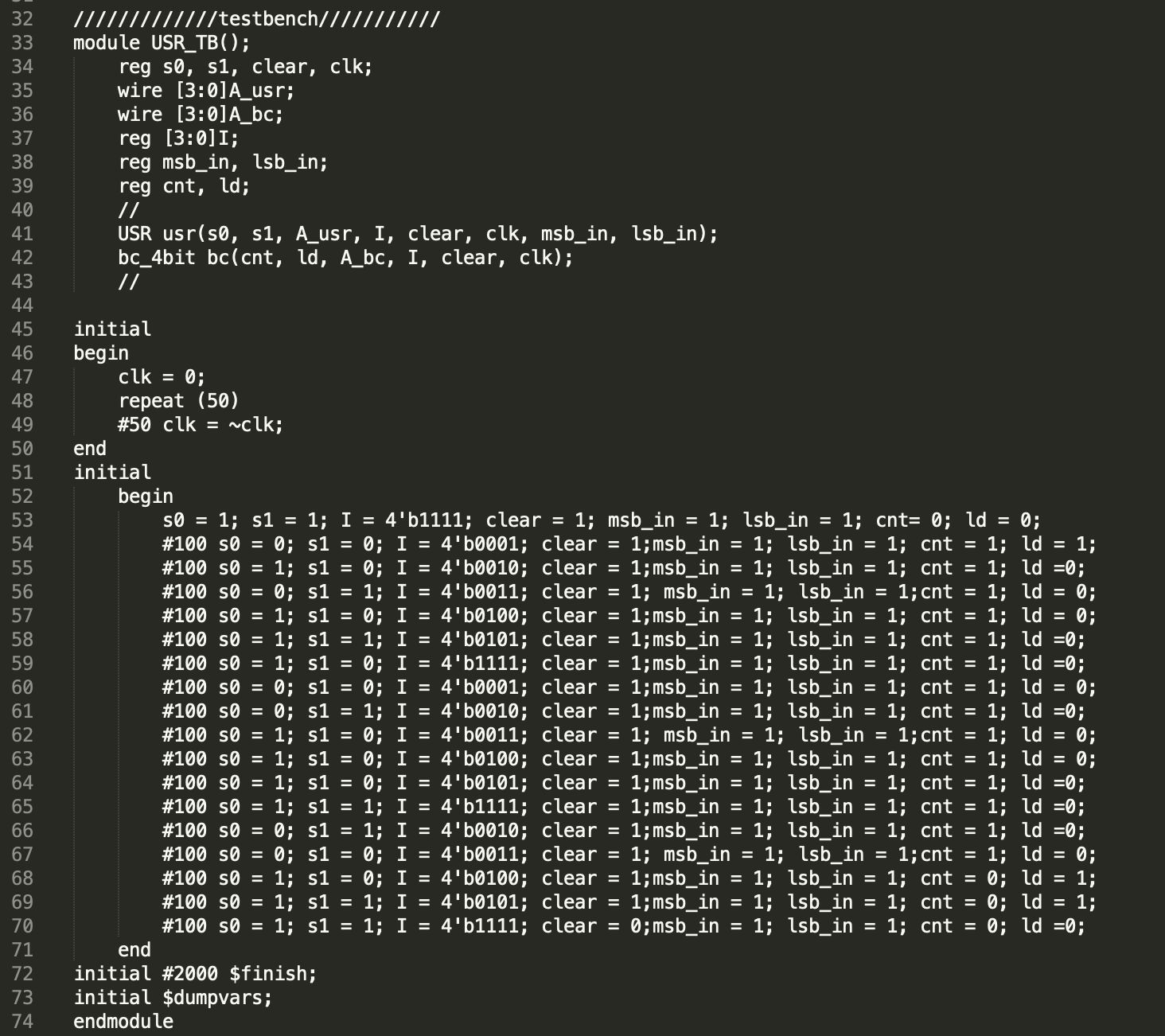


4-bit binary counter

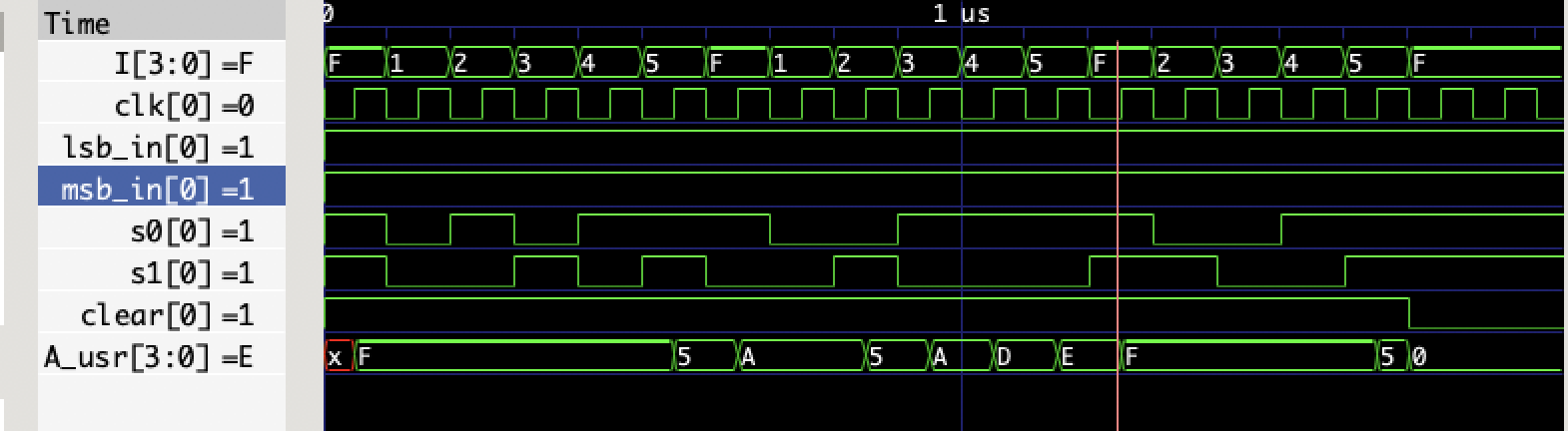


code:



test bench:waveform:

1. 4-bit universal shift register



2. 4-bit binary counter

