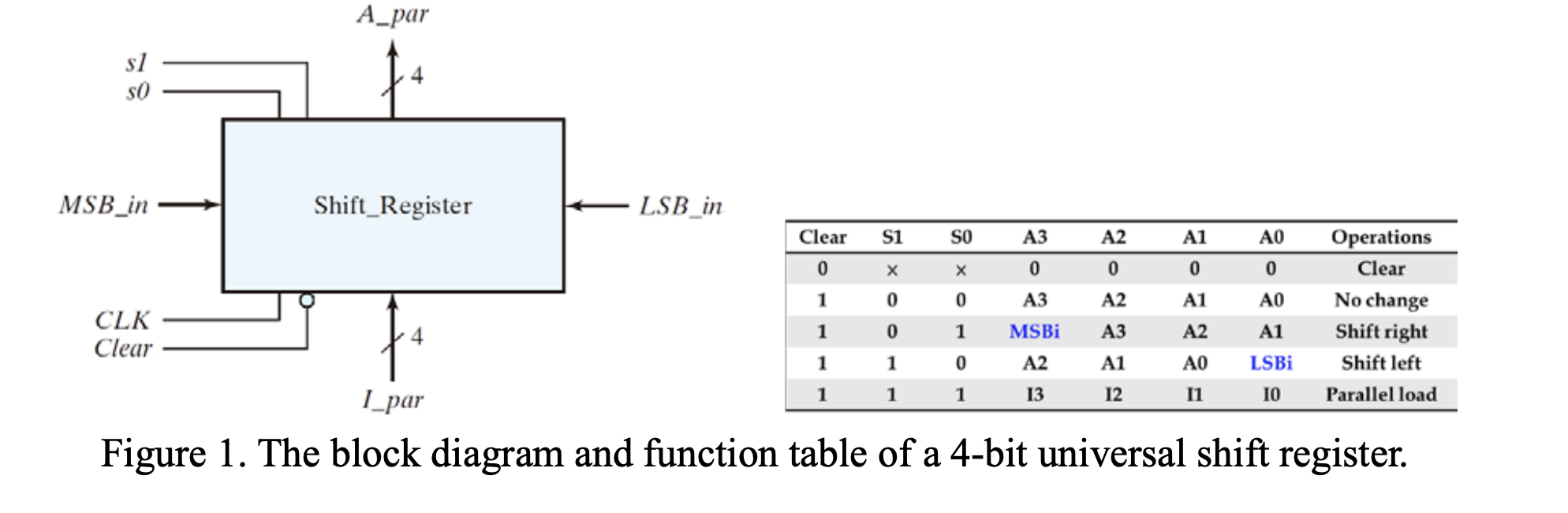
Verilog project5 b10601002 廖品捷

Github: <https://github.com/JamesLiao714/DLD-verilog>

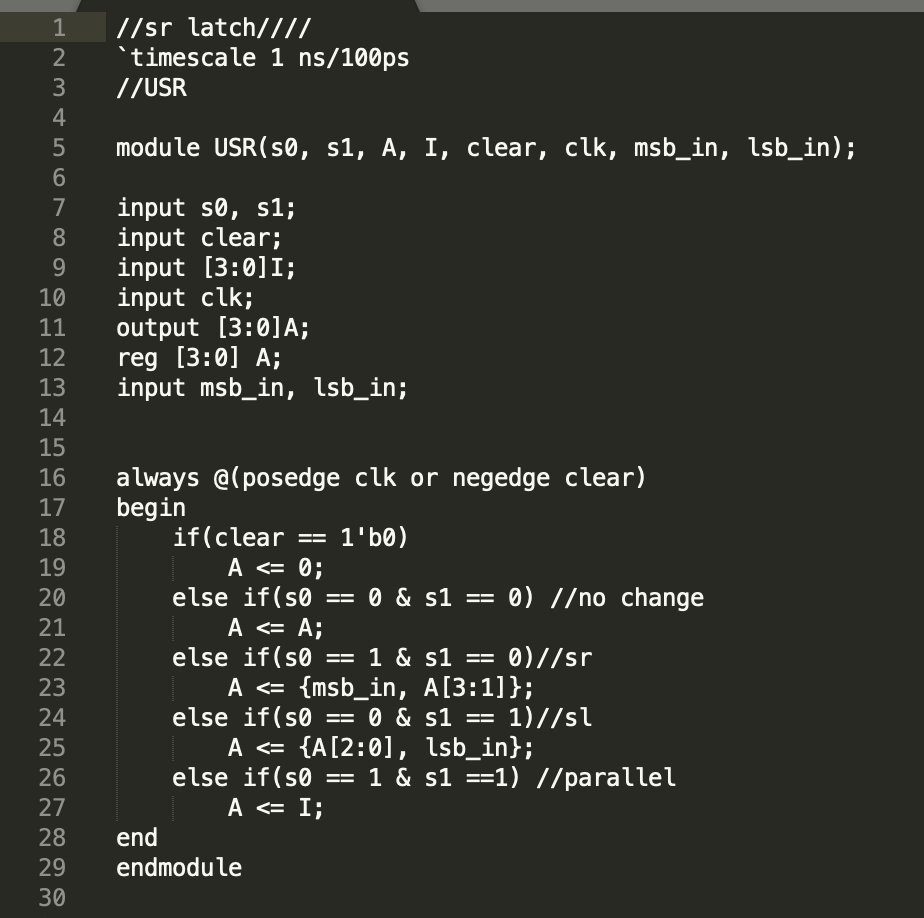
4-bit universal shift register

根據S1 和 S2 的值來決定output的function

當clear為0時將Ａ清為0



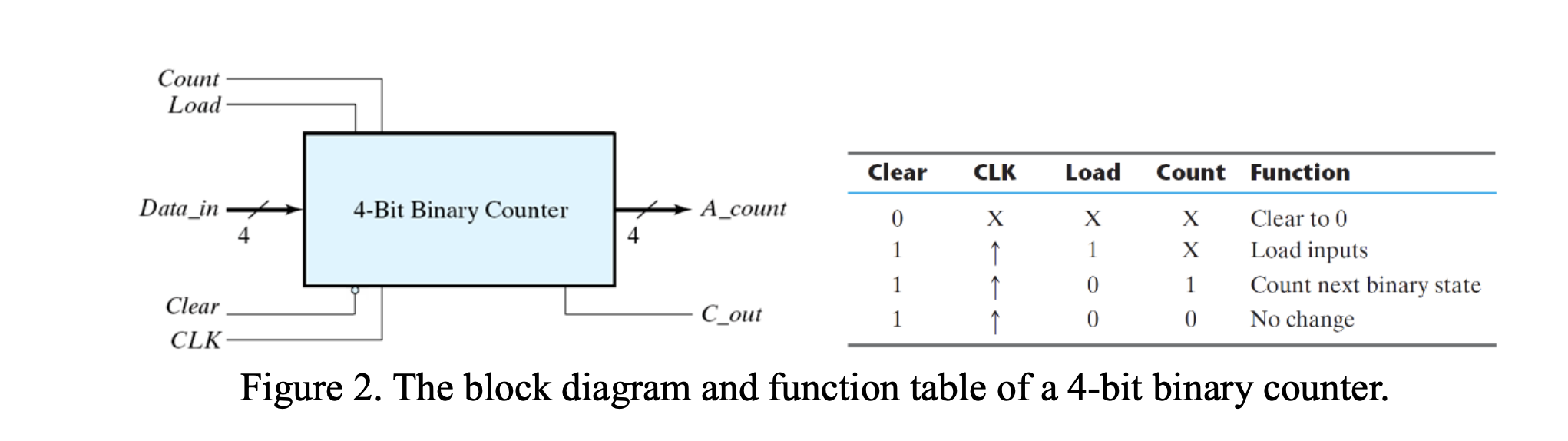
code:



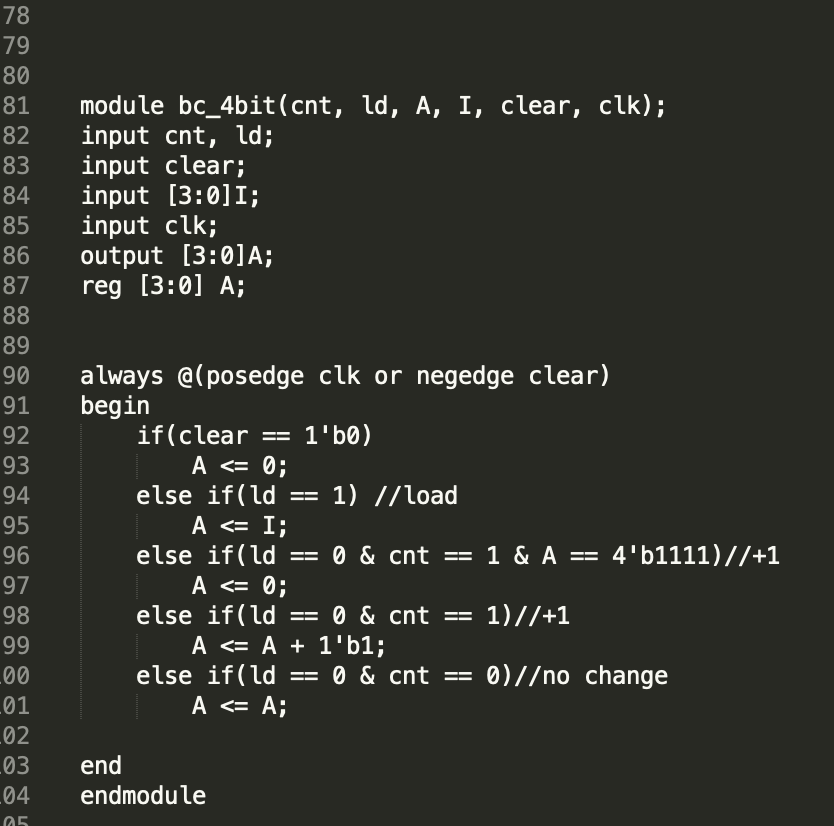
4-bit binary counter

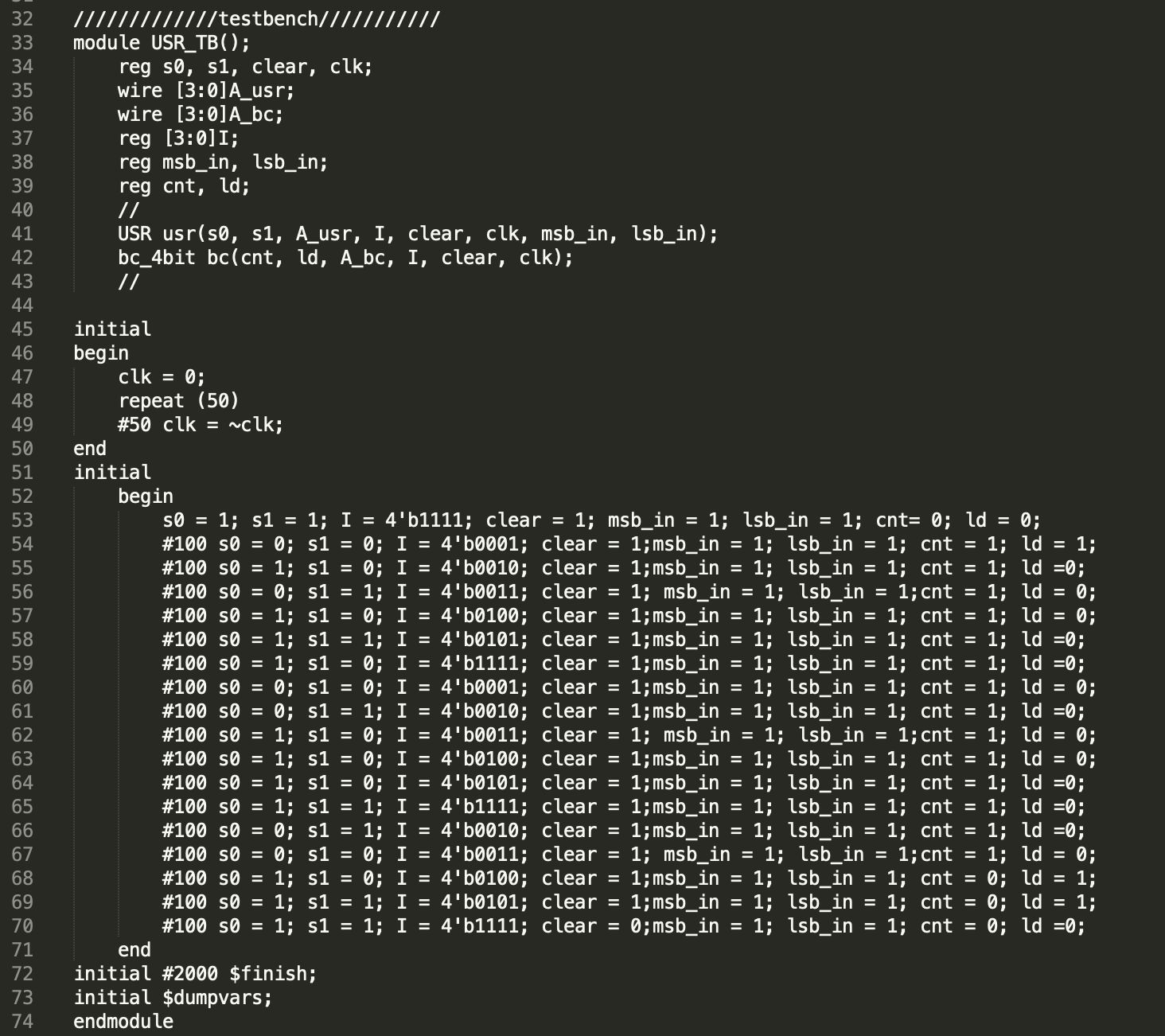
根據load 和 count 的值來決定output的function

當clear 為0時 講output清為 0



code:

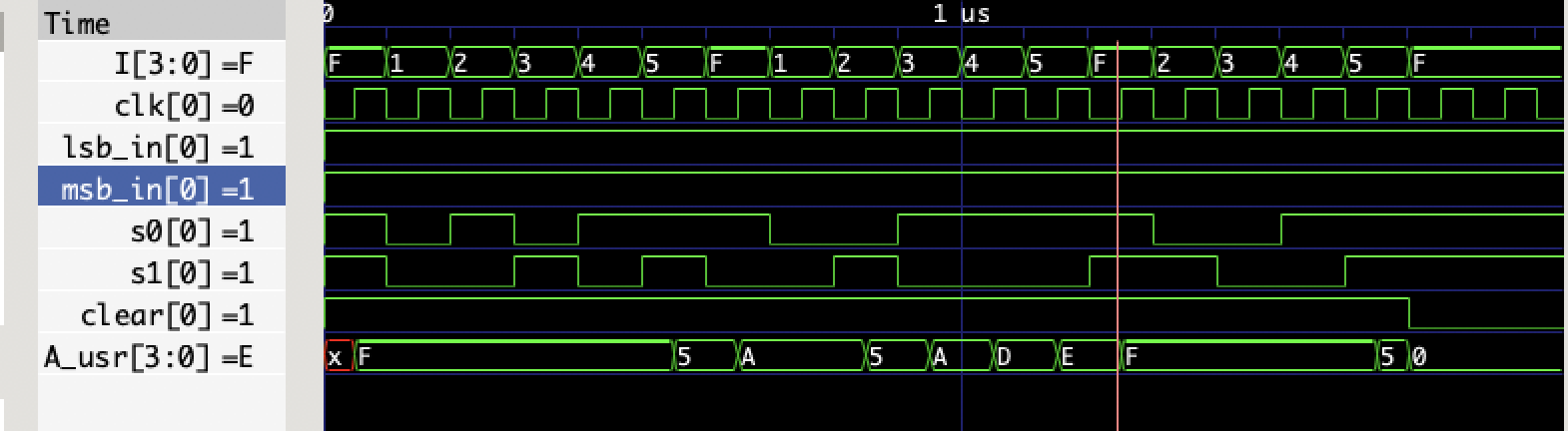


test bench:waveform:

實作模擬如下圖

1. 4-bit universal shift register

A\_usr為根據s0,s1 所產生的output(shift…)



1. 4-bit binary counter

A\_bc為根據ld 和cnt所產生的ouput(計數, load I)

