Evaluation Board AD1555/AD1556 24-Bit Σ-Δ ADC

Preliminary Technical Data EVAL-AD1555/56EB

FEATURES :

- **On-Board Reference, Oscillator, Control Logic and Buffers**
- **Easy interface to printer port of PC**
- **PC Software for Control and Data Analysis**
- **Stand Alone Capability to ease design**
- **Analog and Digital Prototype Area**

GENERAL DESCRIPTION

The EVAL-AD1555/56EB is an evaluation board for the AD1555 and AD1556 24-bit Σ-Δ ADC chip-set. The AD1555/AD1556 chip-set can convert a high dynamic range input signal, operates from +5V and -5V supplies and uses a serial interface.

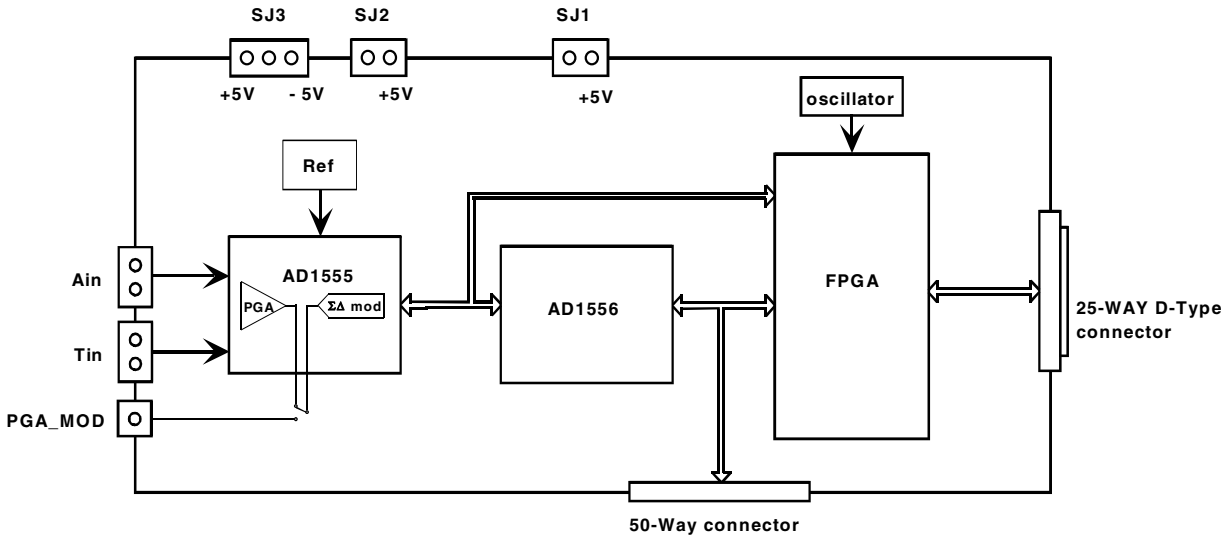
The AD1555/AD1556 evaluation board is designed to demonstrate the ADC's performance and operation. A full description of the AD1555/AD1556 is available in the AD1555/AD1556 data sheet and should be consulted when utilizing this evaluation board.

The EVAL-AD1555/56EB is ideal for use either as a stand-alone evaluation board to interface with a customer application or with any compatible PC using the parallel printer port.

On-board components include an AD780 3V ultra low noise bandgap reference, a crystal oscillator, and digital control logic. The board has both a Centronics male connector to interface with PC printer port and a 50-pin connector for stand-alone operation.

Software is provided to allow simple demonstration and evaluation of the AD1555/AD1556 chip-set.

FUNCTIONAL BLOCK DIAGRAM



REV. PrD

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

OPERATING THE EVAL-AD1555/56EB

The EVAL-AD1555/56EB is a two-layer board carefully laid out and tested to demonstrate the specific high dynamic performance of the chip-set.
Figure 4 shows the schematics of the evaluation board.
The layout of the board is given in the next four figures :
Figure 5 shows the Top side silk-screen.
Figure 6 shows the Top layer.
Figure 7 shows the Bottom side silk-screen.
Figure 8 shows the Bottom layer.
The available test points are listed in Table I and a description of each selectable jumper is listed in Table II. The component list is provided in Table III.

Power Supplies and Grounding :

The EVAL-AD1555/56EB has three power supply blocks: a single +5V supply V_{cc} (SJ1) for the evaluation board digital section, another +5V or +3.3V supply V_L (SJ2) for the digital supply of AD1555 only and a +/-5V supply (SJ3) for the analog section of AD1555.

The evaluation board ground plane is separated into three sections: a DGND plane for the AD1556 and the digital interface circuitry, a LGND plane for the digital section of AD1555 and an analog AGND plane for the AD1555, its analog input and external reference circuitry. To facilitate grounding connections of test equipment and attain high performance the board was designed with a good isolation barrier between the AD1555 and the rest of the digital functions. This isolation barrier is not required in applications where the analog and digital ground are not tied together externally. That is achieved using optocouplers and high value resistors. The analog ground and AD1555 digital ground can be tied together close to the AD1555 using JP2 which is the optimal configuration.

Analog inputs :

Fully differential signals could be applied on either A_{IN} and T_{IN} inputs through SMB plugs. The analog input ranges have to be compatible with the PGA gain settings used as described in the AD1555/AD1556 datasheet. The modulator section of the AD1555 can be separately evaluated using the PGA_MOD SMB plug.

TABLE I. EVAL-AD1555/56EB Test Points

Test Point	Available Signal
TP1	REFIN (3V)
TP2	DGND (FPGA)
TP3	DGND (AD1556)
TP4	CB0
TP5	CB1
TP6	CB2
TP7	CB3
TP8	CB4
TP9	MDATA
TP10	MCLKOUT
TP11	MFLG

TABLE II. JUMPER DESCRIPTION

Jumper	Function
SW1	To get all the software functionality, SW1 should be in the position where the identification dot on the core of the switch is visible. When SW1 is in the other position (the switch hole is hidden), the AD1556 could be controlled externally using the 50-pin connector P2. (see chapter using the EVAL-AD1555/56EB in customized system for details).
JP1	JP1 controls the input signal applied to the AD1555 modulator input MODIN. In position A, the PGA output is applied to MODIN. In position B, the signal on PGA_MOD SMB plug is applied to MODIN.
JP2	JP2 allows LGND and AGND to be tied together close to the AD1555 which is generally the preferred configuration.

RUNNING THE EVAL-AD1555/56EB SOFTWARE

Software Description :

The EVAL-AD1555/56EB comes with software for analyzing the AD1555/AD1556 chip-set. This software allows comprehensive control and evaluation of the AD1555/AD1556 chip-set or the AD1555 and the AD1556 separately. The front-end PC software has only one screen shown in Figure 1. This screen is partitioned into five windows which allows the user to select the configuration, launch the sampling sequence, perform computation on the output signal and display the results. The choices for display are Time domain response, Spectral response and histogram chart. Different measurements as Dynamic range, equivalent input noise, Total Harmonic Distortion (THD) and DC offset can be done. Figure 1 describes the steps to follow for proper software operation.

Software Installation :

The EVAL-AD1555/56EB software runs under Windows95. It requires a minimum of 7MB hard-disk space available and a display with a minimum resolution of 800 by 600. Due to the real-time operation, it is recommended that other programs be closed when using the EVAL-AD1555/56EB software.

The EVAL-AD1555/56EB software installation process is:

- Run Setup.exe using the EVAL-AD1555/56EB disk 1 and follow the instructions. The files can be stored in any directory at the user convenience using the destination folder field. The default folder is C:\Program Files\Ad1555_56.

- Run AD1555_56.exe to launch the software. It will open the window in figure 1.

- If the window in figure 1 exceeds the actual screen, the display resolution needs to be increased by opening Start>Settings>Control Panel>Display then settings> 800*600 for desktop area >apply>OK.

- The software uses a special font which can be installed using Start>Settings>Control Panel>Fonts>File>install new fonts> then select ADILogo Regular in the working directory then OK.

- To operate the software, follow the 5 steps described in figure 1.

Using the EVAL-AD1555/56B in the customized system :

The EVAL-AD1555/56EB is also designed to ease the evaluation and the design of the AD1555 and the AD1556 in the customized system. The useful interface signals can be connected to the customized system using the connector P2. The switch SW1 in the position where the identification dot of the switch is hidden changes the configuration of U1 as follows :

- The AD1556 CLKIN at 1.024MHz is supplied by U1 (exact division by 8 of U5 oscillator).

- U1 transmits the AD1556 MCLK output (256kHz) to the AD1555 MCLK with the appropriate phase (one inversion is done by U1 in order to cancel the U9 inversion).

- U1 output pins PGA0-4, CS*, R/W*, DINM1, BW0-2, H/S*, RSEL, CSEL, PWRDN, RESET, SYNC, SCLKOUT, TDATA are Hi-Z .

This configuration allows the control of these signals by the customized system. The AD1555 and AD1556 clock are still generated by the EVAL-AD1555/56EB.

TABLE III. Component List.

Integrated Circuits

U1	FPGA EPM7128ELC84-15.
U2	AD1556AS.
U3	AD1555AP.
U4	reference AD780AN.
U5	Oscillator 8.192MHz.
U6	Buffer 74HC245.
U7	Invertor 74HC04.
U8,U9	Optocoupler HCPL2630.

Capacitors

C1-C6,C8-C9,C11-C12, C14-C16,C22-C24,C27, C29-C31,C33,C34	100nF Ceramic Capacitors.
C7,C10,C13,C17-C18, C21,C25,C26,C28	10μF Tantalum Capacitors.
C20	22μF Tantalum Capacitor 6.3v.

Resistors

R6,R10-R15	47.5KΩ Resistor.
R1-R5	13KΩ Resistor.
R8,R9	4.7KΩ Resistor.
R17,R21,R22	2KΩ Resistor.
R18-R20	402Ω Resistor.
R16	10Ω Resistor.

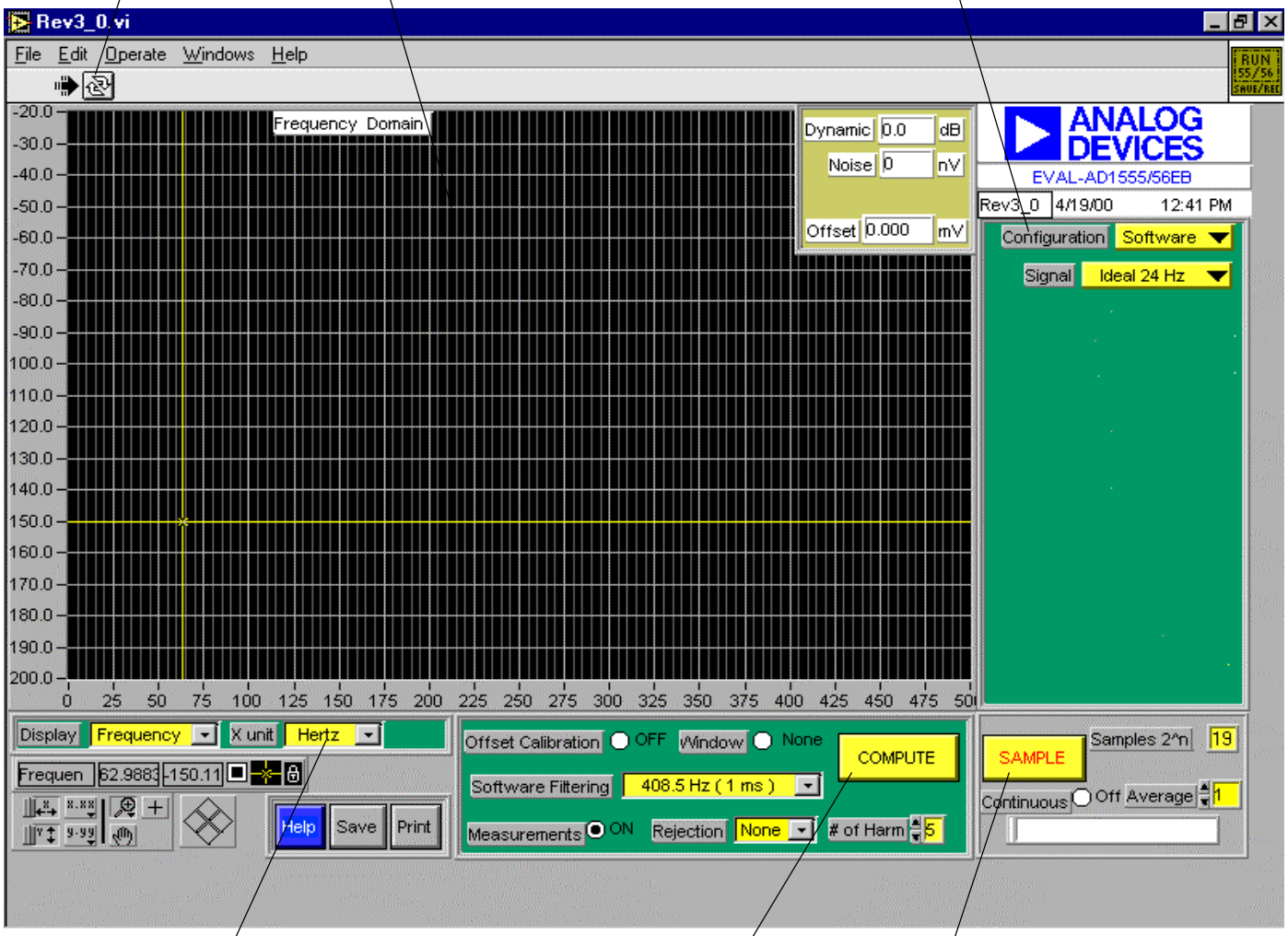
Sockets

P2	50pin Male ribbon cable connector.
P1	25pin DB-25 connector.
JP2	2 Position Male jumper strip.
PB1	SMT push-button.
SW1,JP1	Slide Switch.
SMB1-SMB5	SMB Connector.

Step 1 Start execution: click on the double-arrows icon to start execution.

Step 2 Configuration menu: Selects Configuration, Signal input, PGA gain setting, AD1556 filter selection, power controls, interface settings.

Display window : displays either Time domain or Frequency domain or Histogram and/or performance values such as dynamic range, equivalent input noise level, THD and DC offset.



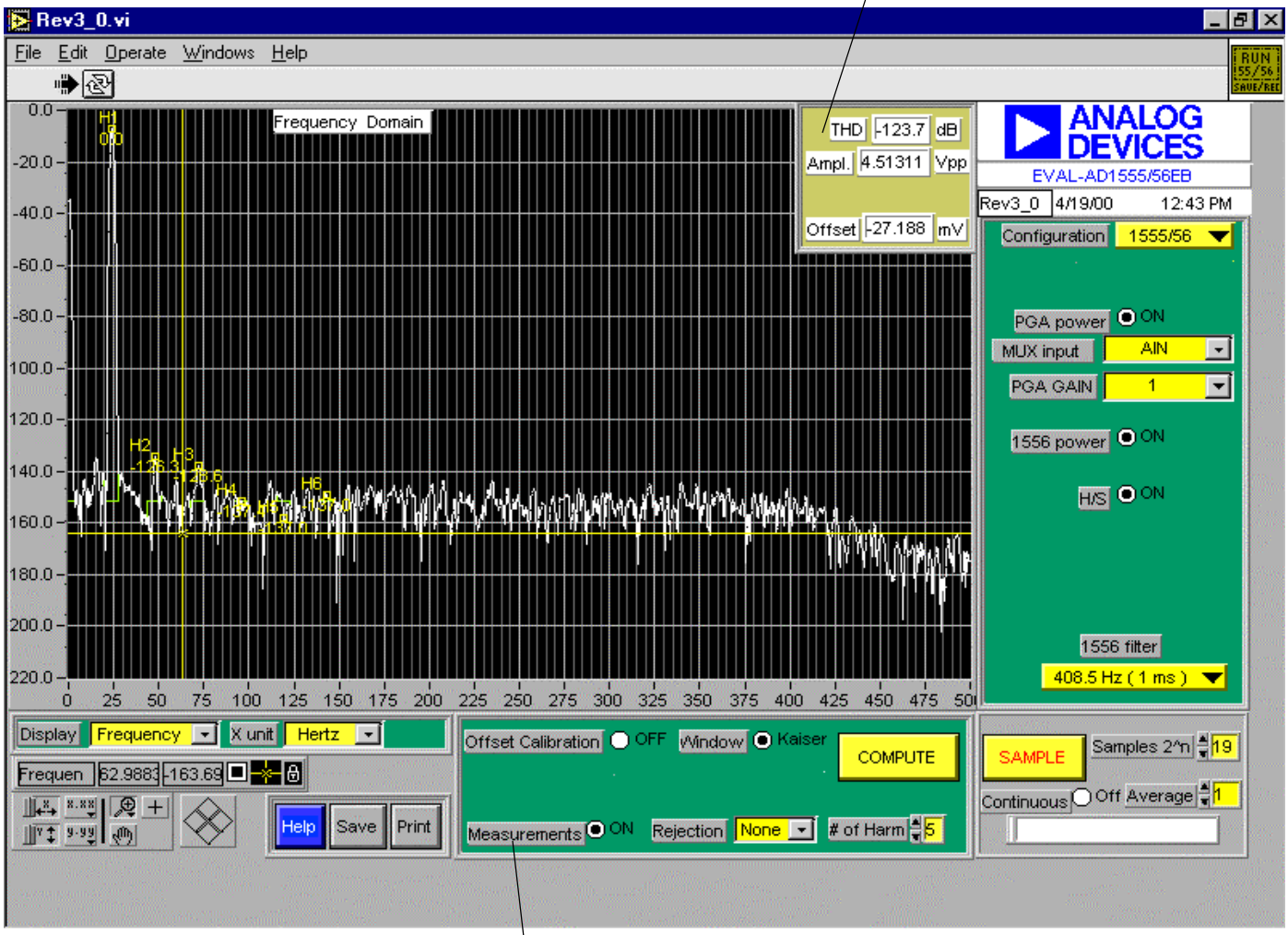
Step 5 Display menu : selects Time/Frequency domain or histogram, controls display parameters (scales, zoom, cursor...), and controls outputs (save to file or print).

Step 4 Computation menu : COMPUTE launches the specified computation data process before display, allowing windowing, software filtering or measurements computation if desired. Compute sequence should be done again after changes into computation, sampling, configuration menus. F3 is the key command for "compute".

Step 3 Sampling menu : after the desired samples number is selected, SAMPLE launches a sampling sequence. When complete, "Successful" will appear in the status window. If not, verify the configuration and the hardware setup. When the configuration or sampling menu is modified, a sampling sequence should be done again. F2 is the key command for "sample". "Continuous" allows continuous running sampling and computing (F4 is the key command key for "continuous"). "Average" allows the averaging between successive sampling.

Figure 1. Software main screen.

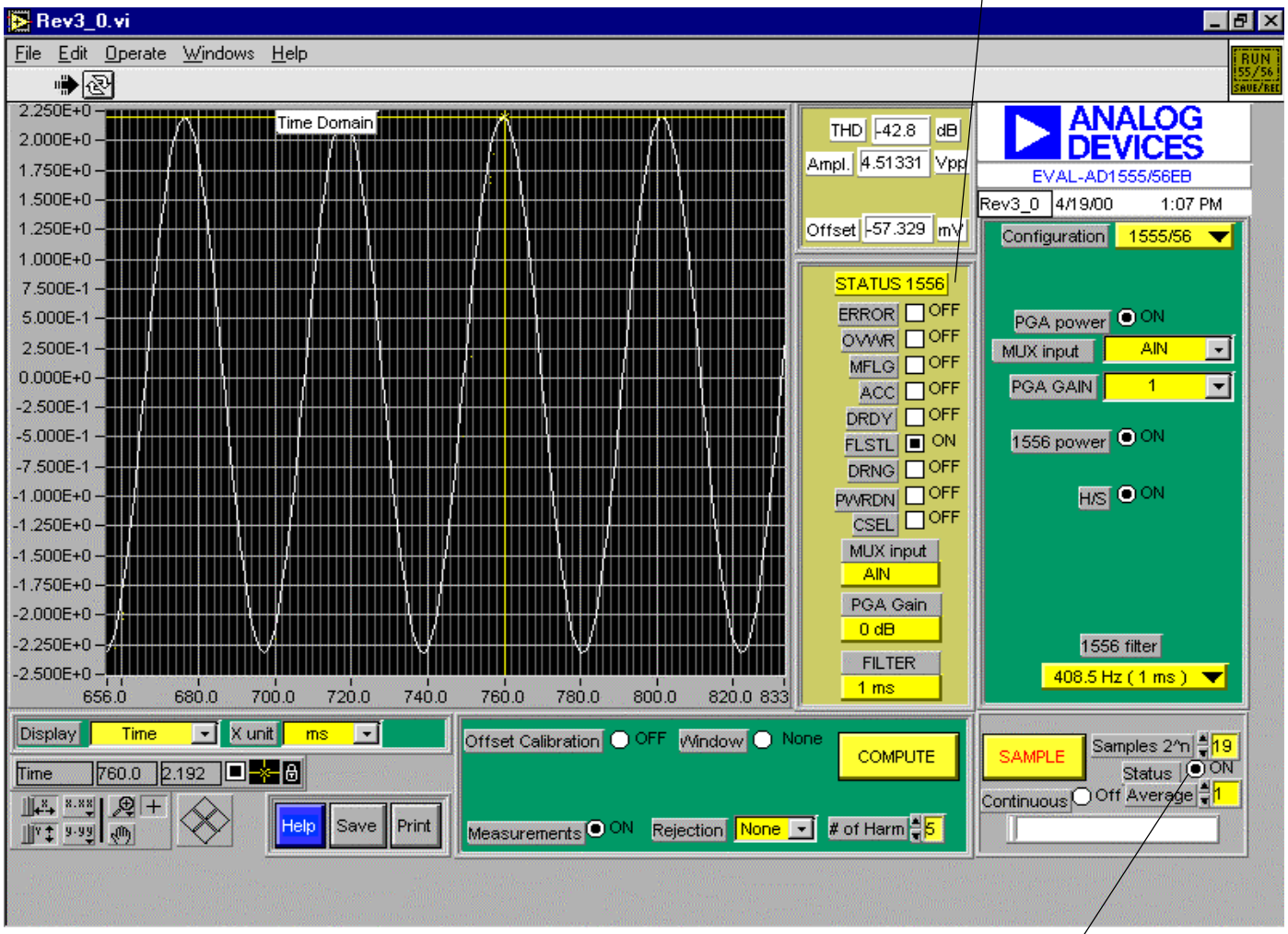
Measurements display : This window displays the measurements. When a signal approximately at least 10 times higher than the noise floor is detected, the THD is measured otherwise, the dynamic range and equivalent input noise are displayed.



Measurement enable : This button enables the measurements computation when on. 50 Hz or 60 Hz rejection filter can be used before noise computation. The number of harmonics uses in the THD computation is selectable.

Figure 2. Frequency domain screen with measurements.

Status Register display : This window displays each bit of the AD1556 status register. The displayed value is the status register value corresponding to the data value marked with the cursor in the time domain display.



Status enable : This button enables the AD1556 Status register reading. This feature is only available in time domain.

Figure 3. Time domain screen with AD1556 Status register content.

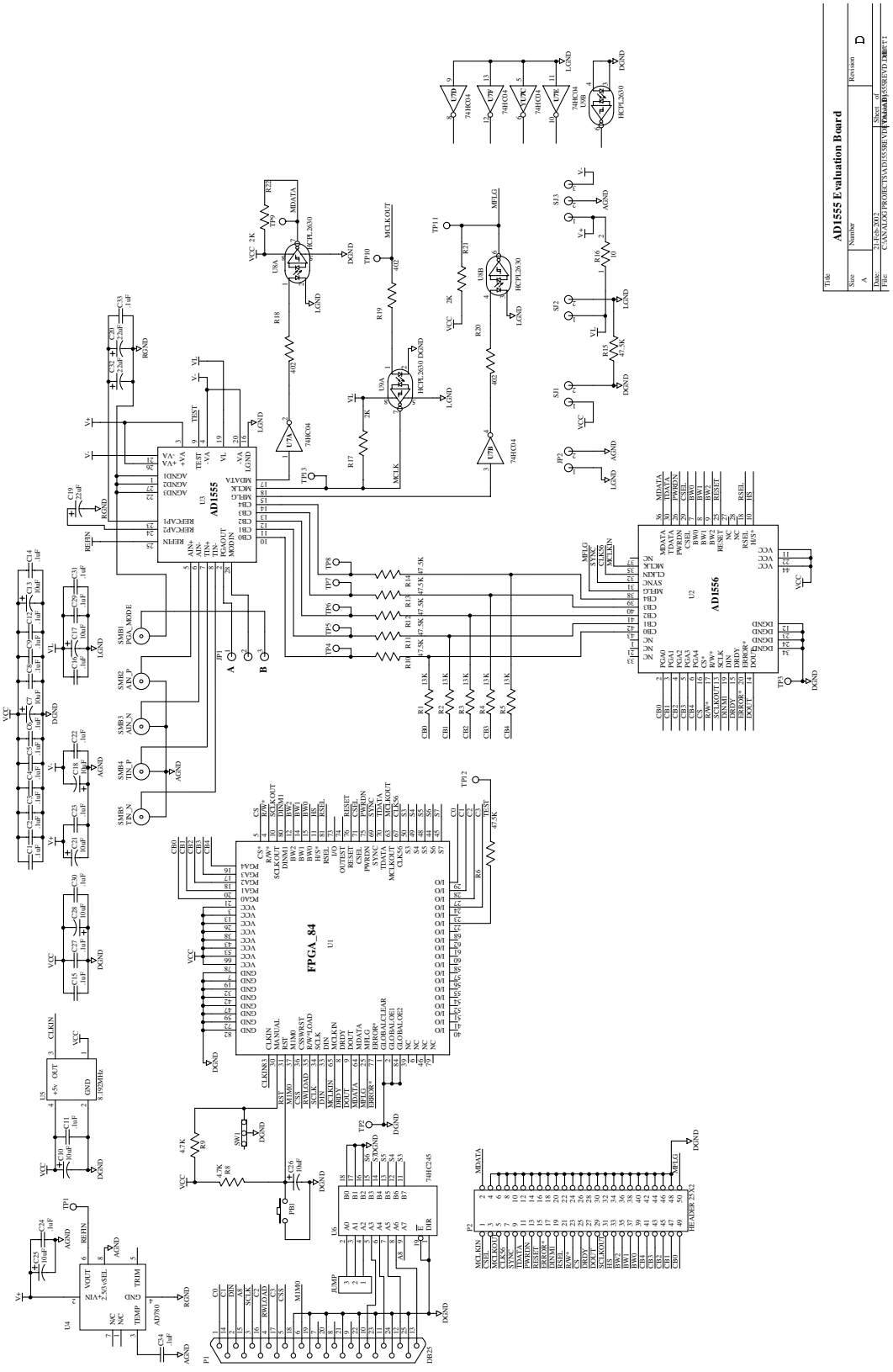


Figure 4. Schematics.

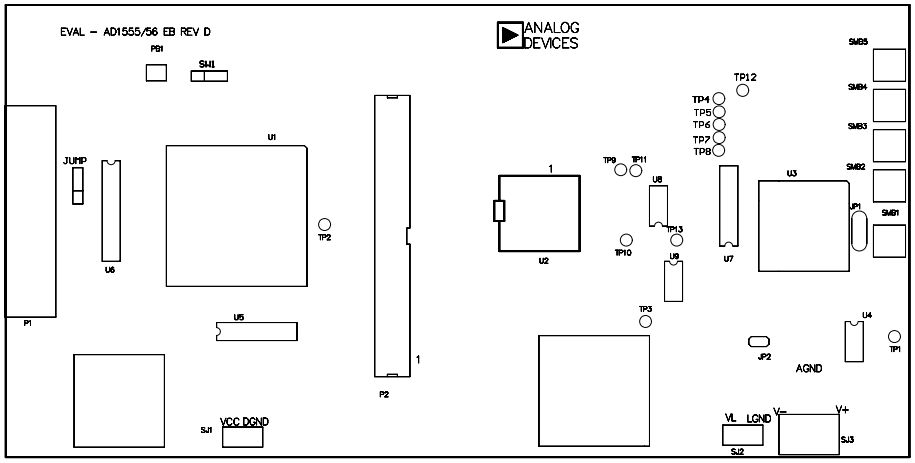


Figure 5. Top side silk-screen (not to scale).

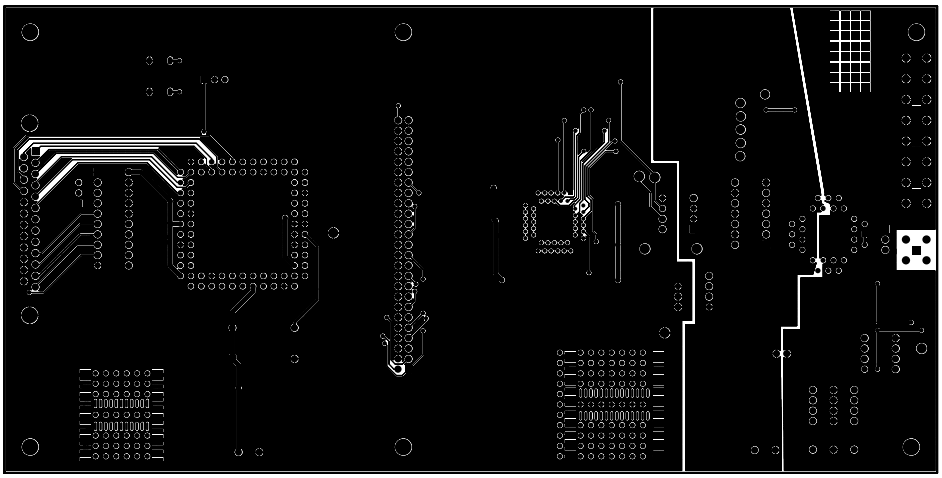


Figure 6. Top layer (not to scale).

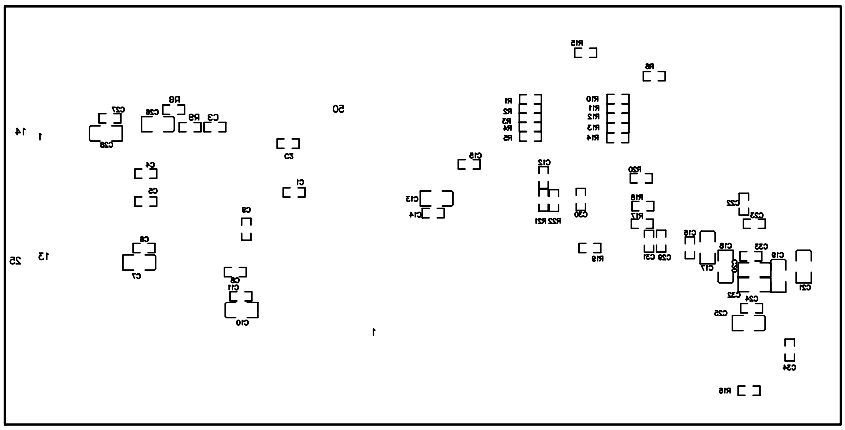


Figure 7. Bottom side silk-screen (not to scale).

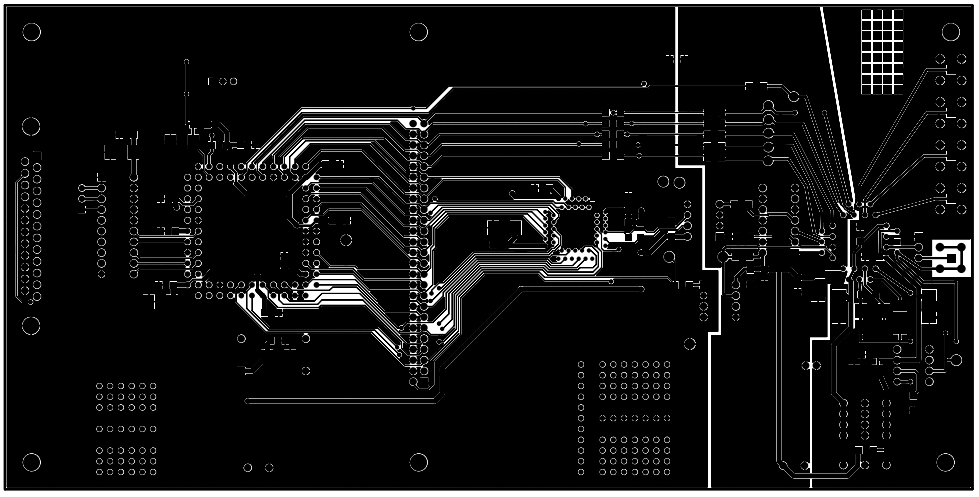


Figure 8. Bottom layer (not to scale).