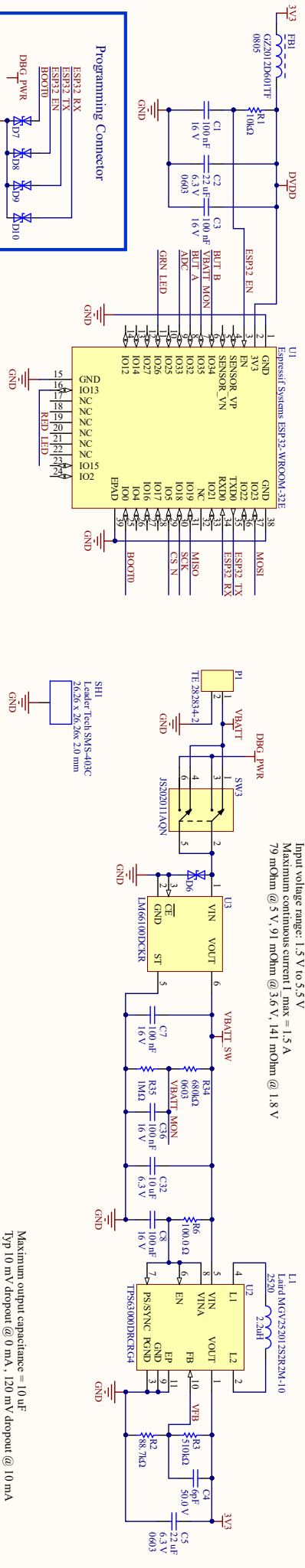


All passive components are 0402 unless specified
Resistor tolerance = 1%, Capacitor tolerance = 10%

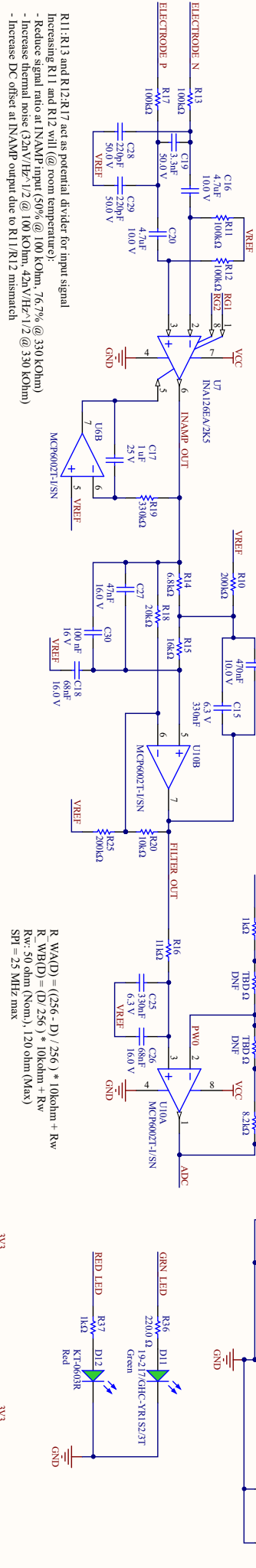


Gain = $5 + 80k / R_G$
 $R_G = 71.5\text{ ohm}$, Gain = 1120
Input High-pass filter $f_c = 0.34\text{ Hz}$
INAAMP High-pass filter $f_c = 0.48\text{ Hz}$
RFL Low-pass filter $f_c = 233\text{ Hz}$
RFL Low-pass filter $f_c = 7.2\text{ kHz}$

Third order Butterworth low-pass filter
 $Q = 2.17$, $f_c = 57.4\text{ Hz}$, $f_n = 50\text{ Hz}$
50 Hz Rejection:
Min = 17 dB, Nom = 35 dB, Max = 55 dB

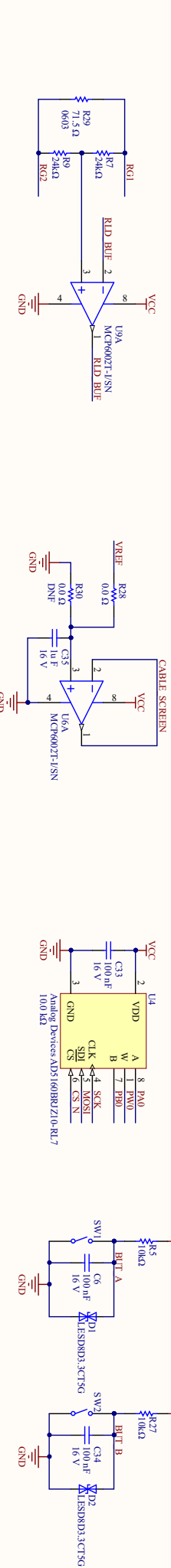
Gain = $1.745 - 19.2$ where DigPot D = 0 - 255
Feedback low-pass $f_c = 1.29\text{ kHz}$ - 5.8 kHz
Input low-pass $f_c = 36.35\text{ Hz}$

Maximum output capacitance = 10 uF
Typ 10 mV dropout @ 0 mA, 120 mV dropout @ 10 mA



R11: R13 and R12: R17 act as potential divider for input signal
Increasing R11 and R12 will (@ room temperature):
- Reduce signal ratio at INAAMP input (50% @ 100 Kohm, 76.7% @ 330 Kohm)
- Increase thermal noise (32nV/Hz^{1/2} @ 100 Kohm, 42nV/Hz^{1/2} @ 330 Kohm)
- Increase DC offset at INAAMP output due to R11/R12 mismatch

$R_{WA(D)} = ((256 - D) / 256) * 10\text{kohm} + R_w$
 $R_{WB(D)} = (D / 256) * 10\text{kohm} + R_w$
 R_w : 50 ohm (Nom), 120 ohm (Max)
 $SPL = 25\text{ MHz max}$



Title			Revision		
Size	A3		Number	Sheet of	
Date:	19/05/2021		Drawn By:	D	
File:	main.schDoc		Drawn By:	D	