```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     2 ************************************************************************
                                                     3 *
                                                     4 *        Zvector E6 instruction tests for VRX encoded:
                                                     5 *
                                                     6 *        E601 VLEBRH  - VECTOR LOAD BYTE REVERSED ELEMENT (16)
                                                     7 *        E602 VLEBRG  - VECTOR LOAD BYTE REVERSED ELEMENT (64)
                                                     8 *        E603 VLEBRF  - VECTOR LOAD BYTE REVERSED ELEMENT (32)
                                                     9 *        E604 VLLEBRZ - VECTOR LOAD BYTE REVERSED ELEMENT AND ZERO
                                                    10 *        E605 VLBRREP - VECTOR LOAD BYTE REVERSED ELEMENT AND REPLICATE
                                                    11 *        E606 VLBR    - VECTOR LOAD BYTE REVERSED ELEMENTS
                                                    12 *        E607 VLER    - VECTOR LOAD ELEMENTS REVERSED
                                                    13 *
                                                    14 *        James Wekel June 2024
                                                    15 ************************************************************************


                                                    17 ************************************************************************
                                                    18 *
                                                    19 *        basic instruction tests
                                                    20 *
                                                    21 ************************************************************************
                                                    22 *  This program tests proper functioning of the z/arch E6 VRX vector
                                                    23 *  load instructions. Exceptions are not tested.
                                                    24 *
                                                    25 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    26 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    27 *  NOT designed to test all aspects of any of the instructions.
                                                    28 *
                                                    29 ************************************************************************
                                                    30 *
                                                    31 *    *Testcase VECTOR E6 VRX load instructions
                                                    32 *    *
                                                    33 *    *   Zvector E6 instruction tests for VRX encoded:
                                                    34 *    *
                                                    35 *    *   E601 VLEBRH  - VECTOR LOAD BYTE REVERSED ELEMENT (16)
                                                    36 *    *   E602 VLEBRG  - VECTOR LOAD BYTE REVERSED ELEMENT (64)
                                                    37 *    *   E603 VLEBRF  - VECTOR LOAD BYTE REVERSED ELEMENT (32)
                                                    38 *    *   E604 VLLEBRZ - VECTOR LOAD BYTE REVERSED ELEMENT AND ZERO
                                                    39 *    *   E605 VLBRREP - VECTOR LOAD BYTE REVERSED ELEMENT AND REPLICATE
                                                    40 *    *   E606 VLBR    - VECTOR LOAD BYTE REVERSED ELEMENTS
                                                    41 *    *   E607 VLER    - VECTOR LOAD ELEMENTS REVERSED
                                                    42 *    *
                                                    43 *    *   # ---------------------------------------------------------
                                                    44 *    *   #  This tests only the basic function of the instruction.
                                                    45 *    *   #  Exceptions are NOT tested.
                                                    46 *    *   # ---------------------------------------------------------
                                                    47 *    *
                                                    48 *    mainsize    2
                                                    49 *    numcpu      1
                                                    50 *    sysclear
                                                    51 *    archlvl     z/Arch
                                                    52 *
                                                    53 *    loadcore    "$(testpath)/zvector-e6-01-loads.core" 0x0
                                                    54 *
                                                    55 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                    56 *    runtest     2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     57 *    diag8cmd    disable   # (reset back to default)
                                                     58 *
                                                     59 *    *Done
                                                     60 *
                                                     61 ********************************************************************************


                                00000000  00001693    63 ZVE6TST  START 0
00000000                        00000000              64          USING ZVE6TST,R0            Low core addressability
                                                      65
                                00000140  00000000    66 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                        00000000  000001A0    68          ORG   ZVE6TST+X'1A0'       z/Architecure RESTART PSW
000001A0  00000001 80000000                           69          DC    X'0000000180000000'
000001A8  00000000 00000200                           70          DC    AD(BEGIN)

000001B0                        000001B0  000001D0    72          ORG   ZVE6TST+X'1D0'       z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                           73          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                           74          DC    AD(X'DEAD')


000001E0                        000001E0  00000200    76          ORG   ZVE6TST+X'200'       Start of actual test program...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                      78
                                                      79 ************************************************************************
                                                      80 *               The actual "ZVE6TST" program itself...
                                                      81 ************************************************************************
                                                      82 *
                                                      83 *  Architecture Mode: z/Arch
                                                      84 *  Register Usage:
                                                      85 *
                                                      86 *   R0       (work)
                                                      87 *   R1-4     (work)
                                                      88 *   R5       Testing control table - current test base
                                                      89 *   R6-R7    (work)
                                                      90 *   R8       First base register
                                                      91 *   R9       Second base register
                                                      92 *   R10      E6TESTS register
                                                      93 *   R11      E6TEST call return
                                                      94 *   R12-R13  (work)
                                                      95 *   R14      Subroutine call
                                                      96 *   R15      Secondary Subroutine call or work
                                                      97 *
                                                      98 ************************************************************************

00000200                        00000200             100          USING  BEGIN,R8        FIRST Base Register
00000200                        00001200             101          USING  BEGIN+4096,R9   SECOND Base Register

00000200  0580                                       103 BEGIN    BALR  R8,0             Initalize FIRST base register
00000202  0680                                       104          BCTR  R8,0             Initalize FIRST base register
00000204  0680                                       105          BCTR  R8,0             Initalize FIRST base register

00000206  4190 8800                  00000800        107          LA    R9,2048(,R8)     Initalize SECOND base register
0000020A  4190 9800                  00000800        108          LA    R9,2048(,R9)     Initalize SECOND base register
                                                     109
0000020E  B600 81D4                  000003D4        110          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
00000212  9604 81D5                  000003D5        111          OI    CTLR0+1,X'04'    Turn on AFP bit
00000216  9602 81D5                  000003D5        112          OI    CTLR0+1,X'02'    Turn on Vector bit
0000021A  B700 81D4                  000003D4        113          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                     114
                                                     115 *
0000021E  41A0 9414                  00001614        116          LA    R10,E6TESTS       get table of test addresses
                                                     117
                                00000222  00000001   118 NEXTE6   EQU   *
00000222  5850 A000                  00000000        119          L     R5,0(0,R10)       get test address
00000226  1255                                       120          LTR   R5,R5                have a test?
00000228  4780 8064                  00000264        121          BZ    ENDTEST                 done?
                                                     122
0000022C                        00000000             123          USING E6TEST,R5
0000022C  E710 8EA0 0006             000010A0        124          VL    V1,V1FUDGE        pollute V1
00000232  58B0 5000                  00000000        125          L     R11,TSUB          get address of test routine
00000236  05BB                                       126          BALR  R11,R11           do test
00000238  E710 8E80 000E             00001080        127          VST   V1,V1SAVED        save test vector
0000023E  D50F 8E80 5014  00001080   00000014        128          CLC   V1SAVED,RESULT    valid?
00000244  4770 8050                  00000250        129          BNE   FAILMSG              no, issue failed message
                                                     130
00000248  41A0 A004                  00000004        131          LA    R10,4(0,R10)      next test address
0000024C  47F0 8022                  00000222        132          B     NEXTE6
                                                     133
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    134 *
                                                    135 * test failed: issue message with test number, instruction under test
                                                    136 *               and instruction m3
                                                    137 *
                                 00000250  00000001 138 FAILMSG  EQU   *
00000250  45F0 8072                        00000272 139           BAL   R15,RPTERROR
00000254  5800 81DC                        000003DC 140           L     R0,=F'1'          set failed test indicator
00000258  5000 8E00                        00001000 141           ST    R0,FAILED
                                                    142
0000025C  41A0 A004                        00000004 143           LA    R10,4(0,R10)      next test address
00000260  47F0 8022                        00000222 144           B     NEXTE6
                                                    145
                                 00000264  00000001 146 ENDTEST  EQU   *
00000264  5810 8E00                        00001000 147           L     R1,FAILED         did a test fail?
00000268  1211                                      148           LTR   R1,R1
0000026A  4780 81B8                        000003B8 149           BZ    EOJ                  No, exit
0000026E  47F0 81D0                        000003D0 150           B     FAILTEST             Yes, exit with BAD PSW
                                                    151
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    153 ********************************************************************************
                                                    154 *        RPTERROR                  Report instruction test in error
                                                    155 ********************************************************************************

00000272  50F0 80D4                      000002D4   157 RPTERROR ST    R15,RPTSAVE          Save return address
00000276  5050 80D8                      000002D8   158          ST    R5,RPTSVR5           Save R5
                                                    159 *
0000027A  4820 5004                      00000004   160          LH    R2,TNUM              get test number and convert
0000027E  4E20 8E6E                      0000106E   161          CVD   R2,DECNUM
00000282  D211 8E58 8E42       00001058  00001042   162          MVC   PRT3,EDIT
00000288  DE11 8E58 8E6E       00001058  0000106E   163          ED    PRT3,DECNUM
0000028E  D202 8E14 8E65       00001014  00001065   164          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    165
00000294  D207 8E2F 5008       0000102F  00000008   166          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    167 *
0000029A  E320 5007 0076                 00000007   168          LB    R2,M3                get m3 and convert
000002A0  4E20 8E6E                      0000106E   169          CVD   R2,DECNUM
000002A4  D211 8E58 8E42       00001058  00001042   170          MVC   PRT3,EDIT
000002AA  DE11 8E58 8E6E       00001058  0000106E   171          ED    PRT3,DECNUM
000002B0  D200 8E40 8E67       00001040  00001067   172          MVC   PRTM3(1),PRT3+15     fill in message with m3 field

                                                    174 *
                                                    175 *        Use Hercules Diagnose for Message to console
                                                    176 *
000002B6  9002 80E0                      000002E0   177          STM   R0,R2,RPTDWSAV       save regs used by MSG
000002BA  4100 003E                      0000003E   178          LA    R0,PRTLNG            message length
000002BE  4110 8E04                      00001004   179          LA    R1,PRTLINE             messagfe address
000002C2  4520 80F0                      000002F0   180          BAL   R2,MSG               call Hercules console MSG display
000002C6  9802 80E0                      000002E0   181          LM    R0,R2,RPTDWSAV       restore regs


000002CA  5850 80D8                      000002D8   183          L     R5,RPTSVR5           Restore R5
000002CE  58F0 80D4                      000002D4   184          L     R15,RPTSAVE          Restore return address
000002D2  07FF                                      185          BR    R15                  Return to caller

000002D4  00000000                                  187 RPTSAVE  DC    F'0'                 R15 save area
000002D8  00000000                                  188 RPTSVR5  DC    F'0'                 R5 save area

000002E0  00000000 00000000                         190 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    192 ************************************************************************
                                                    193 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    194 *              R2 = return address
                                                    195 ************************************************************************
000002F0  4900 81E0                  000003E0       197 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000002F4  07D2                                      198          BNHR  R2                      No, ignore

000002F6  9002 8128                  00000328       200          STM   R0,R2,MSGSAVE           Save registers

000002FA  4900 81E2                  000003E2       202          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000002FE  47D0 8106                  00000306       203          BNH   MSGOK                   Yes, continue
00000302  4100 005F                  0000005F       204          LA    R0,L'MSGMSG             No, set to maximum

00000306  1820                                      206 MSGOK    LR    R2,R0                   Copy length to work register
00000308  0620                                      207          BCTR  R2,0                    Minus-1 for execute
0000030A  4420 8134                  00000334       208          EX    R2,MSGMVC               Copy message to O/P buffer

0000030E  4120 200A                  0000000A       210          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
00000312  4110 813A                  0000033A       211          LA    R1,MSGCMD               Point to true command

00000316  83120008                                  213          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
0000031A  4780 8120                  00000320       214          BZ    MSGRET                  Return if successful
0000031E  0000                                      215          DC    H'0'                    CRASH for debugging purposes

00000320  9802 8128                  00000328       217 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
00000324  07F2                                      218          BR    R2                      Return to caller



00000328  00000000 00000000                         220 MSGSAVE  DC    3F'0'                   Registers save area
00000334  D200 8143 1000      00000343  00000000    221 MSGMVC   MVC   MSGMSG(0),0(R1)         Executed instruction


0000033A  D4E2C7D5 D6C8405C                         223 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
00000343  40404040 40404040                         224 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    225
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     227 ********************************************************************************
                                                     228 *        Normal completion or Abnormal termination PSWs
                                                     229 ********************************************************************************

000003A8  00020001 80000000                          231 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
000003B8  B2B2 81A8                  000003A8        233 EOJ      LPSWE EOJPSW                Normal completion

000003C0  00020001 80000000                          235 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
000003D0  B2B2 81C0                  000003C0        237 FAILTEST LPSWE FAILPSW               Abnormal termination

                                                     239 ********************************************************************************
                                                     240 *        Working Storage
                                                     241 ********************************************************************************

000003D4  00000000                                   243 CTLR0    DS    F                     CR0
000003D8  00000000                                   244          DS    F

000003DC                                             246          LTORG ,                     Literals pool
000003DC  00000001                                   247                =F'1'
000003E0  0000                                       248                =H'0'
000003E2  005F                                       249                =AL2(L'MSGMSG)
                                                     250
                                                     251 *        some constants
                                                     252
                         00000400  00000001          253 K        EQU   1024                One KB
                         00001000  00000001          254 PAGE     EQU   (4*K)               Size of one page
                         00010000  00000001          255 K64      EQU   (64*K)              64 KB
                         00100000  00000001          256 MB       EQU   (K*K)                1 MB
                                                     257
                         AABBCCDD  00000001          258 REG2PATT EQU   X'AABBCCDD'      Polluted Register pattern
                         000000DD  00000001          259 REG2LOW  EQU         X'DD'      (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    261 *=========================================================================
                                                    262 *
                                                    263 *  NOTE: start data on an address that is easy to display
                                                    264 *        within Hercules
                                                    265 *
                                                    266 *=========================================================================
                                                    267
000003E4                      000003E4  00001000    268          ORG   ZVE6TST+X'1000'
00001000  00000000                                  269 FAILED   DC    F'0'                      some test failed?


                                                    271 *
                                                    272 *        failed message and associated editting
                                                    273 *
00001004  40404040 40404040                         274 PRTLINE  DC    C'         Test # '
00001014  A7A7A7                                    275 PRTNUM   DC    C'xxx'
00001017  40868189 93858440                         276          DC    c' failed for instruction '
0000102F  A7A7A7A7 A7A7A7A7                         277 PRTNAME  DC    CL8'xxxxxxxx'
00001037  40A689A3 884094F3                         278          DC    C' with m3='
00001040  A7                                        279 PRTM3    DC    C'x'
00001041  4B                                        280          DC    C'.'
                              0000003E  00000001    281 PRTLNG   EQU   *-PRTLINE
00001042  40212020 20202020                        282 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                    283
00001054  7E7E7E6E                                  284          DC    C'===>'
00001058  40404040 40404040                         285 PRT3     DC    CL18' '
0000106A  4C7E7E7E                                  286          DC    C'<===='
0000106E  00000000 00000000                         287 DECNUM   DS    CL16


                                                    289 *
                                                    290 *        Vector instruction results, pollution and input
                                                    291 *
00001080                                            292          DS    0F
00001080  00000000 00000000                         293 V1SAVED  DS    XL16                                          V1 OUTPUT
00001090  00000000 00000000                         294          DS    XL16                                             gap
000010A0  FFFFFFFF FFFFFFFF                         295 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010B0  00010203 04050607                         296 V1INPUT  DC    XL16'000102030405060708090101112131415'    V1 input
000010C0  00000000 00000000                         297          DS    XL16                                             gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     299 ********************************************************************************
                                                     300 *        E6TEST DSECT
                                                     301 ********************************************************************************


                                                     303 E6TEST   DSECT ,
00000000  00000000                                   304 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       305 TNUM     DC    H'00'          Test Number
00000006  00                                         306          DC    X'00'
00000007  00                                         307 M3       DC    X'00'          M3 used
                                                     308
00000008  40404040 40404040                          309 OPNAME   DC    CL8' '         E6 name
00000010  00000000                                   310 RELEN    DC    A(0)           RESULT LENGTH
00000014  00000000                                   311 RESULT   DC    A(0)
                                                     312 *        EXPECTED RESULT
                                                     313 **
                                                     314 *        test routine will be here (from VRX macro)


                          00000000  00001693         316 ZVE6TST  CSECT ,
000010D0                                             317          DS    0F


                                                     319 ********************************************************************************
                                                     320 *     Macros to help build test tables
                                                     321 ********************************************************************************


                                                     323 *
                                                     324 * macro to generate individual test
                                                     325 *
                                                     326          MACRO
                                                     327          VRX   &INST,&M3,&RESULT
                                                     328 .*                                &INST    - VRX instruction under test
                                                     329 .*                                &M3      - m3 field
                                                     330 .*                                &RESULT  - XL16 result field
                                                     331          GBLA  &TNUM
                                                     332 &TNUM    SETA  &TNUM+1
                                                     333
                                                     334          DS    0FD
                                                     335          USING *,R5               base for test data and test routine
                                                     336
                                                     337 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                     338          DC    H'&TNUM'           test number
                                                     339          DC    X'00'
                                                     340          DC    X'&M3'             M3
                                                     341          DC    CL8'&INST'         instruction name
                                                     342          DC    A(X&TNUM-RE&TNUM)   result length
                                                     343 RE&TNUM  DC    &RESULT            expected result
                                                     344 .*
                                                     345 *
                                                     346 X&TNUM   DS    0F
                                                     347          &INST V1,V1INPUT,&M3     test instruction
                                                     348          BR    R11                return
                                                     349
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      350          DROP  R5
                                                      351 .*
                                                      352          MEND


                                                      354 *
                                                      355 * macro to generate table of pointers to individual tests
                                                      356 *
                                                      357          MACRO
                                                      358          PTTABLE
                                                      359          GBLA  &TNUM
                                                      360          LCLA  &CUR
                                                      361 &CUR     SETA  1
                                                      362 .*
                                                      363 TTABLE   DS    0F
                                                      364 .LOOP    ANOP
                                                      365 .*
                                                      366          DC    A(T&CUR)          TEST &CUR
                                                      367 .*
                                                      368 &CUR     SETA  &CUR+1
                                                      369          AIF   (&CUR LE &TNUM).LOOP
                                                      370 *
                                                      371          DC    A(0)              END OF TABLE
                                                      372          DC    A(0)
                                                      373 .*
                                                      374          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     376 ************************************************************************
                                                     377 *        E6 VRX load tests
                                                     378 ************************************************************************
                                                     379          PRINT DATA
                                                     380 *        E601 VLEBRH  - VECTOR LOAD BYTE REVERSED ELEMENT (16)
                                                     381 *        E602 VLEBRG  - VECTOR LOAD BYTE REVERSED ELEMENT (64)
                                                     382 *        E603 VLEBRF  - VECTOR LOAD BYTE REVERSED ELEMENT (32)
                                                     383 *        E604 VLLEBRZ - VECTOR LOAD BYTE REVERSED ELEMENT AND ZERO
                                                     384 *        E605 VLBRREP - VECTOR LOAD BYTE REVERSED ELEMENT AND REPLICATE
                                                     385 *        E606 VLBR    - VECTOR LOAD BYTE REVERSED ELEMENTS
                                                     386 *        E607 VLER    - VECTOR LOAD ELEMENTS REVERSED
                                                     387
                                                     388 *        VRX   instruction, m3, 16 byte expected result
                                                     389          VRX   VLEBRH,0,XL16'0100FFFFFFFFFFFFFFFFFFFFFFFF'
000010D0                                             390+         DS    0FD
000010D0                          000010D0           391+         USING *,R5             base for test data and test routine
000010D0  000010F4                                   392+T1       DC    A(X1)            address of test routine
000010D4  0001                                       393+         DC    H'1'             test number
000010D6  00                                         394+         DC    X'00'
000010D7  00                                         395+         DC    X'0'             M3
000010D8  E5D3C5C2 D9C84040                          396+         DC    CL8'VLEBRH'      instruction name
000010E0  00000010                                   397+         DC    A(X1-RE1)         result length
                                                     398+RE1      DC    XL16'0100FFFFFFFFFFFFFFFFFFFFFFFF' \
000010E4  0100FFFF FFFFFFFF                             +                               expected result
000010EC  FFFFFFFF FFFFFFFF
                                                     399+*
000010F4                                             400+X1       DS    0F
000010F4  E610 8EB0 0001                  000010B0   401+         VLEBRH V1,V1INPUT,0    test instruction
000010FA  07FB                                       402+         BR    R11              return
000010FC                                             403+         DROP  R5
                                                     404          VRX   VLEBRH,1,XL16'FFFF0100FFFFFFFFFFFFFFFFFFFF'
00001100                                             405+         DS    0FD
00001100                          00001100           406+         USING *,R5             base for test data and test routine
00001100  00001124                                   407+T2       DC    A(X2)            address of test routine
00001104  0002                                       408+         DC    H'2'             test number
00001106  00                                         409+         DC    X'00'
00001107  01                                         410+         DC    X'1'             M3
00001108  E5D3C5C2 D9C84040                          411+         DC    CL8'VLEBRH'      instruction name
00001110  00000010                                   412+         DC    A(X2-RE2)         result length
                                                     413+RE2      DC    XL16'FFFF0100FFFFFFFFFFFFFFFFFFFF' \
00001114  FFFF0100 FFFFFFFF                             +                               expected result
0000111C  FFFFFFFF FFFFFFFF
                                                     414+*
00001124                                             415+X2       DS    0F
00001124  E610 8EB0 1001                  000010B0   416+         VLEBRH V1,V1INPUT,1    test instruction
0000112A  07FB                                       417+         BR    R11              return
0000112C                                             418+         DROP  R5
                                                     419          VRX   VLEBRH,2,XL16'FFFFFFFF0100FFFFFFFFFFFFFFFF'
00001130                                             420+         DS    0FD
00001130                          00001130           421+         USING *,R5             base for test data and test routine
00001130  00001154                                   422+T3       DC    A(X3)            address of test routine
00001134  0003                                       423+         DC    H'3'             test number
00001136  00                                         424+         DC    X'00'
00001137  02                                         425+         DC    X'2'             M3
00001138  E5D3C5C2 D9C84040                          426+         DC    CL8'VLEBRH'      instruction name
00001140  00000010                                   427+         DC    A(X3-RE3)         result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   428+RE3      DC    XL16'FFFFFFFF0100FFFFFFFFFFFFFFFFFFFF' \
00001144  FFFFFFFF 0100FFFF                           +                                 expected result
0000114C  FFFFFFFF FFFFFFFF
                                                   429+*
00001154                                           430+X3       DS    0F
00001154  E610 8EB0 2001                 000010B0  431+         VLEBRH V1,V1INPUT,2     test instruction
0000115A  07FB                                     432+         BR    R11               return
0000115C                                           433+         DROP  R5
                                                   434          VRX   VLEBRH,3,XL16'FFFFFFFFFFFF0100FFFFFFFFFFFFFFFF'
00001160                                           435+         DS    0FD
00001160                 00001160                  436+         USING *,R5              base for test data and test routine
00001160  00001184                                 437+T4       DC    A(X4)             address of test routine
00001164  0004                                     438+         DC    H'4'              test number
00001166  00                                       439+         DC    X'00'
00001167  03                                       440+         DC    X'3'              M3
00001168  E5D3C5C2 D9C84040                        441+         DC    CL8'VLEBRH'       instruction name
00001170  00000010                                 442+         DC    A(X4-RE4)          result length
                                                   443+RE4      DC    XL16'FFFFFFFFFFFF0100FFFFFFFFFFFFFFFF' \
00001174  FFFFFFFF FFFF0100                           +                                 expected result
0000117C  FFFFFFFF FFFFFFFF
                                                   444+*
00001184                                           445+X4       DS    0F
00001184  E610 8EB0 3001                 000010B0  446+         VLEBRH V1,V1INPUT,3     test instruction
0000118A  07FB                                     447+         BR    R11               return
0000118C                                           448+         DROP  R5
                                                   449          VRX   VLEBRH,4,XL16'FFFFFFFFFFFFFFFF0100FFFFFFFFFFFF'
00001190                                           450+         DS    0FD
00001190                 00001190                  451+         USING *,R5              base for test data and test routine
00001190  000011B4                                 452+T5       DC    A(X5)             address of test routine
00001194  0005                                     453+         DC    H'5'              test number
00001196  00                                       454+         DC    X'00'
00001197  04                                       455+         DC    X'4'              M3
00001198  E5D3C5C2 D9C84040                        456+         DC    CL8'VLEBRH'       instruction name
000011A0  00000010                                 457+         DC    A(X5-RE5)          result length
                                                   458+RE5      DC    XL16'FFFFFFFFFFFFFFFF0100FFFFFFFFFFFF' \
000011A4  FFFFFFFF FFFFFFFF                           +                                 expected result
000011AC  0100FFFF FFFFFFFF
                                                   459+*
000011B4                                           460+X5       DS    0F
000011B4  E610 8EB0 4001                 000010B0  461+         VLEBRH V1,V1INPUT,4     test instruction
000011BA  07FB                                     462+         BR    R11               return
000011BC                                           463+         DROP  R5
                                                   464          VRX   VLEBRH,5,XL16'FFFFFFFFFFFFFFFFFFFF0100FFFFFFFF'
000011C0                                           465+         DS    0FD
000011C0                 000011C0                  466+         USING *,R5              base for test data and test routine
000011C0  000011E4                                 467+T6       DC    A(X6)             address of test routine
000011C4  0006                                     468+         DC    H'6'              test number
000011C6  00                                       469+         DC    X'00'
000011C7  05                                       470+         DC    X'5'              M3
000011C8  E5D3C5C2 D9C84040                        471+         DC    CL8'VLEBRH'       instruction name
000011D0  00000010                                 472+         DC    A(X6-RE6)          result length
                                                   473+RE6      DC    XL16'FFFFFFFFFFFFFFFFFFFF0100FFFFFFFF' \
000011D4  FFFFFFFF FFFFFFFF                           +                                 expected result
000011DC  FFFF0100 FFFFFFFF
                                                   474+*
000011E4                                           475+X6       DS    0F
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000011E4  E610 8EB0 5001                 000010B0   476+         VLEBRH V1,V1INPUT,5     test instruction
000011EA  07FB                                      477+         BR    R11               return
000011EC                                            478+         DROP  R5
                                                    479          VRX   VLEBRH,6,XL16'FFFFFFFFFFFFFFFFFFFFFFFF0100FFFF'
000011F0                                            480+         DS    0FD
000011F0                          000011F0          481+         USING *,R5              base for test data and test routine
000011F0  00001214                                  482+T7       DC    A(X7)             address of test routine
000011F4  0007                                      483+         DC    H'7'              test number
000011F6  00                                        484+         DC    X'00'
000011F7  06                                        485+         DC    X'6'              M3
000011F8  E5D3C5C2 D9C84040                         486+         DC    CL8'VLEBRH'       instruction name
00001200  00000010                                  487+         DC    A(X7-RE7)          result length
                                                    488+RE7      DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFF0100FFFF' \
00001204  FFFFFFFF FFFFFFFF                            +                                  expected result
0000120C  FFFFFFFF 0100FFFF
                                                    489+*
00001214                                            490+X7       DS    0F
00001214  E610 8EB0 6001                 000010B0   491+         VLEBRH V1,V1INPUT,6     test instruction
0000121A  07FB                                      492+         BR    R11               return
0000121C                                            493+         DROP  R5
                                                    494          VRX   VLEBRH,7,XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFF0100'
00001220                                            495+         DS    0FD
00001220                          00001220          496+         USING *,R5              base for test data and test routine
00001220  00001244                                  497+T8       DC    A(X8)             address of test routine
00001224  0008                                      498+         DC    H'8'              test number
00001226  00                                        499+         DC    X'00'
00001227  07                                        500+         DC    X'7'              M3
00001228  E5D3C5C2 D9C84040                         501+         DC    CL8'VLEBRH'       instruction name
00001230  00000010                                  502+         DC    A(X8-RE8)          result length
                                                    503+RE8      DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFF0100' \
00001234  FFFFFFFF FFFFFFFF                            +                                  expected result
0000123C  FFFFFFFF FFFF0100
                                                    504+*
00001244                                            505+X8       DS    0F
00001244  E610 8EB0 7001                 000010B0   506+         VLEBRH V1,V1INPUT,7     test instruction
0000124A  07FB                                      507+         BR    R11               return
0000124C                                            508+         DROP  R5
                                                    509 *
                                                    510          VRX   VLEBRG,0,XL16'07060504030201000FFFFFFFFFFFFFFFF'
00001250                                            511+         DS    0FD
00001250                          00001250          512+         USING *,R5              base for test data and test routine
00001250  00001274                                  513+T9       DC    A(X9)             address of test routine
00001254  0009                                      514+         DC    H'9'              test number
00001256  00                                        515+         DC    X'00'
00001257  00                                        516+         DC    X'0'              M3
00001258  E5D3C5C2 D9C74040                         517+         DC    CL8'VLEBRG'       instruction name
00001260  00000010                                  518+         DC    A(X9-RE9)          result length
                                                    519+RE9      DC    XL16'07060504030201000FFFFFFFFFFFFFFFF' \
00001264  07060504 03020100                            +                                  expected result
0000126C  FFFFFFFF FFFFFFFF
                                                    520+*
00001274                                            521+X9       DS    0F
00001274  E610 8EB0 0002                 000010B0   522+         VLEBRG V1,V1INPUT,0     test instruction
0000127A  07FB                                      523+         BR    R11               return
0000127C                                            524+         DROP  R5
                                                    525          VRX   VLEBRG,1,XL16'FFFFFFFFFFFFFFFF07060504030201000'
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001280                                           526+         DS    0FD
00001280                      00001280             527+         USING *,R5              base for test data and test routine
00001280  000012A4                                 528+T10      DC    A(X10)            address of test routine
00001284  000A                                     529+         DC    H'10'             test number
00001286  00                                       530+         DC    X'00'
00001287  01                                       531+         DC    X'1'              M3
00001288  E5D3C5C2 D9C74040                        532+         DC    CL8'VLEBRG'       instruction name
00001290  00000010                                 533+         DC    A(X10-RE10)        result length
                                                   534+RE10     DC    XL16'FFFFFFFFFFFFFFFF070605040302010' \
00001294  FFFFFFFF FFFFFFFF                          +                                  expected result
0000129C  07060504 03020100
                                                   535+*
000012A4                                           536+X10      DS    0F
000012A4  E610 8EB0 1002                 000010B0  537+         VLEBRG V1,V1INPUT,1     test instruction
000012AA  07FB                                     538+         BR    R11               return
000012AC                                           539+         DROP  R5
                                                   540 *
                                                   541          VRX   VLEBRF,0,XL16'03020100FFFFFFFFFFFFFFFFFFFFFFFF'
000012B0                                           542+         DS    0FD
000012B0                      000012B0             543+         USING *,R5              base for test data and test routine
000012B0  000012D4                                 544+T11      DC    A(X11)            address of test routine
000012B4  000B                                     545+         DC    H'11'             test number
000012B6  00                                       546+         DC    X'00'
000012B7  00                                       547+         DC    X'0'              M3
000012B8  E5D3C5C2 D9C64040                        548+         DC    CL8'VLEBRF'       instruction name
000012C0  00000010                                 549+         DC    A(X11-RE11)        result length
                                                   550+RE11     DC    XL16'03020100FFFFFFFFFFFFFFFFFFFFFFFF' \
000012C4  03020100 FFFFFFFF                          +                                  expected result
000012CC  FFFFFFFF FFFFFFFF
                                                   551+*
000012D4                                           552+X11      DS    0F
000012D4  E610 8EB0 0003                 000010B0  553+         VLEBRF V1,V1INPUT,0     test instruction
000012DA  07FB                                     554+         BR    R11               return
000012DC                                           555+         DROP  R5
                                                   556          VRX   VLEBRF,1,XL16'FFFFFFFF03020100FFFFFFFFFFFFFFFF'
000012E0                                           557+         DS    0FD
000012E0                      000012E0             558+         USING *,R5              base for test data and test routine
000012E0  00001304                                 559+T12      DC    A(X12)            address of test routine
000012E4  000C                                     560+         DC    H'12'             test number
000012E6  00                                       561+         DC    X'00'
000012E7  01                                       562+         DC    X'1'              M3
000012E8  E5D3C5C2 D9C64040                        563+         DC    CL8'VLEBRF'       instruction name
000012F0  00000010                                 564+         DC    A(X12-RE12)        result length
                                                   565+RE12     DC    XL16'FFFFFFFF03020100FFFFFFFFFFFFFFFF' \
000012F4  FFFFFFFF 03020100                          +                                  expected result
000012FC  FFFFFFFF FFFFFFFF
                                                   566+*
00001304                                           567+X12      DS    0F
00001304  E610 8EB0 1003                 000010B0  568+         VLEBRF V1,V1INPUT,1     test instruction
0000130A  07FB                                     569+         BR    R11               return
0000130C                                           570+         DROP  R5
                                                   571          VRX   VLEBRF,2,XL16'FFFFFFFFFFFFFFFF03020100FFFFFFFF'
00001310                                           572+         DS    0FD
00001310                      00001310             573+         USING *,R5              base for test data and test routine
00001310  00001334                                 574+T13      DC    A(X13)            address of test routine
00001314  000D                                     575+         DC    H'13'             test number
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001316  00                                       576+          DC    X'00'
00001317  02                                       577+          DC    X'2'              M3
00001318  E5D3C5C2 D9C64040                         578+          DC    CL8'VLEBRF'       instruction name
00001320  00000010                                 579+          DC    A(X13-RE13)        result length
                                                   580+RE13      DC    XL16'FFFFFFFFFFFFFFFF03020100FFFFFFFF' \
00001324  FFFFFFFF FFFFFFFF                           +                                     expected result
0000132C  03020100 FFFFFFFF
                                                   581+*
00001334                                           582+X13       DS    0F
00001334  E610 8EB0 2003                 000010B0  583+          VLEBRF V1,V1INPUT,2     test instruction
0000133A  07FB                                     584+          BR    R11               return
0000133C                                           585+          DROP  R5
                                                   586           VRX   VLEBRF,3,XL16'FFFFFFFFFFFFFFFFFFFFFFFF03020100'
00001340                                           587+          DS    0FD
00001340                 00001340                  588+          USING *,R5              base for test data and test routine
00001340  00001364                                 589+T14       DC    A(X14)            address of test routine
00001344  000E                                     590+          DC    H'14'             test number
00001346  00                                       591+          DC    X'00'
00001347  03                                       592+          DC    X'3'              M3
00001348  E5D3C5C2 D9C64040                         593+          DC    CL8'VLEBRF'       instruction name
00001350  00000010                                 594+          DC    A(X14-RE14)        result length
                                                   595+RE14      DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFF03020100' \
00001354  FFFFFFFF FFFFFFFF                           +                                     expected result
0000135C  FFFFFFFF 03020100
                                                   596+*
00001364                                           597+X14       DS    0F
00001364  E610 8EB0 3003                 000010B0  598+          VLEBRF V1,V1INPUT,3     test instruction
0000136A  07FB                                     599+          BR    R11               return
0000136C                                           600+          DROP  R5
                                                   601 *
                                                   602           VRX   VLLEBRZ,1,XL16'00000000000010000000000000000000'
00001370                                           603+          DS    0FD
00001370                 00001370                  604+          USING *,R5              base for test data and test routine
00001370  00001394                                 605+T15       DC    A(X15)            address of test routine
00001374  000F                                     606+          DC    H'15'             test number
00001376  00                                       607+          DC    X'00'
00001377  01                                       608+          DC    X'1'              M3
00001378  E5D3D3C5 C2D9E940                         609+          DC    CL8'VLLEBRZ'      instruction name
00001380  00000010                                 610+          DC    A(X15-RE15)        result length
                                                   611+RE15      DC    XL16'00000000000010000000000000000000' \
00001384  00000000 00000100                           +                                     expected result
0000138C  00000000 00000000
                                                   612+*
00001394                                           613+X15       DS    0F
00001394  E610 8EB0 1004                 000010B0  614+          VLLEBRZ V1,V1INPUT,1    test instruction
0000139A  07FB                                     615+          BR    R11               return
0000139C                                           616+          DROP  R5
                                                   617           VRX   VLLEBRZ,2,XL16'00000000302010000000000000000000'
000013A0                                           618+          DS    0FD
000013A0                 000013A0                  619+          USING *,R5              base for test data and test routine
000013A0  000013C4                                 620+T16       DC    A(X16)            address of test routine
000013A4  0010                                     621+          DC    H'16'             test number
000013A6  00                                       622+          DC    X'00'
000013A7  02                                       623+          DC    X'2'              M3
000013A8  E5D3D3C5 C2D9E940                       624+          DC    CL8'VLLEBRZ'      instruction name
000013B0  00000010                                 625+          DC    A(X16-RE16)        result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    626+RE16     DC    XL16'00000000302010000000000000000000' \
000013B4  00000000 03020100                            +                          expected result
000013BC  00000000 00000000
                                                    627+*
000013C4                                            628+X16      DS    0F
000013C4  E610 8EB0 2004                 000010B0   629+         VLLEBRZ V1,V1INPUT,2    test instruction
000013CA  07FB                                      630+         BR    R11               return
000013CC                                            631+         DROP  R5
                                                    632          VRX   VLLEBRZ,3,XL16'07060504030201000000000000000000'
000013D0                                            633+         DS    0FD
000013D0                      000013D0              634+         USING *,R5              base for test data and test routine
000013D0  000013F4                                  635+T17      DC    A(X17)            address of test routine
000013D4  0011                                      636+         DC    H'17'             test number
000013D6  00                                        637+         DC    X'00'
000013D7  03                                        638+         DC    X'3'              M3
000013D8  E5D3D3C5 C2D9E940                         639+         DC    CL8'VLLEBRZ'      instruction name
000013E0  00000010                                  640+         DC    A(X17-RE17)        result length
                                                    641+RE17     DC    XL16'07060504030201000000000000000000' \
000013E4  07060504 03020100                            +                          expected result
000013EC  00000000 00000000
                                                    642+*
000013F4                                            643+X17      DS    0F
000013F4  E610 8EB0 3004                 000010B0   644+         VLLEBRZ V1,V1INPUT,3    test instruction
000013FA  07FB                                      645+         BR    R11               return
000013FC                                            646+         DROP  R5
                                                    647          VRX   VLLEBRZ,6,XL16'03020100000000000000000000000000'
00001400                                            648+         DS    0FD
00001400                      00001400              649+         USING *,R5              base for test data and test routine
00001400  00001424                                  650+T18      DC    A(X18)            address of test routine
00001404  0012                                      651+         DC    H'18'             test number
00001406  00                                        652+         DC    X'00'
00001407  06                                        653+         DC    X'6'              M3
00001408  E5D3D3C5 C2D9E940                         654+         DC    CL8'VLLEBRZ'      instruction name
00001410  00000010                                  655+         DC    A(X18-RE18)        result length
                                                    656+RE18     DC    XL16'03020100000000000000000000000000' \
00001414  03020100 00000000                            +                          expected result
0000141C  00000000 00000000
                                                    657+*
00001424                                            658+X18      DS    0F
00001424  E610 8EB0 6004                 000010B0   659+         VLLEBRZ V1,V1INPUT,6    test instruction
0000142A  07FB                                      660+         BR    R11               return
0000142C                                            661+         DROP  R5
                                                    662 *
                                                    663          VRX   VLBRREP,1,XL16'01000100010001000100010001000100'
00001430                                            664+         DS    0FD
00001430                      00001430              665+         USING *,R5              base for test data and test routine
00001430  00001454                                  666+T19      DC    A(X19)            address of test routine
00001434  0013                                      667+         DC    H'19'             test number
00001436  00                                        668+         DC    X'00'
00001437  01                                        669+         DC    X'1'              M3
00001438  E5D3C2D9 D9C5D740                         670+         DC    CL8'VLBRREP'      instruction name
00001440  00000010                                  671+         DC    A(X19-RE19)        result length
                                                    672+RE19     DC    XL16'01000100010001000100010001000100' \
00001444  01000100 01000100                            +                          expected result
0000144C  01000100 01000100
                                                    673+*
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00001454                                          674+X19      DS    0F
00001454  E610 8EB0 1005                000010B0  675+         VLBRREP V1,V1INPUT,1    test instruction
0000145A  07FB                                    676+         BR    R11               return
0000145C                                          677+         DROP  R5
                                                  678          VRX   VLBRREP,2,XL16'0302010003020100030201000302010003020100'
00001460                                          679+         DS    0FD
00001460                  00001460                680+         USING *,R5              base for test data and test routine
00001460  00001484                                681+T20      DC    A(X20)            address of test routine
00001464  0014                                    682+         DC    H'20'             test number
00001466  00                                      683+         DC    X'00'
00001467  02                                      684+         DC    X'2'              M3
00001468  E5D3C2D9 D9C5D740                       685+         DC    CL8'VLBRREP'      instruction name
00001470  00000010                                686+         DC    A(X20-RE20)        result length
                                                  687+RE20     DC    XL16'0302010003020100030201000302010003020100' \
00001474  03020100 03020100                        +                                   expected result
0000147C  03020100 03020100
                                                  688+*
00001484                                          689+X20      DS    0F
00001484  E610 8EB0 2005                000010B0  690+         VLBRREP V1,V1INPUT,2    test instruction
0000148A  07FB                                    691+         BR    R11               return
0000148C                                          692+         DROP  R5
                                                  693          VRX   VLBRREP,3,XL16'0706050403020100070605040302010007060504030201000706050403020100'
00001490                                          694+         DS    0FD
00001490                  00001490                695+         USING *,R5              base for test data and test routine
00001490  000014B4                                696+T21      DC    A(X21)            address of test routine
00001494  0015                                    697+         DC    H'21'             test number
00001496  00                                      698+         DC    X'00'
00001497  03                                      699+         DC    X'3'              M3
00001498  E5D3C2D9 D9C5D740                       700+         DC    CL8'VLBRREP'      instruction name
000014A0  00000010                                701+         DC    A(X21-RE21)        result length
                                                  702+RE21     DC    XL16'0706050403020100070605040302010007060504030201000706050403020100' \
000014A4  07060504 03020100                       +                                   expected result
000014AC  07060504 03020100
                                                  703+*
000014B4                                          704+X21      DS    0F
000014B4  E610 8EB0 3005                000010B0  705+         VLBRREP V1,V1INPUT,3    test instruction
000014BA  07FB                                    706+         BR    R11               return
000014BC                                          707+         DROP  R5
                                                  708 *
                                                  709          VRX   VLBR,1,XL16'0100030205040706090811101312151400'
000014C0                                          710+         DS    0FD
000014C0                  000014C0                711+         USING *,R5              base for test data and test routine
000014C0  000014E4                                712+T22      DC    A(X22)            address of test routine
000014C4  0016                                    713+         DC    H'22'             test number
000014C6  00                                      714+         DC    X'00'
000014C7  01                                      715+         DC    X'1'              M3
000014C8  E5D3C2D9 40404040                       716+         DC    CL8'VLBR'         instruction name
000014D0  00000010                                717+         DC    A(X22-RE22)        result length
                                                  718+RE22     DC    XL16'0100030205040706090811101312151400' \
000014D4  01000302 05040706                       +                                   expected result
000014DC  09081110 13121514
                                                  719+*
000014E4                                          720+X22      DS    0F
000014E4  E610 8EB0 1006                000010B0  721+         VLBR  V1,V1INPUT,1      test instruction
000014EA  07FB                                    722+         BR    R11               return
000014EC                                          723+         DROP  R5
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     724          VRX   VLBR,2,XL16'0302010007060504111009081514131 2'
000014F0                                             725+         DS    0FD
000014F0                       000014F0              726+         USING *,R5             base for test data and test routine
000014F0  00001514                                   727+T23      DC    A(X23)           address of test routine
000014F4  0017                                       728+         DC    H'23'            test number
000014F6  00                                         729+         DC    X'00'
000014F7  02                                         730+         DC    X'2'             M3
000014F8  E5D3C2D9 40404040                          731+         DC    CL8'VLBR'        instruction name
00001500  00000010                                   732+         DC    A(X23-RE23)       result length
                                                     733+RE23     DC    XL16'0302010007060504111009081514131 2' \
00001504  03020100 07060504                             +                               expected result
0000150C  11100908 15141312
                                                     734+*
00001514                                             735+X23      DS    0F
00001514  E610 8EB0 2006                 000010B0    736+         VLBR  V1,V1INPUT,2     test instruction
0000151A  07FB                                       737+         BR    R11              return
0000151C                                             738+         DROP  R5
                                                     739          VRX   VLBR,3,XL16'0706050403020100151413121110090 '
00001520                                             740+         DS    0FD
00001520                       00001520              741+         USING *,R5             base for test data and test routine
00001520  00001544                                   742+T24      DC    A(X24)           address of test routine
00001524  0018                                       743+         DC    H'24'            test number
00001526  00                                         744+         DC    X'00'
00001527  03                                         745+         DC    X'3'             M3
00001528  E5D3C2D9 40404040                          746+         DC    CL8'VLBR'        instruction name
00001530  00000010                                   747+         DC    A(X24-RE24)       result length
                                                     748+RE24     DC    XL16'0706050403020100151413121110090 ' \
00001534  07060504 03020100                             +                               expected result
0000153C  15141312 11100908
                                                     749+*
00001544                                             750+X24      DS    0F
00001544  E610 8EB0 3006                 000010B0    751+         VLBR  V1,V1INPUT,3     test instruction
0000154A  07FB                                       752+         BR    R11              return
0000154C                                             753+         DROP  R5
                                                     754          VRX   VLBR,4,XL16'1514131211100908070605040302 100'
00001550                                             755+         DS    0FD
00001550                       00001550              756+         USING *,R5             base for test data and test routine
00001550  00001574                                   757+T25      DC    A(X25)           address of test routine
00001554  0019                                       758+         DC    H'25'            test number
00001556  00                                         759+         DC    X'00'
00001557  04                                         760+         DC    X'4'             M3
00001558  E5D3C2D9 40404040                          761+         DC    CL8'VLBR'        instruction name
00001560  00000010                                   762+         DC    A(X25-RE25)       result length
                                                     763+RE25     DC    XL16'1514131211100908070605040302 100' \
00001564  15141312 11100908                             +                               expected result
0000156C  07060504 03020100
                                                     764+*
00001574                                             765+X25      DS    0F
00001574  E610 8EB0 4006                 000010B0    766+         VLBR  V1,V1INPUT,4     test instruction
0000157A  07FB                                       767+         BR    R11              return
0000157C                                             768+         DROP  R5
                                                     769 *
                                                     770          VRX   VLER,1,XL16'1415121310110809060704050203 001'
00001580                                             771+         DS    0FD
00001580                       00001580              772+         USING *,R5             base for test data and test routine
00001580  000015A4                                   773+T26      DC    A(X26)           address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001584  001A                                     774+          DC    H'26'             test number
00001586  00                                       775+          DC    X'00'
00001587  01                                       776+          DC    X'1'              M3
00001588  E5D3C5D9 40404040                         777+          DC    CL8'VLER'         instruction name
00001590  00000010                                 778+          DC    A(X26-RE26)        result length
                                                   779+RE26      DC    XL16'14151213101108090607040502030001' \
00001594  14151213 10110809                          +                                   expected result
0000159C  06070405 02030001
                                                   780+*
000015A4                                           781+X26       DS    0F
000015A4  E610 8EB0 1007                 000010B0  782+          VLER  V1,V1INPUT,1      test instruction
000015AA  07FB                                     783+          BR    R11               return
000015AC                                           784+          DROP  R5
                                                   785           VRX   VLER,2,XL16'12131415080910110405060700010203'
000015B0                                           786+          DS    0FD
000015B0                 000015B0                  787+          USING *,R5              base for test data and test routine
000015B0  000015D4                                 788+T27       DC    A(X27)            address of test routine
000015B4  001B                                     789+          DC    H'27'             test number
000015B6  00                                       790+          DC    X'00'
000015B7  02                                       791+          DC    X'2'              M3
000015B8  E5D3C5D9 40404040                        792+          DC    CL8'VLER'         instruction name
000015C0  00000010                                 793+          DC    A(X27-RE27)        result length
                                                   794+RE27      DC    XL16'12131415080910110405060700010203' \
000015C4  12131415 08091011                        795+                                  expected result
000015CC  04050607 00010203
                                                   795+*
000015D4                                           796+X27       DS    0F
000015D4  E610 8EB0 2007                 000010B0  797+          VLER  V1,V1INPUT,2      test instruction
000015DA  07FB                                     798+          BR    R11               return
000015DC                                           799+          DROP  R5
                                                   800           VRX   VLER,3,XL16'08091011121314150001020304050607'
000015E0                                           801+          DS    0FD
000015E0                 000015E0                  802+          USING *,R5              base for test data and test routine
000015E0  00001604                                 803+T28       DC    A(X28)            address of test routine
000015E4  001C                                     804+          DC    H'28'             test number
000015E6  00                                       805+          DC    X'00'
000015E7  03                                       806+          DC    X'3'              M3
000015E8  E5D3C5D9 40404040                        807+          DC    CL8'VLER'         instruction name
000015F0  00000010                                 808+          DC    A(X28-RE28)        result length
                                                   809+RE28      DC    XL16'08091011121314150001020304050607' \
000015F4  08091011 12131415                        810+                                  expected result
000015FC  00010203 04050607
                                                   810+*
00001604                                           811+X28       DS    0F
00001604  E610 8EB0 3007                 000010B0  812+          VLER  V1,V1INPUT,3      test instruction
0000160A  07FB                                     813+          BR    R11               return
0000160C                                           814+          DROP  R5
                                                   815
0000160C  00000000                                 816           DC    F'0'     END OF TABLE
00001610  00000000                                 817           DC    F'0'
                                                   818 *
                                                   819 * table of pointers to individual load test
                                                   820 *
00001614                                           821 E6TESTS   DS    0F
                                                   822           PTTABLE
00001614                                           823+TTABLE    DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001614  000010D0                          824+         DC    A(T1)             TEST &CUR
00001618  00001100                          825+         DC    A(T2)             TEST &CUR
0000161C  00001130                          826+         DC    A(T3)             TEST &CUR
00001620  00001160                          827+         DC    A(T4)             TEST &CUR
00001624  00001190                          828+         DC    A(T5)             TEST &CUR
00001628  000011C0                          829+         DC    A(T6)             TEST &CUR
0000162C  000011F0                          830+         DC    A(T7)             TEST &CUR
00001630  00001220                          831+         DC    A(T8)             TEST &CUR
00001634  00001250                          832+         DC    A(T9)             TEST &CUR
00001638  00001280                          833+         DC    A(T10)            TEST &CUR
0000163C  000012B0                          834+         DC    A(T11)            TEST &CUR
00001640  000012E0                          835+         DC    A(T12)            TEST &CUR
00001644  00001310                          836+         DC    A(T13)            TEST &CUR
00001648  00001340                          837+         DC    A(T14)            TEST &CUR
0000164C  00001370                          838+         DC    A(T15)            TEST &CUR
00001650  000013A0                          839+         DC    A(T16)            TEST &CUR
00001654  000013D0                          840+         DC    A(T17)            TEST &CUR
00001658  00001400                          841+         DC    A(T18)            TEST &CUR
0000165C  00001430                          842+         DC    A(T19)            TEST &CUR
00001660  00001460                          843+         DC    A(T20)            TEST &CUR
00001664  00001490                          844+         DC    A(T21)            TEST &CUR
00001668  000014C0                          845+         DC    A(T22)            TEST &CUR
0000166C  000014F0                          846+         DC    A(T23)            TEST &CUR
00001670  00001520                          847+         DC    A(T24)            TEST &CUR
00001674  00001550                          848+         DC    A(T25)            TEST &CUR
00001678  00001580                          849+         DC    A(T26)            TEST &CUR
0000167C  000015B0                          850+         DC    A(T27)            TEST &CUR
00001680  000015E0                          851+         DC    A(T28)            TEST &CUR
                                            852+*
00001684  00000000                          853+         DC    A(0)              END OF TABLE
00001688  00000000                          854+         DC    A(0)
                                            855
0000168C  00000000                          856          DC    F'0'      END OF TABLE
00001690  00000000                          857          DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                          859 ********************************************************************************
                                          860 *        Register equates
                                          861 ********************************************************************************

                            00000000  00000001   863 R0       EQU   0
                            00000001  00000001   864 R1       EQU   1
                            00000002  00000001   865 R2       EQU   2
                            00000003  00000001   866 R3       EQU   3
                            00000004  00000001   867 R4       EQU   4
                            00000005  00000001   868 R5       EQU   5
                            00000006  00000001   869 R6       EQU   6
                            00000007  00000001   870 R7       EQU   7
                            00000008  00000001   871 R8       EQU   8
                            00000009  00000001   872 R9       EQU   9
                            0000000A  00000001   873 R10      EQU   10
                            0000000B  00000001   874 R11      EQU   11
                            0000000C  00000001   875 R12      EQU   12
                            0000000D  00000001   876 R13      EQU   13
                            0000000E  00000001   877 R14      EQU   14
                            0000000F  00000001   878 R15      EQU   15
```

```
                                          880 ********************************************************************************
                                          881 *        Register equates
                                          882 ********************************************************************************

                            00000000  00000001   884 V0       EQU   0
                            00000001  00000001   885 V1       EQU   1
                            00000002  00000001   886 V2       EQU   2
                            00000003  00000001   887 V3       EQU   3
                            00000004  00000001   888 V4       EQU   4
                            00000005  00000001   889 V5       EQU   5
                            00000006  00000001   890 V6       EQU   6
                            00000007  00000001   891 V7       EQU   7
                            00000008  00000001   892 V8       EQU   8
                            00000009  00000001   893 V9       EQU   9
                            0000000A  00000001   894 V10      EQU   10
                            0000000B  00000001   895 V11      EQU   11
                            0000000C  00000001   896 V12      EQU   12
                            0000000D  00000001   897 V13      EQU   13
                            0000000E  00000001   898 V14      EQU   14
                            0000000F  00000001   899 V15      EQU   15
                            00000010  00000001   900 V16      EQU   16
                            00000011  00000001   901 V17      EQU   17
                            00000012  00000001   902 V18      EQU   18
                            00000013  00000001   903 V19      EQU   19
                            00000014  00000001   904 V20      EQU   20
                            00000015  00000001   905 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001   906 V22      EQU   22
                                00000017  00000001   907 V23      EQU   23
                                00000018  00000001   908 V24      EQU   24
                                00000019  00000001   909 V25      EQU   25
                                0000001A  00000001   910 V26      EQU   26
                                0000001B  00000001   911 V27      EQU   27
                                0000001C  00000001   912 V28      EQU   28
                                0000001D  00000001   913 V29      EQU   29
                                0000001E  00000001   914 V30      EQU   30
                                0000001F  00000001   915 V31      EQU   31
                                                     916
                                                     917          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	103	70 100 101
CTLR0	F	000003D4	4	243	110 111 112 113
DECNUM	C	0000106E	16	287	161 163 169 171
E6TEST	4	00000000	24	303	123
E6TESTS	F	00001614	4	821	116
EDIT	X	00001042	18	282	162 170
ENDTEST	U	00000264	1	146	121
EOJ	I	000003B8	4	233	149
EOJPSW	D	000003A8	8	231	233
FAILED	F	00001000	4	269	141 147
FAILMSG	U	00000250	1	138	129
FAILPSW	D	000003C0	8	235	237
FAILTEST	I	000003D0	4	237	150
IMAGE	1	00000000	5780	0	
K	U	00000400	1	253	254 255 256
K64	U	00010000	1	255	
M3	X	00000007	1	307	168
MB	U	00100000	1	256	
MSG	I	000002F0	4	197	180
MSGCMD	C	0000033A	9	223	210 211
MSGMSG	C	00000343	95	224	204 221 202
MSGMVC	I	00000334	6	221	208
MSGOK	I	00000306	2	206	203
MSGRET	I	00000320	4	217	214
MSGSAVE	F	00000328	4	220	200 217
NEXTE6	U	00000222	1	118	132 144
OPNAME	C	00000008	8	309	166
PAGE	U	00001000	1	254	
PRT3	C	00001058	18	285	162 163 164 170 171 172
PRTLINE	C	00001004	16	274	281 179
PRTLNG	U	0000003E	1	281	178
PRTM3	C	00001040	1	279	172
PRTNAME	C	0000102F	8	277	166
PRTNUM	C	00001014	3	275	164
R0	U	00000000	1	863	64 110 113 140 141 177 178 181 197 200 202 204 206 217
R1	U	00000001	1	864	147 148 179 211 221
R10	U	0000000A	1	873	116 119 131 143
R11	U	0000000B	1	874	125 126 402 417 432 447 462 477 492 507 523 538 554 569 584 599 615 630 645 660 676 691 706 722 737 752 767 783 798 813
R12	U	0000000C	1	875	
R13	U	0000000D	1	876	
R14	U	0000000E	1	877	
R15	U	0000000F	1	878	139 157 184 185
R2	U	00000002	1	865	160 161 168 169 177 180 181 198 200 206 207 208 210 217 218
R3	U	00000003	1	866	
R4	U	00000004	1	867	
R5	U	00000005	1	868	119 120 123 158 183 391 403 406 418 421 433 436 448 451 463 466 478 481 493 496 508 512 524 527 539 543 555 558 570 573 585 588 600 604 616 619 631 634 646 649 661 665 677 680 692 695 707 711 723 726 738 741 753 756 768 772 784 787 799 802 814
R6	U	00000006	1	869	
R7	U	00000007	1	870	
R8	U	00000008	1	871	100 103 104 105 107
R9	U	00000009	1	872	101 107 108
RE1	X	000010E4	16	398	397

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE10	X	00001294	16	534	533
RE11	X	000012C4	16	550	549
RE12	X	000012F4	16	565	564
RE13	X	00001324	16	580	579
RE14	X	00001354	16	595	594
RE15	X	00001384	16	611	610
RE16	X	000013B4	16	626	625
RE17	X	000013E4	16	641	640
RE18	X	00001414	16	656	655
RE19	X	00001444	16	672	671
RE2	X	00001114	16	413	412
RE20	X	00001474	16	687	686
RE21	X	000014A4	16	702	701
RE22	X	000014D4	16	718	717
RE23	X	00001504	16	733	732
RE24	X	00001534	16	748	747
RE25	X	00001564	16	763	762
RE26	X	00001594	16	779	778
RE27	X	000015C4	16	794	793
RE28	X	000015F4	16	809	808
RE3	X	00001144	16	428	427
RE4	X	00001174	16	443	442
RE5	X	000011A4	16	458	457
RE6	X	000011D4	16	473	472
RE7	X	00001204	16	488	487
RE8	X	00001234	16	503	502
RE9	X	00001264	16	519	518
REG2LOW	U	000000DD	1	259	
REG2PATT	U	AABBCCDD	1	258	
RELEN	A	00000010	4	310	
RESULT	A	00000014	4	311	128
RPTDWSAV	D	000002E0	8	190	177 181
RPTERROR	I	00000272	4	157	139
RPTSAVE	F	000002D4	4	187	157 184
RPTSVR5	F	000002D8	4	188	158 183
SVOLDPSW	U	00000140	0	66	
T1	A	000010D0	4	392	824
T10	A	00001280	4	528	833
T11	A	000012B0	4	544	834
T12	A	000012E0	4	559	835
T13	A	00001310	4	574	836
T14	A	00001340	4	589	837
T15	A	00001370	4	605	838
T16	A	000013A0	4	620	839
T17	A	000013D0	4	635	840
T18	A	00001400	4	650	841
T19	A	00001430	4	666	842
T2	A	00001100	4	407	825
T20	A	00001460	4	681	843
T21	A	00001490	4	696	844
T22	A	000014C0	4	712	845
T23	A	000014F0	4	727	846
T24	A	00001520	4	742	847
T25	A	00001550	4	757	848
T26	A	00001580	4	773	849
T27	A	000015B0	4	788	850

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T28	A	000015E0	4	803	851
T3	A	00001130	4	422	826
T4	A	00001160	4	437	827
T5	A	00001190	4	452	828
T6	A	000011C0	4	467	829
T7	A	000011F0	4	482	830
T8	A	00001220	4	497	831
T9	A	00001250	4	513	832
TNUM	H	00000004	2	305	160
TSUB	A	00000000	4	304	125
TTABLE	F	00001614	4	823	
V0	U	00000000	1	884	
V1	U	00000001	1	885	124 127 401 416 431 446 461 476 491 506 522 537 553 568 583 598 614 629 644 659 675 690 705 721 736 751 766 782 797 812
V10	U	0000000A	1	894	
V11	U	0000000B	1	895	
V12	U	0000000C	1	896	
V13	U	0000000D	1	897	
V14	U	0000000E	1	898	
V15	U	0000000F	1	899	
V16	U	00000010	1	900	
V17	U	00000011	1	901	
V18	U	00000012	1	902	
V19	U	00000013	1	903	
V1FUDGE	X	000010A0	16	295	124
V1INPUT	X	000010B0	16	296	401 416 431 446 461 476 491 506 522 537 553 568 583 598 614 629 644 659 675 690 705 721 736 751 766 782 797 812
V1SAVED	X	00001080	16	293	127 128
V2	U	00000002	1	886	
V20	U	00000014	1	904	
V21	U	00000015	1	905	
V22	U	00000016	1	906	
V23	U	00000017	1	907	
V24	U	00000018	1	908	
V25	U	00000019	1	909	
V26	U	0000001A	1	910	
V27	U	0000001B	1	911	
V28	U	0000001C	1	912	
V29	U	0000001D	1	913	
V3	U	00000003	1	887	
V30	U	0000001E	1	914	
V31	U	0000001F	1	915	
V4	U	00000004	1	888	
V5	U	00000005	1	889	
V6	U	00000006	1	890	
V7	U	00000007	1	891	
V8	U	00000008	1	892	
V9	U	00000009	1	893	
X1	F	000010F4	4	400	392 397
X10	F	000012A4	4	536	528 533
X11	F	000012D4	4	552	544 549
X12	F	00001304	4	567	559 564
X13	F	00001334	4	582	574 579
X14	F	00001364	4	597	589 594
X15	F	00001394	4	613	605 610
X16	F	000013C4	4	628	620 625

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X17	F	000013F4	4	643	635 640
X18	F	00001424	4	658	650 655
X19	F	00001454	4	674	666 671
X2	F	00001124	4	415	407 412
X20	F	00001484	4	689	681 686
X21	F	000014B4	4	704	696 701
X22	F	000014E4	4	720	712 717
X23	F	00001514	4	735	727 732
X24	F	00001544	4	750	742 747
X25	F	00001574	4	765	757 762
X26	F	000015A4	4	781	773 778
X27	F	000015D4	4	796	788 793
X28	F	00001604	4	811	803 808
X3	F	00001154	4	430	422 427
X4	F	00001184	4	445	437 442
X5	F	000011B4	4	460	452 457
X6	F	000011E4	4	475	467 472
X7	F	00001214	4	490	482 487
X8	F	00001244	4	505	497 502
X9	F	00001274	4	521	513 518
ZVE6TST	J	00000000	5780	63	66 68 72 76 268 64
=AL2(L'MSGMSG)	R	000003E2	2	249	202
=F'1'	F	000003DC	4	247	140
=H'0'	H	000003E0	2	248	197

```
 MACRO    DEFN   REFERENCES

PTTABLE    358    822
VRX        327    389    404    419    434    449    464    479    494    510    525    541    556    571    586    602    617    632    647    663    678    693
                  709    724    739    754    770    785    800
```

```
   DESC      SYMBOL   SIZE     POS         ADDR

Entry: 0

Image       IMAGE    5780  0000-1693  0000-1693
  Region             5780  0000-1693  0000-1693
    CSECT   ZVE6TST  5780  0000-1693  0000-1693
```

```
   STMT                    FILE NAME
1     /devstor/dev/tests/zvector-e6-01-loads.asm

** NO ERRORS FOUND **
```