```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                        2 ************************************************************************
                                                        3 *
                                                        4 *        Zvector E6 instruction tests for VRI-h encoded:
                                                        5 *
                                                        6 *        E649 VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                        7 *
                                                        8 *        James Wekel June 2024
                                                        9 ************************************************************************
                                                       10
                                                       11 ************************************************************************
                                                       12 *
                                                       13 *        basic instruction tests
                                                       14 *
                                                       15 ************************************************************************
                                                       16 *  This program tests proper functioning of the z/arch E6 VRI-h vector
                                                       17 *  load immediate decimal. Exceptions are not tested.
                                                       18 *
                                                       19 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                       20 *  obvious coding errors.  None of the tests are thorough.  They are
                                                       21 *  NOT designed to test all aspects of any of the instructions.
                                                       22 *
                                                       23 ************************************************************************
                                                       24 *
                                                       25 *    *Testcase zvector-e6-10-VLIP: VECTOR E6 VRI-h VLIP instruction
                                                       26 *    *
                                                       27 *    *   Zvector E6 tests for VRI-h encoded instruction:
                                                       28 *    *
                                                       29 *    *   E649 VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                       30 *    *
                                                       31 *    *   # ---------------------------------------------------
                                                       32 *    *   #  This tests only the basic function of the instruction.
                                                       33 *    *   #  Exceptions are NOT tested.
                                                       34 *    *   # ---------------------------------------------------
                                                       35 *    *
                                                       36 *    mainsize    2
                                                       37 *    numcpu      1
                                                       38 *    sysclear
                                                       39 *    archlvl     z/Arch
                                                       40 *
                                                       41 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                       42 *    loadcore    "zvector-e6-10-VLIP.core" 0x0
                                                       43 *    diag8cmd    disable   # (reset back to default)
                                                       44 *
                                                       45 *    *Done
                                                       46 ************************************************************************


                          00000000  0000141F     48 ZVE6TST  START 0
00000000                  00000000                 49          USING ZVE6TST,R0            Low core addressability
                                                   50
                          00000140  00000000     51 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                  00000000  000001A0     53          ORG   ZVE6TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                      54          DC    X'0000000180000000'
000001A8  00000000 00000200                      55          DC    AD(BEGIN)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000001B0                     000001B0  000001D0    57          ORG   ZVE6TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                        58          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                        59          DC    AD(X'DEAD')

000001E0                     000001E0  00000200    61          ORG   ZVE6TST+X'200'        Start of actual test program...
                                                   62
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     64 ************************************************************************
                                                     65 *               The actual "ZVE6TST" program itself...
                                                     66 ************************************************************************
                                                     67 *
                                                     68 *  Architecture Mode: z/Arch
                                                     69 *  Register Usage:
                                                     70 *
                                                     71 *   R0       (work)
                                                     72 *   R1-4     (work)
                                                     73 *   R5       Testing control table - current test base
                                                     74 *   R6-R7    (work)
                                                     75 *   R8       First base register
                                                     76 *   R9       Second base register
                                                     77 *   R10      Third base register
                                                     78 *   R11      E6TEST call return
                                                     79 *   R12      E6TESTS register
                                                     80 *   R13      (work)
                                                     81 *   R14      Subroutine call
                                                     82 *   R15      Secondary Subroutine call or work
                                                     83 *
                                                     84 ************************************************************************

00000200                          00000200           86          USING  BEGIN,R8        FIRST Base Register
00000200                          00001200           87          USING  BEGIN+4096,R9   SECOND Base Register

00000200  0580                                       89 BEGIN    BALR  R8,0             Initalize FIRST base register
00000202  0680                                       90          BCTR  R8,0             Initalize FIRST base register
00000204  0680                                       91          BCTR  R8,0             Initalize FIRST base register

00000206  4190 8800                      00000800    93          LA    R9,2048(,R8)     Initalize SECOND base register
0000020A  4190 9800                      00000800    94          LA    R9,2048(,R9)     Initalize SECOND base register

0000020E  41A0 9800                      00000800    96          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                      00000800    97          LA    R10,2048(,R10)   Initalize THIRD base register
                                                     98
00000216  B600 81FC                      000003FC    99          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 81FD                      000003FD   100          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 81FD                      000003FD   101          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 81FC                      000003FC   102          LCTL  R0,R0,CTLR0      Reload updated CR0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    104 ********************************************************************************
                                                    105 *               Do tests in the E6TESTS table
                                                    106 ********************************************************************************
                                                    107
00000226  58C0 8204                       00000404 108           L     R12,E6TADR       get table of test addresses
                                                    109
                                0000022A  00000001 110 NEXTE6    EQU   *
0000022A  5850 C000                       00000000 111           L     R5,0(0,R12)       get test address
0000022E  1255                                     112           LTR   R5,R5                have a test?
00000230  4780 80D0                       000002D0 113           BZ    ENDTEST                 done?
                                                    114
00000234                        00000000           115           USING E6TEST,R5
00000234  E710 8EE0 0006                  000010E0 116           VL    V1,V1FUDGEB       fudge output
                                                    117
0000023A  58B0 5000                       00000000 118           L     R11,TSUB          get address of test routine
0000023E  05BB                                     119           BALR  R11,R11           do test
                                                    120
                                00000240  00000001 121 TESTREST EQU   *
00000240  E310 5018 0014                  00000018 122           LGF   R1,READDR         get address of expected result
00000246  D50F 8EB0 1000        000010B0  00000000 123           CLC   V1OUTPUT,0(R1)    valid?
0000024C  4770 8058                       00000258 124           BNE   FAILMSG              no, issue failed message
                                                    125
00000250  41C0 C004                       00000004 126           LA    R12,4(0,R12)      next test address
00000254  47F0 802A                       0000022A 127           B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    129 ************************************************************************
                                                    130 * result not as expected:
                                                    131 *        issue message with test number, instruction under test
                                                    132 *              and instruction l2
                                                    133 ************************************************************************
                                 00000258  00000001 134 FAILMSG  EQU   *
00000258  4820 5004                        00000004 135          LH    R2,TNUM              get test number and convert
0000025C  4E20 8E7E                        0000107E 136          CVD   R2,DECNUM
00000260  D211 8E68 8E52       00001068  00001052 137          MVC   PRT3,EDIT
00000266  DE11 8E68 8E7E       00001068  0000107E 138          ED    PRT3,DECNUM
0000026C  D202 8E14 8E75       00001014  00001075 139          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    140
00000272  D207 8E2F 500A       0000102F  0000000A 141          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    142
00000278  B982 0022                                143          XGR   R2,R2                get i2 as U16
0000027C  4820 5008                        00000008 144          LH    R2,I2
00000280  4E20 8E7E                        0000107E 145          CVD   R2,DECNUM            and convert
00000284  D211 8E68 8E52       00001068  00001052 146          MVC   PRT3,EDIT
0000028A  DE11 8E68 8E7E       00001068  0000107E 147          ED    PRT3,DECNUM
00000290  D204 8E40 8E73       00001040  00001073 148          MVC   PRTI2(5),PRT3+11     fill in message with i2 field
                                                    149
00000296  B982 0022                                150          XGR   R2,R2                get i3 as U8
0000029A  4320 5007                        00000007 151          IC    R2,I3                and convert
0000029E  4E20 8E7E                        0000107E 152          CVD   R2,DECNUM
000002A2  D211 8E68 8E52       00001068  00001052 153          MVC   PRT3,EDIT
000002A8  DE11 8E68 8E7E       00001068  0000107E 154          ED    PRT3,DECNUM
000002AE  D201 8E4F 8E76       0000104F  00001076 155          MVC   PRTI3(2),PRT3+14     fill in message with i3 field
                                                    156
000002B4  4100 004E                        0000004E 157          LA    R0,PRTLNG            message length
000002B8  4110 8E04                        00001004 158          LA    R1,PRTLINE           messagfe address
000002BC  45F0 80DE                        000002DE 159          BAL   R15,RPTERROR


                                                    161 ************************************************************************
                                                    162 * continue after a failed test
                                                    163 ************************************************************************
                                 000002C0  00000001 164 FAILCONT EQU   *
000002C0  5800 8208                        00000408 165          L     R0,=F'1'           set GLOBAL failed test indicator
000002C4  5000 8E00                        00001000 166          ST    R0,FAILED
                                                    167
000002C8  41C0 C004                        00000004 168          LA    R12,4(0,R12)       next test address
000002CC  47F0 802A                        0000022A 169          B     NEXTE6


                                                    171 ************************************************************************
                                                    172 * end of testing; set ending psw
                                                    173 ************************************************************************
                                 000002D0  00000001 174 ENDTEST  EQU   *
000002D0  5810 8E00                        00001000 175          L     R1,FAILED            did a test fail?
000002D4  1211                                     176          LTR   R1,R1
000002D6  4780 81E0                        000003E0 177          BZ    EOJ                     No, exit
000002DA  47F0 81F8                        000003F8 178          B     FAILTEST                Yes, exit with BAD PSW
                                                    179
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    181 ************************************************************************
                                                    182 *        RPTERROR          Report instruction test in error
                                                    183 *                             R0 = MESSGAE LENGTH
                                                    184 *                             R1 = ADDRESS OF MESSAGE
                                                    185 ************************************************************************

000002DE  50F0 80FC                 000002FC   187 RPTERROR ST    R15,RPTSAVE        Save return address
000002E2  5050 8100                 00000300   188          ST    R5,RPTSVR5         Save R5
                                                    189 *
                                                    190 *        Use Hercules Diagnose for Message to console
                                                    191 *
000002E6  9002 8108                 00000308   192          STM   R0,R2,RPTDWSAV     save regs used by MSG
000002EA  4520 8118                 00000318   193          BAL   R2,MSG             call Hercules console MSG display
000002EE  9802 8108                 00000308   194          LM    R0,R2,RPTDWSAV     restore regs


000002F2  5850 8100                 00000300   196          L     R5,RPTSVR5         Restore R5
000002F6  58F0 80FC                 000002FC   197          L     R15,RPTSAVE        Restore return address
000002FA  07FF                                 198          BR    R15                Return to caller

000002FC  00000000                             200 RPTSAVE  DC    F'0'               R15 save area
00000300  00000000                             201 RPTSVR5  DC    F'0'               R5 save area

00000308  00000000 00000000                    203 RPTDWSAV DC    2D'0'              R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    205 ************************************************************************
                                                    206 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    207 *              R2 = return address
                                                    208 ************************************************************************
                                                    209
00000318  4900 820C                 0000040C       210 MSG      CH    R0,=H'0'                Do we even HAVE a message?
0000031C  07D2                                     211          BNHR  R2                      No, ignore
                                                   212
0000031E  9002 8150                 00000350       213          STM   R0,R2,MSGSAVE           Save registers
                                                   214
00000322  4900 820E                 0000040E       215          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
00000326  47D0 812E                 0000032E       216          BNH   MSGOK                   Yes, continue
0000032A  4100 005F                 0000005F       217          LA    R0,L'MSGMSG             No, set to maximum
                                                   218
0000032E  1820                                     219 MSGOK    LR    R2,R0                   Copy length to work register
00000330  0620                                     220          BCTR  R2,0                    Minus-1 for execute
00000332  4420 815C                 0000035C       221          EX    R2,MSGMVC               Copy message to O/P buffer
                                                   222
00000336  4120 200A                 0000000A       223          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
0000033A  4110 8162                 00000362       224          LA    R1,MSGCMD               Point to true command
                                                   225
0000033E  83120008                                 226          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
00000342  4780 8148                 00000348       227          BZ    MSGRET                  Return if successful
00000346  0000                                     228          DC    H'0'                    CRASH for debugging purposes
                                                   229
00000348  9802 8150                 00000350       230 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
0000034C  07F2                                     231          BR    R2                      Return to caller


00000350  00000000 00000000                        233 MSGSAVE  DC    3F'0'                   Registers save area
0000035C  D200 816B 1000      0000036B  00000000   234 MSGMVC   MVC   MSGMSG(0),0(R1)         Executed instruction


00000362  D4E2C7D5 D6C8405C                        236 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
0000036B  40404040 40404040                        237 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                   238
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    240 ************************************************************************
                                                    241 *        Normal completion or Abnormal termination PSWs
                                                    242 ************************************************************************


000003D0  00020001 80000000                         244 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

000003E0  B2B2 81D0                 000003D0        246 EOJ      LPSWE EOJPSW               Normal completion


000003E8  00020001 80000000                         248 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

000003F8  B2B2 81E8                 000003E8        250 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                    252 ************************************************************************
                                                    253 *        Working Storage
                                                    254 ************************************************************************

000003FC  00000000                                  256 CTLR0    DS    F                    CR0
00000400  00000000                                  257          DS    F
                                                    258
00000404  000013E4                                  259 E6TADR   DC    A(E6TESTS)           address of E6 test table


00000408                                            261          LTORG ,                    Literals pool
00000408  00000001                                  262                =F'1'
0000040C  0000                                      263                =H'0'
0000040E  005F                                      264                =AL2(L'MSGMSG)
                                                    265
                                                    266 *        some constants
                                                    267
                    00000400  00000001              268 K        EQU   1024               One KB
                    00001000  00000001              269 PAGE     EQU   (4*K)              Size of one page
                    00010000  00000001              270 K64      EQU   (64*K)             64 KB
                    00100000  00000001              271 MB       EQU   (K*K)               1 MB
                                                    272
                    AABBCCDD  00000001              273 REG2PATT EQU   X'AABBCCDD'      Polluted Register pattern
                    000000DD  00000001              274 REG2LOW  EQU         X'DD'      (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    276 *=====================================================================
                                                    277 *
                                                    278 *  NOTE: start data on an address that is easy to display
                                                    279 *        within Hercules
                                                    280 *
                                                    281 *=====================================================================
                                                    282
00000410                      00000410  00001000    283          ORG   ZVE6TST+X'1000'
00001000  00000000                                  284 FAILED   DC    F'0'                      some test failed?


                                                    286 ************************************************************************
                                                    287 *        TEST failed : result messgae
                                                    288 ************************************************************************
                                                    289 *
                                                    290 *        failed message and associated editting
                                                    291 *
00001004  40404040 40404040                         292 PRTLINE  DC    C'         Test # '
00001014  A7A7A7                                    293 PRTNUM   DC    C'xxx'
00001017  40868189 93858440                         294          DC    C' failed for instruction '
0000102F  A7A7A7A7 A7A7A7A7                         295 PRTNAME  DC    CL8'xxxxxxxx'
00001037  40A689A3 884089F2                         296          DC    C' with i2='
00001040  A7A7A7A7 A7                               297 PRTI2    DC    C'xxxxx'
00001045  6B                                        298          DC    C','
00001046  40A689A3 884089F3                         299          DC    C' with i3='
0000104F  A7A7                                      300 PRTI3    DC    C'xx'
00001051  4B                                        301          DC    C'.'
                                0000004E  00000001  302 PRTLNG   EQU   *-PRTLINE
                                                    303
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    305 ************************************************************************
                                                    306 *        TEST failed : message working storge
                                                    307 ************************************************************************
00001052  40212020 20202020                         308 EDIT     DC    XL18'40212020202020202020202020202020'
                                                    309
00001064  7E7E7E6E                                  310          DC    C'===>'
00001068  40404040 40404040                         311 PRT3     DC    CL18' '
0000107A  4C7E7E7E                                  312          DC    C'<==='
0000107E  00000000 00000000                         313 DECNUM   DS    CL16
                                                    314 *
                                                    315 *        CC extrtaction
                                                    316 *
00001090  00000000 00000000                         317 CCPSW    DS    2F          extract PSW after test (has CC)
00001098  00                                        318 CCFOUND  DS    X           extracted cc


                                                    320 ************************************************************************
                                                    321 *        Vector instruction results, pollution and input
                                                    322 ************************************************************************
000010A0                                            323          DS    0FD
000010A0  00000000 00000000                         324          DS    XL16                                          gap
000010B0  00000000 00000000                         325 V1OUTPUT DS    XL16                                       V1 OUTPUT
000010C0  00000000 00000000                         326          DS    XL16                                          gap
000010D0  FFFFFFFF FFFFFFFF                         327 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010E0  BBBBBBBB BBBBBBBB                         328 V1FUDGEB DC    XL16'BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB'    V1 FUDGE b
000010F0  F1F2F3F4 F5F6F7F8                         329 V1INPUT  DC    CL16'1234567890123456'                    V1 input
00001100  F7F8F9F0 F1F2F3F4                         330          DC    CL14'78901234567890'
0000110E  D9                                        331          DC    X'D9'
0000110F  00000000 00000000                         332          DS    XL16                                          gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     334 ********************************************************************************
                                                     335 *        E6TEST DSECT
                                                     336 ********************************************************************************


                                                     338 E6TEST   DSECT ,
00000000  00000000                                   339 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       340 TNUM     DC    H'00'          Test Number
00000006  00                                         341          DC    XL1'00'
00000007  00                                         342 I3       DC    HL1'00'        I3
00000008  0000                                       343 I2       DC    H'00'          I2 used
                                                     344
0000000A  40404040 40404040                          345 OPNAME   DC    CL8' '         E6 name
                                                     346
00000014  00000000                                   347 RELEN    DC    A(0)           RESULT LENGTH
00000018  00000000                                   348 READDR   DC    A(0)           expected result address
                                                     349
                                                     350 **
                                                     351 *        test routine will be here (from VRS_D macro)
                                                     352 * followed by
                                                     353 *        16-byte EXPECTED RESULT
                                                     354 *        16-byte source
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   356 ************************************************************************
                                                   357 *     Macros to help build test tables
                                                   358 *----------------------------------------------------------------------
                                                   359 *     VRI_H Macro to help build test tables
                                                   360 ************************************************************************
                                                   361          MACRO
                                                   362          VRI_H &INST,&I2,&I3
                                                   363 .*                                  &INST  - VRS-d instruction under test
                                                   364 .*                                  &I2    - 4 decimal immediate (2 bytes)
                                                   365 .*                                  &I3    - bit 0   Sign Control
                                                   366 .*                                         - bit 1-3 Shift Amount
                                                   367 .*
                                                   368 .*
                                                   369          LCLA  &XCC(4)  &CC has mask values for FAILED condition codes
                                                   370 &XCC(1)  SETA  7                   CC != 0
                                                   371 &XCC(2)  SETA  11                  CC != 1
                                                   372 &XCC(3)  SETA  13                  CC != 2
                                                   373 &XCC(4)  SETA  14                  CC != 3
                                                   374
                                                   375          GBLA  &TNUM
                                                   376 &TNUM    SETA  &TNUM+1
                                                   377
                                                   378          DS    0FD
                                                   379          USING *,R5               base for test data and test routine
                                                   380
                                                   381 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                   382          DC    H'&TNUM'           test number
                                                   383          DC    XL1'00'
                                                   384          DC    HL1'&I3'           i3
                                                   385          DC    H'&I2'             i2
                                                   386
                                                   387          DC    CL8'&INST'         instruction name
                                                   388
                                                   389          DC    A(16)              result length
                                                   390 REA&TNUM DC    A(RE&TNUM)         result address
                                                   391 .*
                                                   392 *                                  INSTRUCTION UNDER TEST ROUTINE
                                                   393 X&TNUM   DS    0F
                                                   394          &INST V1,&I2,&I3         test instruction
                                                   395          VST   V1,V1OUTPUT        save
                                                   396
                                                   397          BR    R11                return
                                                   398
                                                   399 RE&TNUM  DC    0F
                                                   400          DROP  R5
                                                   401          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      403 ********************************************************************************
                                                      404 *     PTTABLE Macro to generate table of pointers to individual tests
                                                      405 ********************************************************************************
                                                      406
                                                      407          MACRO
                                                      408          PTTABLE
                                                      409          GBLA  &TNUM
                                                      410          LCLA  &CUR
                                                      411 &CUR     SETA  1
                                                      412 .*
                                                      413 TTABLE   DS    0F
                                                      414 .LOOP    ANOP
                                                      415 .*
                                                      416          DC    A(T&CUR)           address of test
                                                      417 .*
                                                      418 &CUR     SETA  &CUR+1
                                                      419          AIF   (&CUR LE &TNUM).LOOP
                                                      420 *
                                                      421          DC    A(0)               END OF TABLE
                                                      422          DC    A(0)
                                                      423 .*
                                                      424          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     426 ********************************************************************************
                                                     427 *        E6 VRI_H tests
                                                     428 ********************************************************************************
                                00000000  0000141F   429 ZVE6TST  CSECT ,
00001120                                             430          DS    0F


                                                     432          PRINT DATA
                                                     433 *
                                                     434 *        E649 VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                     435 *
                                                     436 *        VRI_H instr, i2, i3
                                                     437 *             followed by
                                                     438 *             v1     - 16 byte expected result
                                                     439
                                                     440 *------------------------------------------------------------------------
                                                     441 * VLIP    - VECTOR LOAD IMMEDIATE DECIMAL
                                                     442 *------------------------------------------------------------------------
                                                     443 * VLIP simple
                                                     444          VRI_H VLIP,22102,2                 i2=x'5656' sc=0, shamt=2
00001120                                             445+         DS    0FD
00001120                                00001120     446+         USING *,R5              base for test data and test routine
00001120  0000113C                                   447+T1       DC    A(X1)             address of test routine
00001124  0001                                       448+         DC    H'1'              test number
00001126  00                                         449+         DC    XL1'00'
00001127  02                                         450+         DC    HL1'2'            i3
00001128  5656                                       451+         DC    H'22102'          i2
0000112A  E5D3C9D7 40404040                          452+         DC    CL8'VLIP'         instruction name
00001134  00000010                                   453+         DC    A(16)             result length
00001138  0000114C                                   454+REA1     DC    A(RE1)            result address
                                                     455+*                                  INSTRUCTION UNDER TEST ROUTINE
0000113C                                             456+X1       DS    0F
0000113C  E610 5656 2049                             457+         VLIP  V1,22102,2        test instruction
00001142  E710 8EB0 000E                 000010B0    458+         VST   V1,V1OUTPUT       save
00001148  07FB                                       459+         BR    R11               return
0000114C                                             460+RE1      DC    0F
0000114C                                             461+         DROP  R5
0000114C  00000000 00000000                          462          DC    XL16'00000000000000000000000000565600C'   V1
00001154  00000000 0565600C
                                                     463
                                                     464          VRI_H VLIP,22102,10                i2=x'5656' sc=1, shamt=2
00001160                                             465+         DS    0FD
00001160                       00001160              466+         USING *,R5              base for test data and test routine
00001160  0000117C                                   467+T2       DC    A(X2)             address of test routine
00001164  0002                                       468+         DC    H'2'              test number
00001166  00                                         469+         DC    XL1'00'
00001167  0A                                         470+         DC    HL1'10'           i3
00001168  5656                                       471+         DC    H'22102'          i2
0000116A  E5D3C9D7 40404040                          472+         DC    CL8'VLIP'         instruction name
00001174  00000010                                   473+         DC    A(16)             result length
00001178  0000118C                                   474+REA2     DC    A(RE2)            result address
                                                     475+*                                  INSTRUCTION UNDER TEST ROUTINE
0000117C                                             476+X2       DS    0F
0000117C  E610 5656 A049                             477+         VLIP  V1,22102,10       test instruction
00001182  E710 8EB0 000E                 000010B0    478+         VST   V1,V1OUTPUT       save
00001188  07FB                                       479+         BR    R11               return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000118C                                            480+RE2      DC    0F
0000118C                                            481+         DROP  R5
0000118C  00000000 00000000                         482          DC    XL16'0000000000000000000000000565600D'   V1
00001194  00000000 0565600D
                                                    483
                                                    484          VRI_H VLIP,22102,7                 i2=x'5656' sc=0, shamt=7
000011A0                                            485+         DS    0FD
000011A0                      000011A0              486+         USING *,R5               base for test data and test routine
000011A0  000011BC                                  487+T3       DC    A(X3)              address of test routine
000011A4  0003                                      488+         DC    H'3'               test number
000011A6  00                                        489+         DC    XL1'00'
000011A7  07                                        490+         DC    HL1'7'             i3
000011A8  5656                                      491+         DC    H'22102'           i2
000011AA  E5D3C9D7 40404040                         492+         DC    CL8'VLIP'          instruction name
000011B4  00000010                                  493+         DC    A(16)              result length
000011B8  000011CC                                  494+REA3     DC    A(RE3)             result address
                                                    495+*                                 INSTRUCTION UNDER TEST ROUTINE
000011BC                                            496+X3       DS    0F
000011BC  E610 5656 7049                            497+         VLIP  V1,22102,7         test instruction
000011C2  E710 8EB0 000E              000010B0      498+         VST   V1,V1OUTPUT        save
000011C8  07FB                                      499+         BR    R11                return
000011CC                                            500+RE3      DC    0F
000011CC                                            501+         DROP  R5
000011CC  00000000 00000000                         502          DC    XL16'0000000000000000000056560000000C'   V1
000011D4  00005656 0000000C
                                                    503
                                                    504          VRI_H VLIP,1,8                     i2=x'0001' sc=1, shamt=0
000011E0                                            505+         DS    0FD
000011E0                      000011E0              506+         USING *,R5               base for test data and test routine
000011E0  000011FC                                  507+T4       DC    A(X4)              address of test routine
000011E4  0004                                      508+         DC    H'4'               test number
000011E6  00                                        509+         DC    XL1'00'
000011E7  08                                        510+         DC    HL1'8'             i3
000011E8  0001                                      511+         DC    H'1'               i2
000011EA  E5D3C9D7 40404040                         512+         DC    CL8'VLIP'          instruction name
000011F4  00000010                                  513+         DC    A(16)              result length
000011F8  0000120C                                  514+REA4     DC    A(RE4)             result address
                                                    515+*                                 INSTRUCTION UNDER TEST ROUTINE
000011FC                                            516+X4       DS    0F
000011FC  E610 0001 8049                            517+         VLIP  V1,1,8             test instruction
00001202  E710 8EB0 000E              000010B0      518+         VST   V1,V1OUTPUT        save
00001208  07FB                                      519+         BR    R11                return
0000120C                                            520+RE4      DC    0F
0000120C                                            521+         DROP  R5
0000120C  00000000 00000000                         522          DC    XL16'0000000000000000000000000000001D'   V1
00001214  00000000 0000001D
                                                    523
                                                    524          VRI_H VLIP,0,8                     i2=x'0001' sc=1, shamt=0
00001220                                            525+         DS    0FD
00001220                      00001220              526+         USING *,R5               base for test data and test routine
00001220  0000123C                                  527+T5       DC    A(X5)              address of test routine
00001224  0005                                      528+         DC    H'5'               test number
00001226  00                                        529+         DC    XL1'00'
00001227  08                                        530+         DC    HL1'8'             i3
00001228  0000                                      531+         DC    H'0'               i2
0000122A  E5D3C9D7 40404040                         532+         DC    CL8'VLIP'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001234  00000010                          533+          DC    A(16)              result length
00001238  0000124C                          534+REA5      DC    A(RE5)             result address
                                            535+*                                  INSTRUCTION UNDER TEST ROUTINE
0000123C                                    536+X5        DS    0F
0000123C  E610 0000 8049                    537+          VLIP  V1,0,8             test instruction
00001242  E710 8EB0 000E              000010B0  538+          VST   V1,V1OUTPUT        save
00001248  07FB                              539+          BR    R11                return
0000124C                                    540+RE5       DC    0F
0000124C                                    541+          DROP  R5
0000124C  00000000 00000000                 542           DC    XL16'0000000000000000000000000000000D'   V1
00001254  00000000 0000000D
                                            543
                                            544           VRI_H VLIP,9,0                    i2=x'0009' sc=0, shamt=0
00001260                                    545+          DS    0FD
00001260                    00001260        546+          USING *,R5               base for test data and test routine
00001260  0000127C                          547+T6        DC    A(X6)              address of test routine
00001264  0006                              548+          DC    H'6'               test number
00001266  00                                549+          DC    XL1'00'
00001267  00                                550+          DC    HL1'0'             i3
00001268  0009                              551+          DC    H'9'               i2
0000126A  E5D3C9D7 40404040                 552+          DC    CL8'VLIP'          instruction name
00001274  00000010                          553+          DC    A(16)              result length
00001278  0000128C                          554+REA6      DC    A(RE6)             result address
                                            555+*                                  INSTRUCTION UNDER TEST ROUTINE
0000127C                                    556+X6        DS    0F
0000127C  E610 0009 0049                    557+          VLIP  V1,9,0             test instruction
00001282  E710 8EB0 000E              000010B0  558+          VST   V1,V1OUTPUT        save
00001288  07FB                              559+          BR    R11                return
0000128C                                    560+RE6       DC    0F
0000128C                                    561+          DROP  R5
0000128C  00000000 00000000                 562           DC    XL16'0000000000000000000000000000009C'   V1
00001294  00000000 0000009C
                                            563
                                            564           VRI_H VLIP,9,1                    i2=x'0009' sc=0, shamt=1
000012A0                                    565+          DS    0FD
000012A0                    000012A0        566+          USING *,R5               base for test data and test routine
000012A0  000012BC                          567+T7        DC    A(X7)              address of test routine
000012A4  0007                              568+          DC    H'7'               test number
000012A6  00                                569+          DC    XL1'00'
000012A7  01                                570+          DC    HL1'1'             i3
000012A8  0009                              571+          DC    H'9'               i2
000012AA  E5D3C9D7 40404040                 572+          DC    CL8'VLIP'          instruction name
000012B4  00000010                          573+          DC    A(16)              result length
000012B8  000012CC                          574+REA7      DC    A(RE7)             result address
                                            575+*                                  INSTRUCTION UNDER TEST ROUTINE
000012BC                                    576+X7        DS    0F
000012BC  E610 0009 1049                    577+          VLIP  V1,9,1             test instruction
000012C2  E710 8EB0 000E              000010B0  578+          VST   V1,V1OUTPUT        save
000012C8  07FB                              579+          BR    R11                return
000012CC                                    580+RE7       DC    0F
000012CC                                    581+          DROP  R5
000012CC  00000000 00000000                 582           DC    XL16'0000000000000000000000000000090C'   V1
000012D4  00000000 0000090C
                                            583
                                            584           VRI_H VLIP,4660,0                 i2=x'1234' sc=0, shamt=0
000012E0                                    585+          DS    0FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000012E0                     000012E0              586+         USING *,R5              base for test data and test routine
000012E0  000012FC                                 587+T8       DC    A(X8)             address of test routine
000012E4  0008                                     588+         DC    H'8'              test number
000012E6  00                                       589+         DC    XL1'00'
000012E7  00                                       590+         DC    HL1'0'            i3
000012E8  1234                                     591+         DC    H'4660'           i2
000012EA  E5D3C9D7 40404040                        592+         DC    CL8'VLIP'         instruction name
000012F4  00000010                                 593+         DC    A(16)             result length
000012F8  0000130C                                 594+REA8     DC    A(RE8)            result address
                                                   595+*                                INSTRUCTION UNDER TEST ROUTINE
000012FC                                           596+X8       DS    0F
000012FC  E610 1234 0049                           597+         VLIP  V1,4660,0         test instruction
00001302  E710 8EB0 000E               000010B0    598+         VST   V1,V1OUTPUT       save
00001308  07FB                                     599+         BR    R11               return
0000130C                                           600+RE8      DC    0F
0000130C                                           601+         DROP  R5
0000130C  00000000 00000000                        602          DC    XL16'00000000000000000000000001234C'   V1
00001314  00000000 0001234C
                                                   603
                                                   604          VRI_H VLIP,4660,1                 i2=x'1234' sc=0, shamt=1
00001320                                           605+         DS    0FD
00001320                     00001320              606+         USING *,R5              base for test data and test routine
00001320  0000133C                                 607+T9       DC    A(X9)             address of test routine
00001324  0009                                     608+         DC    H'9'              test number
00001326  00                                       609+         DC    XL1'00'
00001327  01                                       610+         DC    HL1'1'            i3
00001328  1234                                     611+         DC    H'4660'           i2
0000132A  E5D3C9D7 40404040                        612+         DC    CL8'VLIP'         instruction name
00001334  00000010                                 613+         DC    A(16)             result length
00001338  0000134C                                 614+REA9     DC    A(RE9)            result address
                                                   615+*                                INSTRUCTION UNDER TEST ROUTINE
0000133C                                           616+X9       DS    0F
0000133C  E610 1234 1049                           617+         VLIP  V1,4660,1         test instruction
00001342  E710 8EB0 000E               000010B0    618+         VST   V1,V1OUTPUT       save
00001348  07FB                                     619+         BR    R11               return
0000134C                                           620+RE9      DC    0F
0000134C                                           621+         DROP  R5
0000134C  00000000 00000000                        622          DC    XL16'00000000000000000000000012340C'   V1
00001354  00000000 0012340C
                                                   623
                                                   624          VRI_H VLIP,4660,2                 i2=x'1234' sc=0, shamt=2
00001360                                           625+         DS    0FD
00001360                     00001360              626+         USING *,R5              base for test data and test routine
00001360  0000137C                                 627+T10      DC    A(X10)            address of test routine
00001364  000A                                     628+         DC    H'10'             test number
00001366  00                                       629+         DC    XL1'00'
00001367  02                                       630+         DC    HL1'2'            i3
00001368  1234                                     631+         DC    H'4660'           i2
0000136A  E5D3C9D7 40404040                        632+         DC    CL8'VLIP'         instruction name
00001374  00000010                                 633+         DC    A(16)             result length
00001378  0000138C                                 634+REA10    DC    A(RE10)           result address
                                                   635+*                                INSTRUCTION UNDER TEST ROUTINE
0000137C                                           636+X10      DS    0F
0000137C  E610 1234 2049                           637+         VLIP  V1,4660,2         test instruction
00001382  E710 8EB0 000E               000010B0    638+         VST   V1,V1OUTPUT       save
00001388  07FB                                     639+         BR    R11               return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000138C                                          640+RE10     DC    0F
0000138C                                          641+         DROP  R5
0000138C  00000000 00000000                       642          DC    XL16'0000000000000000000000000123400C'   V1
00001394  00000000 0123400C
                                                  643
                                                  644          VRI_H VLIP,4660,11                  i2=x'1234' sc=1, shamt=3
000013A0                                          645+         DS    0FD
000013A0                          000013A0        646+         USING *,R5               base for test data and test routine
000013A0  000013BC                                647+T11      DC    A(X11)             address of test routine
000013A4  000B                                    648+         DC    H'11'              test number
000013A6  00                                      649+         DC    XL1'00'
000013A7  0B                                      650+         DC    HL1'11'            i3
000013A8  1234                                    651+         DC    H'4660'            i2
000013AA  E5D3C9D7 40404040                       652+         DC    CL8'VLIP'          instruction name
000013B4  00000010                                653+         DC    A(16)              result length
000013B8  000013CC                                654+REA11    DC    A(RE11)            result address
                                                  655+*                                  INSTRUCTION UNDER TEST ROUTINE
000013BC                                          656+X11      DS    0F
000013BC  E610 1234 B049                          657+         VLIP  V1,4660,11         test instruction
000013C2  E710 8EB0 000E                000010B0  658+         VST   V1,V1OUTPUT        save
000013C8  07FB                                    659+         BR    R11                return
000013CC                                          660+RE11     DC    0F
000013CC                                          661+         DROP  R5
000013CC  00000000 00000000                       662          DC    XL16'0000000000000000000000001234000D'   V1
000013D4  00000000 1234000D
                                                  663
                                                  664
000013DC  00000000                                665          DC    F'0'     END OF TABLE
000013E0  00000000                                666          DC    F'0'
                                                  667 *
                                                  668 * table of pointers to individual load test
                                                  669 *
000013E4                                          670 E6TESTS  DS    0F
                                                  671          PTTABLE
000013E4                                          672+TTABLE   DS    0F
000013E4  00001120                                673+         DC    A(T1)              address of test
000013E8  00001160                                674+         DC    A(T2)              address of test
000013EC  000011A0                                675+         DC    A(T3)              address of test
000013F0  000011E0                                676+         DC    A(T4)              address of test
000013F4  00001220                                677+         DC    A(T5)              address of test
000013F8  00001260                                678+         DC    A(T6)              address of test
000013FC  000012A0                                679+         DC    A(T7)              address of test
00001400  000012E0                                680+         DC    A(T8)              address of test
00001404  00001320                                681+         DC    A(T9)              address of test
00001408  00001360                                682+         DC    A(T10)             address of test
0000140C  000013A0                                683+         DC    A(T11)             address of test
                                                  684+*
00001410  00000000                                685+         DC    A(0)               END OF TABLE
00001414  00000000                                686+         DC    A(0)
                                                  687
00001418  00000000                                688          DC    F'0'     END OF TABLE
0000141C  00000000                                689          DC    F'0'
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   691 ********************************************************************************
                                                   692 *        Register equates
                                                   693 ********************************************************************************

                             00000000  00000001   695 R0       EQU   0
                             00000001  00000001   696 R1       EQU   1
                             00000002  00000001   697 R2       EQU   2
                             00000003  00000001   698 R3       EQU   3
                             00000004  00000001   699 R4       EQU   4
                             00000005  00000001   700 R5       EQU   5
                             00000006  00000001   701 R6       EQU   6
                             00000007  00000001   702 R7       EQU   7
                             00000008  00000001   703 R8       EQU   8
                             00000009  00000001   704 R9       EQU   9
                             0000000A  00000001   705 R10      EQU   10
                             0000000B  00000001   706 R11      EQU   11
                             0000000C  00000001   707 R12      EQU   12
                             0000000D  00000001   708 R13      EQU   13
                             0000000E  00000001   709 R14      EQU   14
                             0000000F  00000001   710 R15      EQU   15

                                                   712 ********************************************************************************
                                                   713 *        Register equates
                                                   714 ********************************************************************************

                             00000000  00000001   716 V0       EQU   0
                             00000001  00000001   717 V1       EQU   1
                             00000002  00000001   718 V2       EQU   2
                             00000003  00000001   719 V3       EQU   3
                             00000004  00000001   720 V4       EQU   4
                             00000005  00000001   721 V5       EQU   5
                             00000006  00000001   722 V6       EQU   6
                             00000007  00000001   723 V7       EQU   7
                             00000008  00000001   724 V8       EQU   8
                             00000009  00000001   725 V9       EQU   9
                             0000000A  00000001   726 V10      EQU   10
                             0000000B  00000001   727 V11      EQU   11
                             0000000C  00000001   728 V12      EQU   12
                             0000000D  00000001   729 V13      EQU   13
                             0000000E  00000001   730 V14      EQU   14
                             0000000F  00000001   731 V15      EQU   15
                             00000010  00000001   732 V16      EQU   16
                             00000011  00000001   733 V17      EQU   17
                             00000012  00000001   734 V18      EQU   18
                             00000013  00000001   735 V19      EQU   19
                             00000014  00000001   736 V20      EQU   20
                             00000015  00000001   737 V21      EQU   21
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT
                                                      738 V22       EQU   22
                                 00000016  00000001
                                                      739 V23       EQU   23
                                 00000017  00000001
                                                      740 V24       EQU   24
                                 00000018  00000001
                                                      741 V25       EQU   25
                                 00000019  00000001
                                                      742 V26       EQU   26
                                 0000001A  00000001
                                                      743 V27       EQU   27
                                 0000001B  00000001
                                                      744 V28       EQU   28
                                 0000001C  00000001
                                                      745 V29       EQU   29
                                 0000001D  00000001
                                                      746 V30       EQU   30
                                 0000001E  00000001
                                                      747 V31       EQU   31
                                 0000001F  00000001
                                                      748
                                                      749           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	89	55 86 87
CCFOUND	X	00001098	1	318	
CCPSW	F	00001090	4	317	
CTLR0	F	000003FC	4	256	99 100 101 102
DECNUM	C	0000107E	16	313	136 138 145 147 152 154
E6TADR	A	00000404	4	259	108
E6TEST	4	00000000	28	338	115
E6TESTS	F	000013E4	4	670	259
EDIT	X	00001052	18	308	137 146 153
ENDTEST	U	000002D0	1	174	113
EOJ	I	000003E0	4	246	177
EOJPSW	D	000003D0	8	244	246
FAILCONT	U	000002C0	1	164	
FAILED	F	00001000	4	284	166 175
FAILMSG	U	00000258	1	134	124
FAILPSW	D	000003E8	8	248	250
FAILTEST	I	000003F8	4	250	178
I2	H	00000008	2	343	144
I3	U	00000007	1	342	151
IMAGE	1	00000000	5152	0	
K	U	00000400	1	268	269 270 271
K64	U	00010000	1	270	
MB	U	00100000	1	271	
MSG	I	00000318	4	210	193
MSGCMD	C	00000362	9	236	223 224
MSGMSG	C	0000036B	95	237	217 234 215
MSGMVC	I	0000035C	6	234	221
MSGOK	I	0000032E	2	219	216
MSGRET	I	00000348	4	230	227
MSGSAVE	F	00000350	4	233	213 230
NEXTE6	U	0000022A	1	110	127 169
OPNAME	C	0000000A	8	345	141
PAGE	U	00001000	1	269	
PRT3	C	00001068	18	311	137 138 139 146 147 148 153 154 155
PRTI2	C	00001040	5	297	148
PRTI3	C	0000104F	2	300	155
PRTLINE	C	00001004	16	292	302 158
PRTLNG	U	0000004E	1	302	157
PRTNAME	C	0000102F	8	295	141
PRTNUM	C	00001014	3	293	139
R0	U	00000000	1	695	49 99 102 157 165 166 192 194 210 213 215 217 219 230
R1	U	00000001	1	696	122 123 158 175 176 224 234
R10	U	0000000A	1	705	96 97
R11	U	0000000B	1	706	118 119 459 479 499 519 539 559 579 599 619 639 659
R12	U	0000000C	1	707	108 111 126 168
R13	U	0000000D	1	708	
R14	U	0000000E	1	709	
R15	U	0000000F	1	710	159 187 197 198
R2	U	00000002	1	697	135 136 143 144 145 150 151 152 192 193 194 211 213 219 220 221 223 230 231
R3	U	00000003	1	698	
R4	U	00000004	1	699	
R5	U	00000005	1	700	111 112 115 188 196 446 461 466 481 486 501 506 521 526 541 546 561 566 581 586 601 606 621 626 641 646 661
R6	U	00000006	1	701	
R7	U	00000007	1	702	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R8	U	00000008	1	703	86 89 90 91 93
R9	U	00000009	1	704	87 93 94 96
RE1	F	0000114C	4	460	454
RE10	F	0000138C	4	640	634
RE11	F	000013CC	4	660	654
RE2	F	0000118C	4	480	474
RE3	F	000011CC	4	500	494
RE4	F	0000120C	4	520	514
RE5	F	0000124C	4	540	534
RE6	F	0000128C	4	560	554
RE7	F	000012CC	4	580	574
RE8	F	0000130C	4	600	594
RE9	F	0000134C	4	620	614
REA1	A	00001138	4	454	
REA10	A	00001378	4	634	
REA11	A	000013B8	4	654	
REA2	A	00001178	4	474	
REA3	A	000011B8	4	494	
REA4	A	000011F8	4	514	
REA5	A	00001238	4	534	
REA6	A	00001278	4	554	
REA7	A	000012B8	4	574	
REA8	A	000012F8	4	594	
REA9	A	00001338	4	614	
READDR	A	00000018	4	348	122
REG2LOW	U	000000DD	1	274	
REG2PATT	U	AABBCCDD	1	273	
RELEN	A	00000014	4	347	
RPTDWSAV	D	00000308	8	203	192 194
RPTERROR	I	000002DE	4	187	159
RPTSAVE	F	000002FC	4	200	187 197
RPTSVR5	F	00000300	4	201	188 196
SVOLDPSW	U	00000140	0	51	
T1	A	00001120	4	447	673
T10	A	00001360	4	627	682
T11	A	000013A0	4	647	683
T2	A	00001160	4	467	674
T3	A	000011A0	4	487	675
T4	A	000011E0	4	507	676
T5	A	00001220	4	527	677
T6	A	00001260	4	547	678
T7	A	000012A0	4	567	679
T8	A	000012E0	4	587	680
T9	A	00001320	4	607	681
TESTREST	U	00000240	1	121	
TNUM	H	00000004	2	340	135
TSUB	A	00000000	4	339	118
TTABLE	F	000013E4	4	672	
V0	U	00000000	1	716	
V1	U	00000001	1	717	116 457 458 477 478 497 498 517 518 537 538 557 558 577 578 597 598 617 618 637 638 657 658
V10	U	0000000A	1	726	
V11	U	0000000B	1	727	
V12	U	0000000C	1	728	
V13	U	0000000D	1	729	
V14	U	0000000E	1	730	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V15	U	0000000F	1	731	
V16	U	00000010	1	732	
V17	U	00000011	1	733	
V18	U	00000012	1	734	
V19	U	00000013	1	735	
V1FUDGE	X	000010D0	16	327	
V1FUDGEB	X	000010E0	16	328	116
V1INPUT	C	000010F0	16	329	
V1OUTPUT	X	000010B0	16	325	123 458 478 498 518 538 558 578 598 618 638 658
V2	U	00000002	1	718	
V20	U	00000014	1	736	
V21	U	00000015	1	737	
V22	U	00000016	1	738	
V23	U	00000017	1	739	
V24	U	00000018	1	740	
V25	U	00000019	1	741	
V26	U	0000001A	1	742	
V27	U	0000001B	1	743	
V28	U	0000001C	1	744	
V29	U	0000001D	1	745	
V3	U	00000003	1	719	
V30	U	0000001E	1	746	
V31	U	0000001F	1	747	
V4	U	00000004	1	720	
V5	U	00000005	1	721	
V6	U	00000006	1	722	
V7	U	00000007	1	723	
V8	U	00000008	1	724	
V9	U	00000009	1	725	
X1	F	0000113C	4	456	447
X10	F	0000137C	4	636	627
X11	F	000013BC	4	656	647
X2	F	0000117C	4	476	467
X3	F	000011BC	4	496	487
X4	F	000011FC	4	516	507
X5	F	0000123C	4	536	527
X6	F	0000127C	4	556	547
X7	F	000012BC	4	576	567
X8	F	000012FC	4	596	587
X9	F	0000133C	4	616	607
ZVE6TST	J	00000000	5152	48	51 53 57 61 283 49
=AL2(L'MSGMSG)	R	0000040E	2	264	215
=F'1'	F	00000408	4	262	165
=H'0'	H	0000040C	2	263	210

```
 MACRO    DEFN   REFERENCES

PTTABLE    408    671
VRI_H      362    444    464    484    504    524    544    564    584    604    624    644
```

```
   DESC      SYMBOL   SIZE      POS         ADDR

Entry: 0

Image       IMAGE    5152   0000-141F   0000-141F
  Region             5152   0000-141F   0000-141F
    CSECT   ZVE6TST  5152   0000-141F   0000-141F
```

```
   STMT                    FILE NAME
1     /devstor/dev/tests/zvector-e6-10-VLIP.asm

** NO ERRORS FOUND **
```