```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                        2 ************************************************************************
                                                        3 *
                                                        4 *        Zvector E6 instruction tests for VRI-f encoded:
                                                        5 *
                                                        6 *        E670 VPKZR  - VECTOR PACK ZONED REGISTER
                                                        7 *
                                                        8 *        James Wekel June 2024
                                                        9 ************************************************************************
                                                       10
                                                       11 ************************************************************************
                                                       12 *
                                                       13 *        basic instruction tests
                                                       14 *
                                                       15 ************************************************************************
                                                       16 *  This program tests proper functioning of the z/arch E6 VRI-f vector
                                                       17 *  pack zoned register instruction. Exceptions are not tested.
                                                       18 *
                                                       19 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                       20 *  obvious coding errors.  None of the tests are thorough.  They are
                                                       21 *  NOT designed to test all aspects of any of the instructions.
                                                       22 *
                                                       23 ************************************************************************
                                                       24 *
                                                       25 *   *Testcase VECTOR E6 VPKZR: packed zoned register instruction
                                                       26 *   *
                                                       27 *   *   Zvector E6 tests for VRI-f encoded pack instructions:
                                                       28 *   *
                                                       29 *   *   E670 VPKZR  - VECTOR PACK ZONED REGISTER VPKZR
                                                       30 *   *
                                                       31 *   *   # ------------------------------------------------------------
                                                       32 *   *   #  This tests only the basic function of the instruction.
                                                       33 *   *   #  Exceptions are NOT tested.
                                                       34 *   *   # ------------------------------------------------------------
                                                       35 *   *
                                                       36 *   mainsize    2
                                                       37 *   numcpu      1
                                                       38 *   sysclear
                                                       39 *   archlvl     z/Arch
                                                       40 *
                                                       41 *   loadcore    "$(testpath)/zvector-e6-06-VPKZR.core" 0x0
                                                       42 *
                                                       43 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                       44 *   runtest     2
                                                       45 *   diag8cmd    disable   # (reset back to default)
                                                       46 *
                                                       47 *   *Done
                                                       48 ************************************************************************

                          00000000  000019D7     50 ZVE6TST  START 0
00000000                  00000000               51          USING ZVE6TST,R0            Low core addressability
                                                       52
                          00000140  00000000     53 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW

00000000                  00000000  000001A0     55          ORG   ZVE6TST+X'1A0'        z/Architecure RESTART PSW
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
000001A0  00000001 80000000                           56          DC    X'0000000180000000'
000001A8  00000000 00000200                           57          DC    AD(BEGIN)

000001B0                      000001B0  000001D0      59          ORG   ZVE6TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                           60          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                           61          DC    AD(X'DEAD')

000001E0                      000001E0  00000200      63          ORG   ZVE6TST+X'200'        Start of actual test program...
                                                      64
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    66 ********************************************************************************
                                                    67 *                The actual "ZVE6TST" program itself...
                                                    68 ********************************************************************************
                                                    69 *
                                                    70 *  Architecture Mode: z/Arch
                                                    71 *  Register Usage:
                                                    72 *
                                                    73 *   R0       (work)
                                                    74 *   R1-4     (work)
                                                    75 *   R5       Testing control table - current test base
                                                    76 *   R6-R7    (work)
                                                    77 *   R8       First base register
                                                    78 *   R9       Second base register
                                                    79 *   R10      Third base register
                                                    80 *   R11      E6TEST call return
                                                    81 *   R12      E6TESTS register
                                                    82 *   R13      (work)
                                                    83 *   R14      Subroutine call
                                                    84 *   R15      Secondary Subroutine call or work
                                                    85 *
                                                    86 ********************************************************************************

00000200                          00000200          88          USING  BEGIN,R8        FIRST Base Register
00000200                          00001200          89          USING  BEGIN+4096,R9   SECOND Base Register

00000200  0580                                      91 BEGIN     BALR  R8,0             Initalize FIRST base register
00000202  0680                                      92           BCTR  R8,0             Initalize FIRST base register
00000204  0680                                      93           BCTR  R8,0             Initalize FIRST base register

00000206  4190 8800                 00000800       95           LA    R9,2048(,R8)     Initalize SECOND base register
0000020A  4190 9800                 00000800       96           LA    R9,2048(,R9)     Initalize SECOND base register

0000020E  41A0 9800                 00000800       98           LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                 00000800       99           LA    R10,2048(,R10)   Initalize THIRD base register
                                                   100
00000216  B600 82A4                 000004A4      101           STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 82A5                 000004A5      102           OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 82A5                 000004A5      103           OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 82A4                 000004A4      104           LCTL  R0,R0,CTLR0      Reload updated CR0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    106 ********************************************************************************
                                                    107 *               Do tests in the E6TESTS table
                                                    108 ********************************************************************************
                                                    109
00000226  58C0 82AC                      000004AC   110           L     R12,E6TADR       get table of test addresses
                                                    111
                                0000022A  00000001   112 NEXTE6    EQU   *
0000022A  5850 C000                      00000000   113           L     R5,0(0,R12)       get test address
0000022E  1255                                      114           LTR   R5,R5                have a test?
00000230  4780 8176                      00000376   115           BZ    ENDTEST                 done?
                                                    116
00000234  B982 0000                                 117           XGR   R0,R0              no cc error
                                                    118
00000238                                 00000000   119           USING E6TEST,R5
00000238  E710 8F20 0006                 00001120   120           VL    V1,V1FUDGE
0000023E  58B0 5000                      00000000   121           L     R11,TSUB           get address of test routine
00000242  05BB                                      122           BALR  R11,R11            do test
                                                    123
00000244  E310 500A 0076                 0000000A   124           LB    R1,CCMASK          (failure CC mask)
0000024A  8910 0004                      00000004   125           SLL   R1,4               (shift to BC instr CC position)
0000024E  4410 806A                      0000026A   126           EX    R1,TESTCC             fail if...
                                                    127
                                00000252  00000001   128 TESTREST EQU   *
00000252  E310 5020 0014                 00000020   129           LGF   R1,READDR          get address of expected result
00000258  D50F 8F00 1000       00001100  00000000   130           CLC   V1OUTPUT,0(R1)     valid?
0000025E  4770 80FE                      000002FE   131           BNE   FAILMSG               no, issue failed message
                                                    132
00000262  41C0 C004                      00000004   133           LA    R12,4(0,R12)        next test address
00000266  47F0 802A                      0000022A   134           B     NEXTE6
                                                    135
0000026A  4700 806E                      0000026E   136 TESTCC    BC    0,CCMSG          (fail if unexpected condition code)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    138 ********************************************************************************
                                                    139 * cc was not as expected
                                                    140 ********************************************************************************
                               0000026E  00000001   141 CCMSG    EQU   *
0000026E  E310 0001 0082                 00000001   142          XG    R1,R1
00000274  E310 5008 0076                 00000008   143          LB    R1,M5           M5 has CS bit
0000027A  5410 82B0                      000004B0   144          N     R1,=F'1'        get CS (CC set) bit
0000027E  4780 8052                      00000252   145          BZ    TESTREST           ignore if not set
                                                    146 *
                                                    147 * extract CC extracted PSW
                                                    148 *
00000282  5810 8EE4                      000010E4   149          L     R1,CCPSW
00000286  8810 000C                      0000000C   150          SRL   R1,12
0000028A  5410 82B4                      000004B4   151          N     R1,=XL4'3'
0000028E  4210 8EEC                      000010EC   152          STC   R1,CCFOUND      save cc
                                                    153 *
                                                    154 * FILL IN MESSAGE
                                                    155 *
00000292  4820 5004                      00000004   156          LH    R2,TNUM                  get test number and convert
00000296  4E20 8ED1                      000010D1   157          CVD   R2,DECNUM
0000029A  D211 8EBB 8EA5       000010BB  000010A5   158          MVC   PRT3,EDIT
000002A0  DE11 8EBB 8ED1       000010BB  000010D1   159          ED    PRT3,DECNUM
000002A6  D202 8E60 8EC8       00001060  000010C8   160          MVC   CCPRTNUM(3),PRT3+13      fill in message with test #
                                                    161
000002AC  D207 8E7D 5014       0000107D  00000014   162          MVC   CCPRTNAME,OPNAME         fill in message with instruction
                                                    163
000002B2  B982 0022                                 164          XGR   R2,R2                    get CC as U8
000002B6  4320 5009                      00000009   165          IC    R2,CC
000002BA  4E20 8ED1                      000010D1   166          CVD   R2,DECNUM                and convert
000002BE  D211 8EBB 8EA5       000010BB  000010A5   167          MVC   PRT3,EDIT
000002C4  DE11 8EBB 8ED1       000010BB  000010D1   168          ED    PRT3,DECNUM
000002CA  D200 8E93 8ECA       00001093  000010CA   169          MVC   CCPRTEXP(1),PRT3+15      fill in message with CC field
                                                    170
000002D0  B982 0022                                 171          XGR   R2,R2                    get CCFOUND as U8
000002D4  4320 8EEC                      000010EC   172          IC    R2,CCFOUND
000002D8  4E20 8ED1                      000010D1   173          CVD   R2,DECNUM                and convert
000002DC  D211 8EBB 8EA5       000010BB  000010A5   174          MVC   PRT3,EDIT
000002E2  DE11 8EBB 8ED1       000010BB  000010D1   175          ED    PRT3,DECNUM
000002E8  D200 8EA3 8ECA       000010A3  000010CA   176          MVC   CCPRTGOT(1),PRT3+15    fill in message with ccfound
                                                    177
000002EE  4100 0055                      00000055   178          LA    R0,CCPRTLNG              message length
000002F2  4110 8E50                      00001050   179          LA    R1,CCPRTLINE             messagfe address
000002F6  45F0 8184                      00000384   180          BAL   R15,RPTERROR
                                                    181
000002FA  47F0 8166                      00000366   182          B     FAILCONT
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   184 ************************************************************************
                                                   185 * result not as expected:
                                                   186 *        issue message with test number, instruction under test
                                                   187 *              and instruction m3
                                                   188 ************************************************************************
                             000002FE  00000001    189 FAILMSG  EQU   *
000002FE  4820 5004                    00000004    190          LH    R2,TNUM              get test number and convert
00000302  4E20 8ED1                    000010D1    191          CVD   R2,DECNUM
00000306  D211 8EBB 8EA5       000010BB  000010A5  192          MVC   PRT3,EDIT
0000030C  DE11 8EBB 8ED1       000010BB  000010D1  193          ED    PRT3,DECNUM
00000312  D202 8E14 8EC8       00001014  000010C8  194          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                   195
00000318  D207 8E2F 5014       0000102F  00000014  196          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                   197
0000031E  B982 0022                                198          XGR   R2,R2                get i4 as U8
00000322  4320 5007                    00000007    199          IC    R2,I4
00000326  4E20 8ED1                    000010D1    200          CVD   R2,DECNUM            and convert
0000032A  D211 8EBB 8EA5       000010BB  000010A5  201          MVC   PRT3,EDIT
00000330  DE11 8EBB 8ED1       000010BB  000010D1  202          ED    PRT3,DECNUM
00000336  D202 8E40 8EC8       00001040  000010C8  203          MVC   PRTI4(3),PRT3+13     fill in message with i4 field
                                                   204
0000033C  B982 0022                                205          XGR   R2,R2                get m5 as U8
00000340  4320 5008                    00000008    206          IC    R2,M5                and convert
00000344  4E20 8ED1                    000010D1    207          CVD   R2,DECNUM
00000348  D211 8EBB 8EA5       000010BB  000010A5  208          MVC   PRT3,EDIT
0000034E  DE11 8EBB 8ED1       000010BB  000010D1  209          ED    PRT3,DECNUM
00000354  D201 8E4D 8EC9       0000104D  000010C9  210          MVC   PRTM5(2),PRT3+14     fill in message with m5 field
                                                   211
0000035A  4100 004C                    0000004C    212          LA    R0,PRTLNG            message length
0000035E  4110 8E04                    00001004    213          LA    R1,PRTLINE           messagfe address
00000362  45F0 8184                    00000384    214          BAL   R15,RPTERROR

                                                   216 ************************************************************************
                                                   217 * continue after a failed test
                                                   218 ************************************************************************
                             00000366  00000001    219 FAILCONT EQU   *
00000366  5800 82B0                    000004B0    220          L     R0,=F'1'           set GLOBAL failed test indicator
0000036A  5000 8E00                    00001000    221          ST    R0,FAILED
                                                   222
0000036E  41C0 C004                    00000004    223          LA    R12,4(0,R12)       next test address
00000372  47F0 802A                    0000022A    224          B     NEXTE6


                                                   226 ************************************************************************
                                                   227 * end of testing; set ending psw
                                                   228 ************************************************************************
                             00000376  00000001    229 ENDTEST  EQU   *
00000376  5810 8E00                    00001000    230          L     R1,FAILED          did a test fail?
0000037A  1211                                     231          LTR   R1,R1
0000037C  4780 8288                    00000488    232          BZ    EOJ                   No, exit
00000380  47F0 82A0                    000004A0    233          B     FAILTEST              Yes, exit with BAD PSW
                                                   234
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    236 ************************************************************************
                                                    237 *        RPTERROR          Report instruction test in error
                                                    238 *                             R0 = MESSGAE LENGTH
                                                    239 *                             R1 = ADDRESS OF MESSAGE
                                                    240 ************************************************************************

00000384  50F0 81A4                 000003A4    242 RPTERROR ST    R15,RPTSAVE          Save return address
00000388  5050 81A8                 000003A8    243          ST    R5,RPTSVR5           Save R5
                                                    244 *
                                                    245 *        Use Hercules Diagnose for Message to console
                                                    246 *
0000038C  9002 81B0                 000003B0    247          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000390  4520 81C0                 000003C0    248          BAL   R2,MSG               call Hercules console MSG display
00000394  9802 81B0                 000003B0    249          LM    R0,R2,RPTDWSAV       restore regs


00000398  5850 81A8                 000003A8    251          L     R5,RPTSVR5           Restore R5
0000039C  58F0 81A4                 000003A4    252          L     R15,RPTSAVE          Restore return address
000003A0  07FF                                  253          BR    R15                  Return to caller

000003A4  00000000                              255 RPTSAVE  DC    F'0'                 R15 save area
000003A8  00000000                              256 RPTSVR5  DC    F'0'                 R5 save area

000003B0  00000000 00000000                     258 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    260 ************************************************************************
                                                    261 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    262 *              R2 = return address
                                                    263 ************************************************************************
                                                    264
000003C0  4900 82B8                  000004B8     265 MSG      CH    R0,=H'0'                 Do we even HAVE a message?
000003C4  07D2                                    266          BNHR  R2                       No, ignore
                                                  267
000003C6  9002 81F8                  000003F8     268          STM   R0,R2,MSGSAVE            Save registers
                                                  269
000003CA  4900 82BA                  000004BA     270          CH    R0,=AL2(L'MSGMSG)        Message length within limits?
000003CE  47D0 81D6                  000003D6     271          BNH   MSGOK                    Yes, continue
000003D2  4100 005F                  0000005F     272          LA    R0,L'MSGMSG              No, set to maximum
                                                  273
000003D6  1820                                    274 MSGOK    LR    R2,R0                    Copy length to work register
000003D8  0620                                    275          BCTR  R2,0                     Minus-1 for execute
000003DA  4420 8204                  00000404     276          EX    R2,MSGMVC                Copy message to O/P buffer
                                                  277
000003DE  4120 200A                  0000000A     278          LA    R2,1+L'MSGCMD(,R2)       Calculate true command length
000003E2  4110 820A                  0000040A     279          LA    R1,MSGCMD                Point to true command
                                                  280
000003E6  83120008                                281          DC    X'83',X'12',X'0008'      Issue Hercules Diagnose X'008'
000003EA  4780 81F0                  000003F0     282          BZ    MSGRET                   Return if successful
000003EE  0000                                    283          DC    H'0'                     CRASH for debugging purposes
                                                  284
000003F0  9802 81F8                  000003F8     285 MSGRET   LM    R0,R2,MSGSAVE            Restore registers
000003F4  07F2                                    286          BR    R2                       Return to caller


000003F8  00000000 00000000                       288 MSGSAVE  DC    3F'0'                    Registers save area
00000404  D200 8213 1000      00000413  00000000  289 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction


0000040A  D4E2C7D5 D6C8405C                       291 MSGCMD   DC    C'MSGNOH * '             *** HERCULES MESSAGE COMMAND ***
00000413  40404040 40404040                       292 MSGMSG   DC    CL95' '                  The message text to be displayed
                                                  293
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      295 ************************************************************************
                                                      296 *        Normal completion or Abnormal termination PSWs
                                                      297 ************************************************************************


00000478  00020001 80000000                           299 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000488  B2B2 8278                         00000478  301 EOJ      LPSWE EOJPSW               Normal completion


00000490  00020001 80000000                           303 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

000004A0  B2B2 8290                         00000490  305 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                      307 ************************************************************************
                                                      308 *        Working Storage
                                                      309 ************************************************************************

000004A4  00000000                                    311 CTLR0    DS    F                    CR0
000004A8  00000000                                    312          DS    F
                                                      313
000004AC  00001988                                    314 E6TADR   DC    A(E6TESTS)           address of E6 test table


000004B0                                              316          LTORG ,                    Literals pool
000004B0  00000001                                    317                =F'1'
000004B4  00000003                                    318                =XL4'3'
000004B8  0000                                        319                =H'0'
000004BA  005F                                        320                =AL2(L'MSGMSG)
                                                      321
                                                      322 *        some constants
                                                      323
                            00000400  00000001        324 K        EQU   1024                 One KB
                            00001000  00000001        325 PAGE     EQU   (4*K)                Size of one page
                            00010000  00000001        326 K64      EQU   (64*K)               64 KB
                            00100000  00000001        327 MB       EQU   (K*K)                 1 MB
                                                      328
                            AABBCCDD  00000001        329 REG2PATT EQU   X'AABBCCDD'      Polluted Register pattern
                            000000DD  00000001        330 REG2LOW  EQU         X'DD'      (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    332 *=====================================================================
                                                    333 *
                                                    334 *  NOTE: start data on an address that is easy to display
                                                    335 *        within Hercules
                                                    336 *
                                                    337 *=====================================================================
                                                    338
000004BC                      000004BC  00001000    339          ORG   ZVE6TST+X'1000'
00001000  00000000                                  340 FAILED   DC    F'0'                      some test failed?


                                                    342 ************************************************************************
                                                    343 *        TEST failed : result messgae
                                                    344 ************************************************************************
                                                    345 *
                                                    346 *        failed message and associated editting
                                                    347 *
00001004  40404040 40404040                         348 PRTLINE  DC    C'         Test # '
00001014  A7A7A7                                    349 PRTNUM   DC    C'xxx'
00001017  40868189 93858440                         350          DC    C' failed for instruction '
0000102F  A7A7A7A7 A7A7A7A7                         351 PRTNAME  DC    CL8'xxxxxxxx'
00001037  40A689A3 884089F4                         352          DC    C' with i4='
00001040  A7A7A7                                    353 PRTI4    DC    C'xxx'
00001043  6B                                        354          DC    C','
00001044  40A689A3 884094F5                         355          DC    C' with m5='
0000104D  A7A7                                      356 PRTM5    DC    C'xx'
0000104F  4B                                        357          DC    C'.'
                                0000004C  00000001  358 PRTLNG   EQU   *-PRTLINE


                                                    360 ************************************************************************
                                                    361 *        TEST failed : CC message
                                                    362 ************************************************************************
                                                    363 *
                                                    364 *        failed message and associated editting
                                                    365 *
00001050  40404040 40404040                         366 CCPRTLINE DC   C'         Test # '
00001060  A7A7A7                                    367 CCPRTNUM DC    C'xxx'
00001063  40A69996 95874083                         368          DC    c' wrong cc for instruction '
0000107D  A7A7A7A7 A7A7A7A7                         369 CCPRTNAME DC    CL8'xxxxxxxx'
00001085  4085A797 8583A385                         370          DC    C' expected: cc='
00001093  A7                                        371 CCPRTEXP DC    C'x'
00001094  6B                                        372          DC    C','
00001095  40998583 8589A585                         373          DC    C' received: cc='
000010A3  A7                                        374 CCPRTGOT DC    C'x'
000010A4  4B                                        375          DC    C'.'
                                00000055  00000001  376 CCPRTLNG   EQU   *-CCPRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    378 ************************************************************************
                                                    379 *        TEST failed : message working storge
                                                    380 ************************************************************************
000010A5  40212020 20202020                         381 EDIT     DC    XL18'4021202020202020202020202020202020'
                                                    382
000010B7  7E7E7E6E                                  383          DC    C'===>'
000010BB  40404040 40404040                         384 PRT3     DC    CL18' '
000010CD  4C7E7E7E                                  385          DC    C'<==='
000010D1  00000000 00000000                         386 DECNUM   DS    CL16
                                                    387 *
                                                    388 *        CC extrtaction
                                                    389 *
000010E4  00000000 00000000                         390 CCPSW    DS    2F          extract PSW after test (has CC)
000010EC  00                                        391 CCFOUND  DS    X           extracted cc

                                                    393 ************************************************************************
                                                    394 *        Vector instruction results, pollution and input
                                                    395 ************************************************************************
000010F0                                            396          DS    0FD
000010F0  00000000 00000000                         397          DS    XL16                                    gap
00001100  00000000 00000000                         398 V1OUTPUT DS    XL16                                  V1 OUTPUT
00001110  00000000 00000000                         399          DS    XL16                                    gap
00001120  FFFFFFFF FFFFFFFF                         400 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'  V1 FUDGE
00001130  F1F2F3F4 F5F6F7F8                         401 V1INPUT  DC    CL16'1234567890123456'                  V1 input
00001140  F7F8F9F0 F1F2F3F4                         402          DC    CL14'78901234567890'
0000114E  D9                                        403          DC    X'D9'
0000114F  00000000 00000000                         404 V2PACKED DS    XL16              packed version of macro v2
0000115F  00000000 00000000                         405 V3PACKED DS    XL16              packed version of macro v3
0000116F  00000000 00000000                         406          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     408 ********************************************************************************
                                                     409 *        E6TEST DSECT
                                                     410 ********************************************************************************


                                                     412 E6TEST   DSECT ,
00000000  00000000                                   413 TSUB     DC    A(0)              pointer  to test
00000004  0000                                       414 TNUM     DC    H'00'             Test Number
00000006  00                                         415          DC    X'00'
00000007  00                                         416 I4       DC    HL1'00'           I4 used
00000008  00                                         417 M5       DC    HL1'00'           M5 used
00000009  00                                         418 CC       DC    HL1'00'           cc
0000000A  00                                         419 CCMASK   DC    HL1'00'           not expected CC mask
                                                     420
0000000C  00000000                                   421 V2VALUE  DC    A(0)
00000010  00000000                                   422 V3VALUE  DC    A(0)
                                                     423
00000014  40404040 40404040                          424 OPNAME   DC    CL8' '            E6 name
                                                     425
0000001C  00000000                                   426 RELEN    DC    A(0)              result length
00000020  00000000                                   427 READDR   DC    A(0)              expected result address
                                                     428
                                                     429 *        EXPECTED RESULT
                                                     430 **
                                                     431 *        test routine will be here (from VRI_F macro)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    433 ************************************************************************
                                                    434 *     Macros to help build test tables
                                                    435 *----------------------------------------------------------------------
                                                    436 *     VRI_F Macro to help build test tables
                                                    437 ************************************************************************
                                                    438          MACRO
                                                    439          VRI_F &INST,&I4,&M5,&CC
                                                    440 .*                                &INST - VRI-f instruction under test
                                                    441 .*                                &i4   - i4 field
                                                    442 .*                                &m5   - m5 field
                                                    443 .*                                &CC   - expected CC
                                                    444 .*
                                                    445          LCLA  &XCC(4)  &CC has mask values for FAILED condition codes
                                                    446 &XCC(1)  SETA  7                  CC != 0
                                                    447 &XCC(2)  SETA  11                 CC != 1
                                                    448 &XCC(3)  SETA  13                 CC != 2
                                                    449 &XCC(4)  SETA  14                 CC != 3
                                                    450
                                                    451          GBLA  &TNUM
                                                    452 &TNUM    SETA  &TNUM+1
                                                    453
                                                    454          DS    0FD
                                                    455          USING *,R5               base for test data and test routine
                                                    456
                                                    457 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                    458          DC    H'&TNUM'           test number
                                                    459          DC    X'00'
                                                    460          DC    HL1'&I4'           i4
                                                    461          DC    HL1'&M5'           m5
                                                    462          DC    HL1'&CC'           cc
                                                    463          DC    HL1'&XCC(&CC+1)'   cc failed mask
                                                    464 V2_&TNUM DC    A(RE&TNUM+16)      address of v2: 16-byte zoned decimal
                                                    465 V3_&TNUM DC    A(RE&TNUM+32)      address of v3: 16-byte zoned decimal
                                                    466          DC    CL8'&INST'         instruction name
                                                    467          DC    A(16)              result length
                                                    468 REA&TNUM DC    A(RE&TNUM)         result address
                                                    469 .*
                                                    470 *                                 INSTRUCTION UNDER TEST ROUTINE
                                                    471 X&TNUM   DS    0F
                                                    472          L     R2,V2_&TNUM        get v2
                                                    473          VL    V2,0(R2)
                                                    474
                                                    475          L     R2,V3_&TNUM        get v3
                                                    476          VL    V3,0(R2)
                                                    477
                                                    478          &INST V1,V2,V3,&I4,&M5   test instruction
                                                    479
                                                    480          VST   V1,V1OUTPUT        save result
                                                    481          EPSW  R2,R0              exptract psw
                                                    482          ST    R2,CCPSW               to save CC
                                                    483          BR    R11                return
                                                    484
                                                    485 RE&TNUM  DC    0F
                                                    486          DROP  R5
                                                    487
                                                    488          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      490 ********************************************************************************
                                                      491 *     PTTABLE Macro to generate table of pointers to individual tests
                                                      492 ********************************************************************************
                                                      493
                                                      494          MACRO
                                                      495          PTTABLE
                                                      496          GBLA  &TNUM
                                                      497          LCLA  &CUR
                                                      498 &CUR     SETA  1
                                                      499 .*
                                                      500 TTABLE   DS    0F
                                                      501 .LOOP    ANOP
                                                      502 .*
                                                      503          DC    A(T&CUR)           address of test
                                                      504 .*
                                                      505 &CUR     SETA  &CUR+1
                                                      506          AIF   (&CUR LE &TNUM).LOOP
                                                      507 *
                                                      508          DC    A(0)               END OF TABLE
                                                      509          DC    A(0)
                                                      510 .*
                                                      511          MEND
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      513 ********************************************************************************
                                                      514 *        E6 VRI_F tests
                                                      515 ********************************************************************************
                                00000000  000019D7    516 ZVE6TST  CSECT ,
00001180                                              517         DS    0F


                                                      519         PRINT DATA
                                                      520 *
                                                      521 *        E670 VPKZR  - VECTOR PACK ZONED REGISTER
                                                      522 *
                                                      523 *        VRI_F instr,i4,m5,cc
                                                      524 *              followed by
                                                      525 *              v1 - 16 byte expected result
                                                      526 *              v2 - 16 byte zoned decimal (operand)
                                                      527 *              v3 - 16 byte zoned decimal (operand)
                                                      528
                                                      529 *-------------------------------------------------------------------
                                                      530 * VPKZR  - VECTOR PACK ZONED REGISTER
                                                      531 *-------------------------------------------------------------------
                                                      532 * VPKZR simple + CC checks
                                                      533 *                                                 i4=129(iom=1 & rdc=1)
                                                      534 *                                                 i4=132(iom=1 & rdc=4)
                                                      535 *                                                 i4=135(iom=1 & rdc=7)
                                                      536 *                                                 i4=142(iom=1 & rdc=14)
                                                      537 *                                                 i4=159(iom=1 & rdc=31)
                                                      538         VRI_F VPKZR,159,1,2
00001180                                              539+        DS    0FD
00001180                          00001180            540+        USING *,R5              base for test data and test routine
00001180  000011A4                                    541+T1      DC    A(X1)             address of test routine
00001184  0001                                        542+        DC    H'1'              test number
00001186  00                                          543+        DC    X'00'
00001187  9F                                          544+        DC    HL1'159'          i4
00001188  01                                          545+        DC    HL1'1'            m5
00001189  02                                          546+        DC    HL1'2'            cc
0000118A  0D                                          547+        DC    HL1'13'           cc failed mask
0000118C  000011E0                                    548+V2_1    DC    A(RE1+16)         address of v2: 16-byte zoned decimal
00001190  000011F0                                    549+V3_1    DC    A(RE1+32)         address of v3: 16-byte zoned decimal
00001194  E5D7D2E9 D9404040                           550+        DC    CL8'VPKZR'        instruction name
0000119C  00000010                                    551+        DC    A(16)             result length
000011A0  000011D0                                    552+REA1    DC    A(RE1)            result address
                                                      553+*                               INSTRUCTION UNDER TEST ROUTINE
000011A4                                              554+X1      DS    0F
000011A4  5820 500C                     0000118C      555+        L     R2,V2_1           get v2
000011A8  E722 0000 0006                00000000      556+        VL    V2,0(R2)
000011AE  5820 5010                     00001190      557+        L     R2,V3_1           get v3
000011B2  E732 0000 0006                00000000      558+        VL    V3,0(R2)
000011B8  E612 3019 F070                              559+        VPKZR V1,V2,V3,159,1    test instruction
000011BE  E710 8F00 000E                00001100      560+        VST   V1,V1OUTPUT       save result
000011C4  B98D 0020                                   561+        EPSW  R2,R0             exptract psw
000011C8  5020 8EE4                     000010E4      562+        ST    R2,CCPSW              to save CC
000011CC  07FB                                        563+        BR    R11               return
000011D0                                              564+RE1     DC    0F
000011D0                                              565+        DROP  R5
000011D0  00000000 00000000                          566         DC    XL16'0000000000000000000000000000022C'    V1
000011D8  00000000 0000022C
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000011E0  F0F0F0F0 F0F0F0F0                      567          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000011E8  F0F0F0F0 F0F0F0F0
000011F0  F0F0F0F0 F0F0F0F0                      568          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F2C2'    V3
000011F8  F0F0F0F0 F0F0F2C2
                                                 569
                                                 570          VRI_F VPKZR,159,1,2
00001200                                         571+         DS    0FD
00001200                          00001200       572+         USING *,R5              base for test data and test routine
00001200  00001224                               573+T2       DC    A(X2)             address of test routine
00001204  0002                                   574+         DC    H'2'              test number
00001206  00                                     575+         DC    X'00'
00001207  9F                                     576+         DC    HL1'159'          i4
00001208  01                                     577+         DC    HL1'1'            m5
00001209  02                                     578+         DC    HL1'2'            cc
0000120A  0D                                     579+         DC    HL1'13'           cc failed mask
0000120C  00001260                               580+V2_2     DC    A(RE2+16)         address of v2: 16-byte zoned decimal
00001210  00001270                               581+V3_2     DC    A(RE2+32)         address of v3: 16-byte zoned decimal
00001214  E5D7D2E9 D9404040                      582+         DC    CL8'VPKZR'        instruction name
0000121C  00000010                               583+         DC    A(16)             result length
00001220  00001250                               584+REA2     DC    A(RE2)            result address
                                                 585+*                                INSTRUCTION UNDER TEST ROUTINE
00001224                                         586+X2       DS    0F
00001224  5820 900C                     0000120C 587+         L     R2,V2_2           get v2
00001228  E722 0000 0006                00000000 588+         VL    V2,0(R2)
0000122E  5820 9010                     00001210 589+         L     R2,V3_2           get v3
00001232  E732 0000 0006                00000000 590+         VL    V3,0(R2)
00001238  E612 3019 F070                         591+         VPKZR V1,V2,V3,159,1    test instruction
0000123E  E710 8F00 000E                00001100 592+         VST   V1,V1OUTPUT       save result
00001244  B98D 0020                              593+         EPSW  R2,R0             exptract psw
00001248  5020 8EE4                     000010E4 594+         ST    R2,CCPSW              to save CC
0000124C  07FB                                   595+         BR    R11               return
00001250                                         596+RE2      DC    0F
00001250                                         597+         DROP  R5
00001250  12300000 00000000                      598          DC    XL16'12300000000000000000000000000122C'    V1
00001258  00000000 0000122C
00001260  F0F1F2F3 F0F0F0F0                      599          DC    XL16'F0F1F2F3F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001268  F0F0F0F0 F0F0F0F0
00001270  F0F0F0F0 F0F0F0F0                      600          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F2C2'    V3
00001278  F0F0F0F0 F0F1F2C2
                                                 601
                                                 602          VRI_F VPKZR,159,1,1
00001280                                         603+         DS    0FD
00001280                          00001280       604+         USING *,R5              base for test data and test routine
00001280  000012A4                               605+T3       DC    A(X3)             address of test routine
00001284  0003                                   606+         DC    H'3'              test number
00001286  00                                     607+         DC    X'00'
00001287  9F                                     608+         DC    HL1'159'          i4
00001288  01                                     609+         DC    HL1'1'            m5
00001289  01                                     610+         DC    HL1'1'            cc
0000128A  0B                                     611+         DC    HL1'11'           cc failed mask
0000128C  000012E0                               612+V2_3     DC    A(RE3+16)         address of v2: 16-byte zoned decimal
00001290  000012F0                               613+V3_3     DC    A(RE3+32)         address of v3: 16-byte zoned decimal
00001294  E5D7D2E9 D9404040                      614+         DC    CL8'VPKZR'        instruction name
0000129C  00000010                               615+         DC    A(16)             result length
000012A0  000012D0                               616+REA3     DC    A(RE3)            result address
                                                 617+*                                INSTRUCTION UNDER TEST ROUTINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
000012A4                                          618+X3       DS    0F
000012A4  5820 500C                     0000128C  619+         L     R2,V2_3           get v2
000012A8  E722 0000 0006                00000000  620+         VL    V2,0(R2)
000012AE  5820 5010                     00001290  621+         L     R2,V3_3           get v3
000012B2  E732 0000 0006                00000000  622+         VL    V3,0(R2)
000012B8  E612 3019 F070                          623+         VPKZR V1,V2,V3,159,1    test instruction
000012BE  E710 8F00 000E                00001100  624+         VST   V1,V1OUTPUT       save result
000012C4  B98D 0020                               625+         EPSW  R2,R0             exptract psw
000012C8  5020 8EE4                     000010E4  626+         ST    R2,CCPSW              to save CC
000012CC  07FB                                    627+         BR    R11               return
000012D0                                          628+RE3      DC    0F
000012D0                                          629+         DROP  R5
000012D0  98700000 00000000                       630          DC    XL16'9870000000000000000000000000123D'    V1
000012D8  00000000 0000123D
000012E0  F0F9F8F7 F0F0F0F0                       631          DC    XL16'F0F9F8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000012E8  F0F0F0F0 F0F0F0F0
000012F0  F0F0F0F0 F0F0F0F0                       632          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F1F2D3'    V3
000012F8  F0F0F0F0 F0F1F2D3
                                                  633
                                                  634          VRI_F VPKZR,159,1,3         (overflow; 1st zone is not 0 )
00001300                                          635+         DS    0FD
00001300                  00001300                636+         USING *,R5              base for test data and test routine
00001300  00001324                                637+T4       DC    A(X4)             address of test routine
00001304  0004                                    638+         DC    H'4'              test number
00001306  00                                      639+         DC    X'00'
00001307  9F                                      640+         DC    HL1'159'          i4
00001308  01                                      641+         DC    HL1'1'            m5
00001309  03                                      642+         DC    HL1'3'            cc
0000130A  0E                                      643+         DC    HL1'14'           cc failed mask
0000130C  00001360                                644+V2_4     DC    A(RE4+16)         address of v2: 16-byte zoned decimal
00001310  00001370                                645+V3_4     DC    A(RE4+32)         address of v3: 16-byte zoned decimal
00001314  E5D7D2E9 D9404040                       646+         DC    CL8'VPKZR'        instruction name
0000131C  00000010                                647+         DC    A(16)             result length
00001320  00001350                                648+REA4     DC    A(RE4)            result address
                                                  649+*                                INSTRUCTION UNDER TEST ROUTINE
00001324                                          650+X4       DS    0F
00001324  5820 500C                     0000130C  651+         L     R2,V2_4           get v2
00001328  E722 0000 0006                00000000  652+         VL    V2,0(R2)
0000132E  5820 5010                     00001310  653+         L     R2,V3_4           get v3
00001332  E732 0000 0006                00000000  654+         VL    V3,0(R2)
00001338  E612 3019 F070                          655+         VPKZR V1,V2,V3,159,1    test instruction
0000133E  E710 8F00 000E                00001100  656+         VST   V1,V1OUTPUT       save result
00001344  B98D 0020                               657+         EPSW  R2,R0             exptract psw
00001348  5020 8EE4                     000010E4  658+         ST    R2,CCPSW              to save CC
0000134C  07FB                                    659+         BR    R11               return
00001350                                          660+RE4      DC    0F
00001350                                          661+         DROP  R5
00001350  00000000 00000000                       662          DC    XL16'000000000000000000000000000123D'    V1
00001358  00000000 0000123D
00001360  F9F0F0F0 F0F0F0F0                       663          DC    XL16'F9F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001368  F0F0F0F0 F0F0F0F0
00001370  F0F0F0F0 F0F0F0F0                       664          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F2D3'    V3
00001378  F0F0F0F0 F0F1F2D3
                                                  665
                                                  666          VRI_F VPKZR,135,1,3          (overflow; rdc=7 )
00001380                                          667+         DS    0FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001380                      00001380             668+         USING *,R5              base for test data and test routine
00001380  000013A4                                 669+T5       DC    A(X5)             address of test routine
00001384  0005                                     670+         DC    H'5'              test number
00001386  00                                       671+         DC    X'00'
00001387  87                                       672+         DC    HL1'135'          i4
00001388  01                                       673+         DC    HL1'1'            m5
00001389  03                                       674+         DC    HL1'3'            cc
0000138A  0E                                       675+         DC    HL1'14'           cc failed mask
0000138C  000013E0                                 676+V2_5     DC    A(RE5+16)         address of v2: 16-byte zoned decimal
00001390  000013F0                                 677+V3_5     DC    A(RE5+32)         address of v3: 16-byte zoned decimal
00001394  E5D7D2E9 D9404040                        678+         DC    CL8'VPKZR'        instruction name
0000139C  00000010                                 679+         DC    A(16)             result length
000013A0  000013D0                                 680+REA5     DC    A(RE5)            result address
                                                   681+*                                INSTRUCTION UNDER TEST ROUTINE
000013A4                                           682+X5       DS    0F
000013A4  5820 500C                    0000138C    683+         L     R2,V2_5           get v2
000013A8  E722 0000 0006               00000000    684+         VL    V2,0(R2)
000013AE  5820 5010                    00001390    685+         L     R2,V3_5           get v3
000013B2  E732 0000 0006               00000000    686+         VL    V3,0(R2)
000013B8  E612 3018 7070                           687+         VPKZR V1,V2,V3,135,1    test instruction
000013BE  E710 8F00 000E               00001100    688+         VST   V1,V1OUTPUT       save result
000013C4  B98D 0020                                689+         EPSW  R2,R0             exptract psw
000013C8  5020 8EE4                    000010E4    690+         ST    R2,CCPSW              to save CC
000013CC  07FB                                     691+         BR    R11               return
000013D0                                           692+RE5      DC    0F
000013D0                                           693+         DROP  R5
000013D0  00000000 00000000                        694          DC    XL16'0000000000000000000000000000123D'    V1
000013D8  00000000 0000123D
000013E0  F0F9F8F7 F0F0F0F0                        695          DC    XL16'F0F9F8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000013E8  F0F0F0F0 F0F0F0F0
000013F0  F0F0F0F0 F0F0F0F0                        696          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F2D3'    V3
000013F8  F0F0F0F0 F0F1F2D3
                                                   697
                                                   698          VRI_F VPKZR,135,1,3           (overflow; rdc=7 )
00001400                                           699+         DS    0FD
00001400                      00001400             700+         USING *,R5              base for test data and test routine
00001400  00001424                                 701+T6       DC    A(X6)             address of test routine
00001404  0006                                     702+         DC    H'6'              test number
00001406  00                                       703+         DC    X'00'
00001407  87                                       704+         DC    HL1'135'          i4
00001408  01                                       705+         DC    HL1'1'            m5
00001409  03                                       706+         DC    HL1'3'            cc
0000140A  0E                                       707+         DC    HL1'14'           cc failed mask
0000140C  00001460                                 708+V2_6     DC    A(RE6+16)         address of v2: 16-byte zoned decimal
00001410  00001470                                 709+V3_6     DC    A(RE6+32)         address of v3: 16-byte zoned decimal
00001414  E5D7D2E9 D9404040                        710+         DC    CL8'VPKZR'        instruction name
0000141C  00000010                                 711+         DC    A(16)             result length
00001420  00001450                                 712+REA6     DC    A(RE6)            result address
                                                   713+*                                INSTRUCTION UNDER TEST ROUTINE
00001424                                           714+X6       DS    0F
00001424  5820 500C                    0000140C    715+         L     R2,V2_6           get v2
00001428  E722 0000 0006               00000000    716+         VL    V2,0(R2)
0000142E  5820 5010                    00001410    717+         L     R2,V3_6           get v3
00001432  E732 0000 0006               00000000    718+         VL    V3,0(R2)
00001438  E612 3018 7070                           719+         VPKZR V1,V2,V3,135,1    test instruction
0000143E  E710 8F00 000E               00001100    720+         VST   V1,V1OUTPUT       save result
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001444  B98D 0020                          721+          EPSW  R2,R0              exptract psw
00001448  5020 8EE4                 000010E4 722+          ST    R2,CCPSW                to save CC
0000144C  07FB                              723+          BR    R11               return
00001450                                    724+RE6       DC    0F
00001450                                    725+          DROP  R5
00001450  00000000 00000000                 726           DC    XL16'0000000000000000000000000000123D'    V1
00001458  00000000 0000123D
00001460  F0F0F0F0 F0F0F0F0                 727           DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001468  F0F0F0F0 F0F0F0F0
00001470  F0F0F0F0 F0F0F0F0                 728           DC    XL16'F0F0F0F0F0F0F0F0F9F0F0F0F0F1F2D3'    V3
00001478  F9F0F0F0 F0F1F2D3
                                            729
                                            730           VRI_F VPKZR,142,1,3          (overflow; rdc=14)
00001480                                    731+          DS    0FD
00001480                    00001480        732+          USING *,R5              base for test data and test routine
00001480  000014A4                          733+T7        DC    A(X7)             address of test routine
00001484  0007                              734+          DC    H'7'              test number
00001486  00                                735+          DC    X'00'
00001487  8E                                736+          DC    HL1'142'          i4
00001488  01                                737+          DC    HL1'1'            m5
00001489  03                                738+          DC    HL1'3'            cc
0000148A  0E                                739+          DC    HL1'14'           cc failed mask
0000148C  000014E0                          740+V2_7      DC    A(RE7+16)         address of v2: 16-byte zoned decimal
00001490  000014F0                          741+V3_7      DC    A(RE7+32)         address of v3: 16-byte zoned decimal
00001494  E5D7D2E9 D9404040                 742+          DC    CL8'VPKZR'        instruction name
0000149C  00000010                          743+          DC    A(16)             result length
000014A0  000014D0                          744+REA7      DC    A(RE7)            result address
                                            745+*                                 INSTRUCTION UNDER TEST ROUTINE
000014A4                                    746+X7        DS    0F
000014A4  5820 500C             0000148C    747+          L     R2,V2_7           get v2
000014A8  E722 0000 0006        00000000    748+          VL    V2,0(R2)
000014AE  5820 5010             00001490    749+          L     R2,V3_7           get v3
000014B2  E732 0000 0006        00000000    750+          VL    V3,0(R2)
000014B8  E612 3018 E070                    751+          VPKZR V1,V2,V3,142,1    test instruction
000014BE  E710 8F00 000E        00001100    752+          VST   V1,V1OUTPUT       save result
000014C4  B98D 0020                         753+          EPSW  R2,R0             exptract psw
000014C8  5020 8EE4             000010E4    754+          ST    R2,CCPSW              to save CC
000014CC  07FB                              755+          BR    R11               return
000014D0                                    756+RE7       DC    0F
000014D0                                    757+          DROP  R5
000014D0  00000000 00000000                 758           DC    XL16'0000000000000000000000090000123D'    V1
000014D8  00000009 0000123D
000014E0  F0F0F0F0 F0F0F0F0                 759           DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F9'    V2
000014E8  F0F0F0F0 F0F0F0F9
000014F0  F0F0F0F0 F0F0F0F0                 760           DC    XL16'F0F0F0F0F0F0F0F0F9F0F0F0F0F1F2D3'    V3
000014F8  F9F0F0F0 F0F1F2D3
                                            761
                                            762 * m5 tests (note: cs is always 1)
                                            763 *                         m5=1   (nsv=0, nv=0, p1=0, cs=1)
                                            764 *                         m5=3   (nsv=0, nv=0, p1=1, cs=1)
                                            765 *                         m5=5   (nsv=0, nv=1, p1=0, cs=1)
                                            766 *                         m5=7   (nsv=0, nv=1, p1=1, cs=1)
                                            767 *                         m5=9   (nsv=1, nv=0, p1=0, cs=1)
                                            768 *                         m5=11  (nsv=1, nv=0, p1=1, cs=1)
                                            769 *                         m5=13  (nsv=1, nv=1, p1=0, cs=1)
                                            770 *                         m5=15  (nsv=1, nv=1, p1=1, cs=1)
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     771
                                                     772          VRI_F VPKZR,159,3,2
00001500                                             773+         DS    0FD
00001500                       00001500              774+         USING *,R5              base for test data and test routine
00001500  00001524                                   775+T8       DC    A(X8)             address of test routine
00001504  0008                                       776+         DC    H'8'              test number
00001506  00                                         777+         DC    X'00'
00001507  9F                                         778+         DC    HL1'159'          i4
00001508  03                                         779+         DC    HL1'3'            m5
00001509  02                                         780+         DC    HL1'2'            cc
0000150A  0D                                         781+         DC    HL1'13'           cc failed mask
0000150C  00001560                                   782+V2_8     DC    A(RE8+16)         address of v2: 16-byte zoned decimal
00001510  00001570                                   783+V3_8     DC    A(RE8+32)         address of v3: 16-byte zoned decimal
00001514  E5D7D2E9 D9404040                          784+         DC    CL8'VPKZR'        instruction name
0000151C  00000010                                   785+         DC    A(16)             result length
00001520  00001550                                   786+REA8     DC    A(RE8)            result address
                                                     787+*                                INSTRUCTION UNDER TEST ROUTINE
00001524                                             788+X8       DS    0F
00001524  5820 500C                    0000150C      789+         L     R2,V2_8           get v2
00001528  E722 0000 0006               00000000      790+         VL    V2,0(R2)
0000152E  5820 5010                    00001510      791+         L     R2,V3_8           get v3
00001532  E732 0000 0006               00000000      792+         VL    V3,0(R2)
00001538  E612 3039 F070                             793+         VPKZR V1,V2,V3,159,3    test instruction
0000153E  E710 8F00 000E               00001100      794+         VST   V1,V1OUTPUT       save result
00001544  B98D 0020                                  795+         EPSW  R2,R0             exptract psw
00001548  5020 8EE4                    000010E4      796+         ST    R2,CCPSW              to save CC
0000154C  07FB                                       797+         BR    R11               return
00001550                                             798+RE8      DC    0F
00001550                                             799+         DROP  R5
00001550  00000000 00000000                          800          DC    XL16'0000000000000000000000000000022F'    V1
00001558  00000000 0000022F
00001560  F0F0F0F0 F0F0F0F0                          801          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001568  F0F0F0F0 F0F0F0F0
00001570  F0F0F0F0 F0F0F0F0                          802          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F2C2'    V3
00001578  F0F0F0F0 F0F0F2C2
                                                     803
                                                     804          VRI_F VPKZR,159,3,2           p1=1
00001580                                             805+         DS    0FD
00001580                       00001580              806+         USING *,R5              base for test data and test routine
00001580  000015A4                                   807+T9       DC    A(X9)             address of test routine
00001584  0009                                       808+         DC    H'9'              test number
00001586  00                                         809+         DC    X'00'
00001587  9F                                         810+         DC    HL1'159'          i4
00001588  03                                         811+         DC    HL1'3'            m5
00001589  02                                         812+         DC    HL1'2'            cc
0000158A  0D                                         813+         DC    HL1'13'           cc failed mask
0000158C  000015E0                                   814+V2_9     DC    A(RE9+16)         address of v2: 16-byte zoned decimal
00001590  000015F0                                   815+V3_9     DC    A(RE9+32)         address of v3: 16-byte zoned decimal
00001594  E5D7D2E9 D9404040                          816+         DC    CL8'VPKZR'        instruction name
0000159C  00000010                                   817+         DC    A(16)             result length
000015A0  000015D0                                   818+REA9     DC    A(RE9)            result address
                                                     819+*                                INSTRUCTION UNDER TEST ROUTINE
000015A4                                             820+X9       DS    0F
000015A4  5820 500C                    0000158C      821+         L     R2,V2_9           get v2
000015A8  E722 0000 0006               00000000      822+         VL    V2,0(R2)
000015AE  5820 5010                    00001590      823+         L     R2,V3_9           get v3
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000015B2  E732 0000 0006                 00000000   824+         VL    V3,0(R2)
000015B8  E612 3039 F070                            825+         VPKZR V1,V2,V3,159,3    test instruction
000015BE  E710 8F00 000E                 00001100   826+         VST   V1,V1OUTPUT       save result
000015C4  B98D 0020                                 827+         EPSW  R2,R0             exptract psw
000015C8  5020 8EE4                      000010E4   828+         ST    R2,CCPSW              to save CC
000015CC  07FB                                      829+         BR    R11               return
000015D0                                            830+RE9      DC    0F
000015D0                                            831+         DROP  R5
000015D0  98700000 00000000                         832          DC    XL16'9870000000000000000000000000123F'    V1
000015D8  00000000 0000123F
000015E0  F0F9F8F7 F0F0F0F0                         833          DC    XL16'F0F9F8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000015E8  F0F0F0F0 F0F0F0F0
000015F0  F0F0F0F0 F0F0F0F0                         834          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F2D3'    V3
000015F8  F0F0F0F0 F0F1F2D3
                                                    835
                                                    836          VRI_F VPKZR,159,5,3           nv=1 & invalid sign
00001600                                            837+         DS    0FD
00001600                         00001600           838+         USING *,R5              base for test data and test routine
00001600  00001624                                  839+T10      DC    A(X10)            address of test routine
00001604  000A                                      840+         DC    H'10'             test number
00001606  00                                        841+         DC    X'00'
00001607  9F                                        842+         DC    HL1'159'          i4
00001608  05                                        843+         DC    HL1'5'            m5
00001609  03                                        844+         DC    HL1'3'            cc
0000160A  0E                                        845+         DC    HL1'14'           cc failed mask
0000160C  00001660                                  846+V2_10    DC    A(RE10+16)        address of v2: 16-byte zoned decimal
00001610  00001670                                  847+V3_10    DC    A(RE10+32)        address of v3: 16-byte zoned decimal
00001614  E5D7D2E9 D9404040                         848+         DC    CL8'VPKZR'        instruction name
0000161C  00000010                                  849+         DC    A(16)             result length
00001620  00001650                                  850+REA10    DC    A(RE10)           result address
                                                    851+*                                INSTRUCTION UNDER TEST ROUTINE
00001624                                            852+X10      DS    0F
00001624  5820 500C                      0000160C   853+         L     R2,V2_10          get v2
00001628  E722 0000 0006                 00000000   854+         VL    V2,0(R2)
0000162E  5820 5010                      00001610   855+         L     R2,V3_10          get v3
00001632  E732 0000 0006                 00000000   856+         VL    V3,0(R2)
00001638  E612 3059 F070                            857+         VPKZR V1,V2,V3,159,5    test instruction
0000163E  E710 8F00 000E                 00001100   858+         VST   V1,V1OUTPUT       save result
00001644  B98D 0020                                 859+         EPSW  R2,R0             exptract psw
00001648  5020 8EE4                      000010E4   860+         ST    R2,CCPSW              to save CC
0000164C  07FB                                      861+         BR    R11               return
00001650                                            862+RE10     DC    0F
00001650                                            863+         DROP  R5
00001650  00000000 00000000                         864          DC    XL16'00000000000000000000000000000229'    V1
00001658  00000000 00000229
00001660  F0F0F0F0 F0F0F0F0                         865          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001668  F0F0F0F0 F0F0F0F0
00001670  F0F0F0F0 F0F0F0F0                         866          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F292'    V3
00001678  F0F0F0F0 F0F0F292
                                                    867
                                                    868          VRI_F VPKZR,159,5,3           nv=1 & invalid digit
00001680                                            869+         DS    0FD
00001680                         00001680           870+         USING *,R5              base for test data and test routine
00001680  000016A4                                  871+T11      DC    A(X11)            address of test routine
00001684  000B                                      872+         DC    H'11'             test number
00001686  00                                        873+         DC    X'00'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001687  9F                                        874+          DC    HL1'159'          i4
00001688  05                                        875+          DC    HL1'5'            m5
00001689  03                                        876+          DC    HL1'3'            cc
0000168A  0E                                        877+          DC    HL1'14'           cc failed mask
0000168C  000016E0                                  878+V2_11     DC    A(RE11+16)        address of v2: 16-byte zoned decimal
00001690  000016F0                                  879+V3_11     DC    A(RE11+32)        address of v3: 16-byte zoned decimal
00001694  E5D7D2E9 D9404040                         880+          DC    CL8'VPKZR'        instruction name
0000169C  00000010                                  881+          DC    A(16)             result length
000016A0  000016D0                                  882+REA11     DC    A(RE11)           result address
                                                    883+*                                 INSTRUCTION UNDER TEST ROUTINE
000016A4                                            884+X11       DS    0F
000016A4  5820 500C                       0000168C  885+          L     R2,V2_11          get v2
000016A8  E722 0000 0006                  00000000  886+          VL    V2,0(R2)
000016AE  5820 5010                       00001690  887+          L     R2,V3_11          get v3
000016B2  E732 0000 0006                  00000000  888+          VL    V3,0(R2)
000016B8  E612 3059 F070                            889+          VPKZR V1,V2,V3,159,5    test instruction
000016BE  E710 8F00 000E                  00001100  890+          VST   V1,V1OUTPUT       save result
000016C4  B98D 0020                                 891+          EPSW  R2,R0             exptract psw
000016C8  5020 8EE4                       000010E4  892+          ST    R2,CCPSW              to save CC
000016CC  07FB                                      893+          BR    R11               return
000016D0                                            894+RE11      DC    0F
000016D0                                            895+          DROP  R5
000016D0  F0000000 00000000                         896           DC    XL16'F0000000000000000000000000000229'    V1
000016D8  00000000 00000229
000016E0  F0FFF0F0 F0F0F0F0                         897           DC    XL16'F0FFF0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000016E8  F0F0F0F0 F0F0F0F0
000016F0  F0F0F0F0 F0F0F0F0                         898           DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F292'    V3
000016F8  F0F0F0F0 F0F0F292
                                                    899
                                                    900           VRI_F VPKZR,159,7,3           nv=1, p1=1 & invalid digit
00001700                                            901+          DS    0FD
00001700                        00001700            902+          USING *,R5              base for test data and test routine
00001700  00001724                                  903+T12       DC    A(X12)            address of test routine
00001704  000C                                      904+          DC    H'12'             test number
00001706  00                                        905+          DC    X'00'
00001707  9F                                        906+          DC    HL1'159'          i4
00001708  07                                        907+          DC    HL1'7'            m5
00001709  03                                        908+          DC    HL1'3'            cc
0000170A  0E                                        909+          DC    HL1'14'           cc failed mask
0000170C  00001760                                  910+V2_12     DC    A(RE12+16)        address of v2: 16-byte zoned decimal
00001710  00001770                                  911+V3_12     DC    A(RE12+32)        address of v3: 16-byte zoned decimal
00001714  E5D7D2E9 D9404040                         912+          DC    CL8'VPKZR'        instruction name
0000171C  00000010                                  913+          DC    A(16)             result length
00001720  00001750                                  914+REA12     DC    A(RE12)           result address
                                                    915+*                                 INSTRUCTION UNDER TEST ROUTINE
00001724                                            916+X12       DS    0F
00001724  5820 500C                       0000170C  917+          L     R2,V2_12          get v2
00001728  E722 0000 0006                  00000000  918+          VL    V2,0(R2)
0000172E  5820 5010                       00001710  919+          L     R2,V3_12          get v3
00001732  E732 0000 0006                  00000000  920+          VL    V3,0(R2)
00001738  E612 3079 F070                            921+          VPKZR V1,V2,V3,159,7    test instruction
0000173E  E710 8F00 000E                  00001100  922+          VST   V1,V1OUTPUT       save result
00001744  B98D 0020                                 923+          EPSW  R2,R0             exptract psw
00001748  5020 8EE4                       000010E4  924+          ST    R2,CCPSW              to save CC
0000174C  07FB                                      925+          BR    R11               return
00001750                                            926+RE12      DC    0F
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001750                                             927+         DROP  R5
00001750  F8700000 00000000                          928          DC    XL16'F870000000000000000000000000123F'    V1
00001758  00000000 0000123F
00001760  F0FFF8F7 F0F0F0F0                          929          DC    XL16'F0FFF8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001768  F0F0F0F0 F0F0F0F0
00001770  F0F0F0F0 F0F0F0F0                          930          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F2D3'    V3
00001778  F0F0F0F0 F0F1F2D3
                                                     931
                                                     932          VRI_F VPKZR,159,9,3            nsv=1 & invalid sign
00001780                                             933+         DS    0FD
00001780                          00001780           934+         USING *,R5              base for test data and test routine
00001780  000017A4                                   935+T13      DC    A(X13)            address of test routine
00001784  000D                                       936+         DC    H'13'             test number
00001786  00                                         937+         DC    X'00'
00001787  9F                                         938+         DC    HL1'159'          i4
00001788  09                                         939+         DC    HL1'9'            m5
00001789  03                                         940+         DC    HL1'3'            cc
0000178A  0E                                         941+         DC    HL1'14'           cc failed mask
0000178C  000017E0                                   942+V2_13    DC    A(RE13+16)        address of v2: 16-byte zoned decimal
00001790  000017F0                                   943+V3_13    DC    A(RE13+32)        address of v3: 16-byte zoned decimal
00001794  E5D7D2E9 D9404040                          944+         DC    CL8'VPKZR'        instruction name
0000179C  00000010                                   945+         DC    A(16)             result length
000017A0  000017D0                                   946+REA13    DC    A(RE13)           result address
                                                     947+*                                INSTRUCTION UNDER TEST ROUTINE
000017A4                                             948+X13      DS    0F
000017A4  5820 500C                    0000178C      949+         L     R2,V2_13          get v2
000017A8  E722 0000 0006               00000000      950+         VL    V2,0(R2)
000017AE  5820 5010                    00001790      951+         L     R2,V3_13          get v3
000017B2  E732 0000 0006               00000000      952+         VL    V3,0(R2)
000017B8  E612 3099 F070                             953+         VPKZR V1,V2,V3,159,9    test instruction
000017BE  E710 8F00 000E               00001100      954+         VST   V1,V1OUTPUT       save result
000017C4  B98D 0020                                  955+         EPSW  R2,R0             exptract psw
000017C8  5020 8EE4                    000010E4      956+         ST    R2,CCPSW              to save CC
000017CC  07FB                                       957+         BR    R11               return
000017D0                                             958+RE13     DC    0F
000017D0                                             959+         DROP  R5
000017D0  00000000 00000000                          960          DC    XL16'00000000000000000000000000000229'    V1
000017D8  00000000 00000229
000017E0  F0F0F0F0 F0F0F0F0                          961          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000017E8  F0F0F0F0 F0F0F0F0
000017F0  F0F0F0F0 F0F0F0F0                          962          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F0F292'    V3
000017F8  F0F0F0F0 F0F0F292
                                                     963
                                                     964          VRI_F VPKZR,159,11,3           nsv=1, p1=1 & invalid sign
00001800                                             965+         DS    0FD
00001800                          00001800           966+         USING *,R5              base for test data and test routine
00001800  00001824                                   967+T14      DC    A(X14)            address of test routine
00001804  000E                                       968+         DC    H'14'             test number
00001806  00                                         969+         DC    X'00'
00001807  9F                                         970+         DC    HL1'159'          i4
00001808  0B                                         971+         DC    HL1'11'           m5
00001809  03                                         972+         DC    HL1'3'            cc
0000180A  0E                                         973+         DC    HL1'14'           cc failed mask
0000180C  00001860                                   974+V2_14    DC    A(RE14+16)        address of v2: 16-byte zoned decimal
00001810  00001870                                   975+V3_14    DC    A(RE14+32)        address of v3: 16-byte zoned decimal
00001814  E5D7D2E9 D9404040                          976+         DC    CL8'VPKZR'        instruction name
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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000181C  00000010                            977+         DC    A(16)              result length
00001820  00001850                            978+REA14    DC    A(RE14)            result address
                                              979+*                                 INSTRUCTION UNDER TEST ROUTINE
00001824                                      980+X14      DS    0F
00001824  5820 500C                 0000180C  981+         L     R2,V2_14           get v2
00001828  E722 0000 0006            00000000  982+         VL    V2,0(R2)
0000182E  5820 5010                 00001810  983+         L     R2,V3_14           get v3
00001832  E732 0000 0006            00000000  984+         VL    V3,0(R2)
00001838  E612 30B9 F070                      985+         VPKZR V1,V2,V3,159,11    test instruction
0000183E  E710 8F00 000E            00001100  986+         VST   V1,V1OUTPUT        save result
00001844  B98D 0020                           987+         EPSW  R2,R0              exptract psw
00001848  5020 8EE4                 000010E4  988+         ST    R2,CCPSW               to save CC
0000184C  07FB                                989+         BR    R11                return
00001850                                      990+RE14     DC    0F
00001850                                      991+         DROP  R5
00001850  98700000 00000000                   992          DC    XL16'9870000000000000000000000000123F'    V1
00001858  00000000 0000123F
00001860  F0F9F8F7 F0F0F0F0                   993          DC    XL16'F0F9F8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001868  F0F0F0F0 F0F0F0F0
00001870  F0F0F0F0 F0F0F0F0                   994          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F293'    V3
00001878  F0F0F0F0 F0F1F293
                                              995
                                              996          VRI_F VPKZR,159,13,3   nsv=1, nv=1, p1=0 & invalid sign/digit
00001880                                      997+         DS    0FD
00001880                    00001880          998+         USING *,R5             base for test data and test routine
00001880  000018A4                            999+T15      DC    A(X15)             address of test routine
00001884  000F                                1000+        DC    H'15'              test number
00001886  00                                  1001+        DC    X'00'
00001887  9F                                  1002+        DC    HL1'159'           i4
00001888  0D                                  1003+        DC    HL1'13'            m5
00001889  03                                  1004+        DC    HL1'3'             cc
0000188A  0E                                  1005+        DC    HL1'14'            cc failed mask
0000188C  000018E0                            1006+V2_15   DC    A(RE15+16)         address of v2: 16-byte zoned decimal
00001890  000018F0                            1007+V3_15   DC    A(RE15+32)         address of v3: 16-byte zoned decimal
00001894  E5D7D2E9 D9404040                   1008+        DC    CL8'VPKZR'         instruction name
0000189C  00000010                            1009+        DC    A(16)              result length
000018A0  000018D0                            1010+REA15   DC    A(RE15)            result address
                                              1011+*                                INSTRUCTION UNDER TEST ROUTINE
000018A4                                      1012+X15     DS    0F
000018A4  5820 500C                 0000188C  1013+        L     R2,V2_15           get v2
000018A8  E722 0000 0006            00000000  1014+        VL    V2,0(R2)
000018AE  5820 5010                 00001890  1015+        L     R2,V3_15           get v3
000018B2  E732 0000 0006            00000000  1016+        VL    V3,0(R2)
000018B8  E612 30D9 F070                      1017+        VPKZR V1,V2,V3,159,13    test instruction
000018BE  E710 8F00 000E            00001100  1018+        VST   V1,V1OUTPUT        save result
000018C4  B98D 0020                           1019+        EPSW  R2,R0              exptract psw
000018C8  5020 8EE4                 000010E4  1020+        ST    R2,CCPSW               to save CC
000018CC  07FB                                1021+        BR    R11                return
000018D0                                      1022+RE15    DC    0F
000018D0                                      1023+        DROP  R5
000018D0  F8700000 00000000                   1024         DC    XL16'F870000000000000000000000001239'    V1
000018D8  00000000 00001239
000018E0  F0FFF8F7 F0F0F0F0                   1025         DC    XL16'F0FFF8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
000018E8  F0F0F0F0 F0F0F0F0
000018F0  F0F0F0F0 F0F0F0F0                   1026         DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F293'    V3
000018F8  F0F0F0F0 F0F1F293
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1027
                                                    1028          VRI_F VPKZR,159,15,3   nsv=1, nv=1, p1=1 & invalid sign/digit
00001900                                            1029+         DS    0FD
00001900                      00001900              1030+         USING *,R5              base for test data and test routine
00001900  00001924                                  1031+T16      DC    A(X16)            address of test routine
00001904  0010                                      1032+         DC    H'16'             test number
00001906  00                                        1033+         DC    X'00'
00001907  9F                                        1034+         DC    HL1'159'          i4
00001908  0F                                        1035+         DC    HL1'15'           m5
00001909  03                                        1036+         DC    HL1'3'            cc
0000190A  0E                                        1037+         DC    HL1'14'           cc failed mask
0000190C  00001960                                  1038+V2_16    DC    A(RE16+16)        address of v2: 16-byte zoned decimal
00001910  00001970                                  1039+V3_16    DC    A(RE16+32)        address of v3: 16-byte zoned decimal
00001914  E5D7D2E9 D9404040                         1040+         DC    CL8'VPKZR'        instruction name
0000191C  00000010                                  1041+         DC    A(16)             result length
00001920  00001950                                  1042+REA16    DC    A(RE16)           result address
                                                    1043+*                                INSTRUCTION UNDER TEST ROUTINE
00001924                                            1044+X16      DS    0F
00001924  5820 500C                     0000190C    1045+         L     R2,V2_16          get v2
00001928  E722 0000 0006                00000000    1046+         VL    V2,0(R2)
0000192E  5820 5010                     00001910    1047+         L     R2,V3_16          get v3
00001932  E732 0000 0006                00000000    1048+         VL    V3,0(R2)
00001938  E612 30F9 F070                            1049+         VPKZR V1,V2,V3,159,15   test instruction
0000193E  E710 8F00 000E                00001100    1050+         VST   V1,V1OUTPUT       save result
00001944  B98D 0020                                 1051+         EPSW  R2,R0             exptract psw
00001948  5020 8EE4                     000010E4    1052+         ST    R2,CCPSW              to save CC
0000194C  07FB                                      1053+         BR    R11               return
00001950                                            1054+RE16     DC    0F
00001950                                            1055+         DROP  R5
00001950  F8700000 00000000                         1056          DC    XL16'F87000000000000000000000000123F'    V1
00001958  00000000 0000123F
00001960  F0FFF8F7 F0F0F0F0                         1057          DC    XL16'F0FFF8F7F0F0F0F0F0F0F0F0F0F0F0F0'    V2
00001968  F0F0F0F0 F0F0F0F0
00001970  F0F0F0F0 F0F0F0F0                         1058          DC    XL16'F0F0F0F0F0F0F0F0F0F0F0F0F0F1F293'    V3
00001978  F0F0F0F0 F0F1F293
                                                    1059
00001980  00000000                                  1060          DC    F'0'     END OF TABLE
00001984  00000000                                  1061          DC    F'0'
                                                    1062 *
                                                    1063 * table of pointers to individual load test
                                                    1064 *
00001988                                            1065 E6TESTS  DS    0F
                                                    1066          PTTABLE
00001988                                            1067+TTABLE   DS    0F
00001988  00001180                                  1068+         DC    A(T1)             address of test
0000198C  00001200                                  1069+         DC    A(T2)             address of test
00001990  00001280                                  1070+         DC    A(T3)             address of test
00001994  00001300                                  1071+         DC    A(T4)             address of test
00001998  00001380                                  1072+         DC    A(T5)             address of test
0000199C  00001400                                  1073+         DC    A(T6)             address of test
000019A0  00001480                                  1074+         DC    A(T7)             address of test
000019A4  00001500                                  1075+         DC    A(T8)             address of test
000019A8  00001580                                  1076+         DC    A(T9)             address of test
000019AC  00001600                                  1077+         DC    A(T10)            address of test
000019B0  00001680                                  1078+         DC    A(T11)            address of test
000019B4  00001700                                  1079+         DC    A(T12)            address of test
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019B8  00001780                             1080+          DC    A(T13)            address of test
000019BC  00001800                             1081+          DC    A(T14)            address of test
000019C0  00001880                             1082+          DC    A(T15)            address of test
000019C4  00001900                             1083+          DC    A(T16)            address of test
                                               1084+*
000019C8  00000000                             1085+          DC    A(0)              END OF TABLE
000019CC  00000000                             1086+          DC    A(0)
                                               1087
000019D0  00000000                             1088           DC    F'0'     END OF TABLE
000019D4  00000000                             1089           DC    F'0'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                                          1091 ************************************************************************
                                          1092 *        Register equates
                                          1093 ************************************************************************


                              00000000  00000001  1095 R0       EQU   0
                              00000001  00000001  1096 R1       EQU   1
                              00000002  00000001  1097 R2       EQU   2
                              00000003  00000001  1098 R3       EQU   3
                              00000004  00000001  1099 R4       EQU   4
                              00000005  00000001  1100 R5       EQU   5
                              00000006  00000001  1101 R6       EQU   6
                              00000007  00000001  1102 R7       EQU   7
                              00000008  00000001  1103 R8       EQU   8
                              00000009  00000001  1104 R9       EQU   9
                              0000000A  00000001  1105 R10      EQU   10
                              0000000B  00000001  1106 R11      EQU   11
                              0000000C  00000001  1107 R12      EQU   12
                              0000000D  00000001  1108 R13      EQU   13
                              0000000E  00000001  1109 R14      EQU   14
                              0000000F  00000001  1110 R15      EQU   15


                                          1112 ************************************************************************
                                          1113 *        Register equates
                                          1114 ************************************************************************


                              00000000  00000001  1116 V0       EQU   0
                              00000001  00000001  1117 V1       EQU   1
                              00000002  00000001  1118 V2       EQU   2
                              00000003  00000001  1119 V3       EQU   3
                              00000004  00000001  1120 V4       EQU   4
                              00000005  00000001  1121 V5       EQU   5
                              00000006  00000001  1122 V6       EQU   6
                              00000007  00000001  1123 V7       EQU   7
                              00000008  00000001  1124 V8       EQU   8
                              00000009  00000001  1125 V9       EQU   9
                              0000000A  00000001  1126 V10      EQU   10
                              0000000B  00000001  1127 V11      EQU   11
                              0000000C  00000001  1128 V12      EQU   12
                              0000000D  00000001  1129 V13      EQU   13
                              0000000E  00000001  1130 V14      EQU   14
                              0000000F  00000001  1131 V15      EQU   15
                              00000010  00000001  1132 V16      EQU   16
                              00000011  00000001  1133 V17      EQU   17
                              00000012  00000001  1134 V18      EQU   18
                              00000013  00000001  1135 V19      EQU   19
                              00000014  00000001  1136 V20      EQU   20
                              00000015  00000001  1137 V21      EQU   21
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT
                                                     1138 V22       EQU   22
                                 00000016  00000001  1139 V23       EQU   23
                                 00000017  00000001  1140 V24       EQU   24
                                 00000018  00000001  1141 V25       EQU   25
                                 00000019  00000001  1142 V26       EQU   26
                                 0000001A  00000001  1143 V27       EQU   27
                                 0000001B  00000001  1144 V28       EQU   28
                                 0000001C  00000001  1145 V29       EQU   29
                                 0000001D  00000001  1146 V30       EQU   30
                                 0000001E  00000001  1147 V31       EQU   31
                                 0000001F  00000001  1148
                                                     1149           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	91	57 88 89
CC	U	00000009	1	418	165
CCFOUND	X	000010EC	1	391	152 172
CCMASK	U	0000000A	1	419	124
CCMSG	U	0000026E	1	141	136
CCPRTEXP	C	00001093	1	371	169
CCPRTGOT	C	000010A3	1	374	176
CCPRTLINE	C	00001050	16	366	376 179
CCPRTLNG	U	00000055	1	376	178
CCPRTNAME	C	0000107D	8	369	162
CCPRTNUM	C	00001060	3	367	160
CCPSW	F	000010E4	4	390	149 562 594 626 658 690 722 754 796 828 860 892 924 956 988 1020 1052
CTLR0	F	000004A4	4	311	101 102 103 104
DECNUM	C	000010D1	16	386	157 159 166 168 173 175 191 193 200 202 207 209
E6TADR	A	000004AC	4	314	110
E6TEST	4	00000000	36	412	119
E6TESTS	F	00001988	4	1065	314
EDIT	X	000010A5	18	381	158 167 174 192 201 208
ENDTEST	U	00000376	1	229	115
EOJ	I	00000488	4	301	232
EOJPSW	D	00000478	8	299	301
FAILCONT	U	00000366	1	219	182
FAILED	F	00001000	4	340	221 230
FAILMSG	U	000002FE	1	189	131
FAILPSW	D	00000490	8	303	305
FAILTEST	I	000004A0	4	305	233
I4	U	00000007	1	416	199
IMAGE	1	00000000	6616	0	
K	U	00000400	1	324	325 326 327
K64	U	00010000	1	326	
M5	U	00000008	1	417	143 206
MB	U	00100000	1	327	
MSG	I	000003C0	4	265	248
MSGCMD	C	0000040A	9	291	278 279
MSGMSG	C	00000413	95	292	272 289 270
MSGMVC	I	00000404	6	289	276
MSGOK	I	000003D6	2	274	271
MSGRET	I	000003F0	4	285	282
MSGSAVE	F	000003F8	4	288	268 285
NEXTE6	U	0000022A	1	112	134 224
OPNAME	C	00000014	8	424	162 196
PAGE	U	00001000	1	325	
PRT3	C	000010BB	18	384	158 159 160 167 168 169 174 175 176 192 193 194 201 202 203 208 209 210
PRTI4	C	00001040	3	353	203
PRTLINE	C	00001004	16	348	358 213
PRTLNG	U	0000004C	1	358	212
PRTM5	C	0000104D	2	356	210
PRTNAME	C	0000102F	8	351	196
PRTNUM	C	00001014	3	349	194
R0	U	00000000	1	1095	51 101 104 117 178 212 220 221 247 249 265 268 270 272 274 285 561 593 625 657 689 721 753 795 827 859 891 923 955 987 1019 1051
R1	U	00000001	1	1096	124 125 126 129 130 142 143 144 149 150 151 152 179 213 230 231 279 289

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
R10	U	0000000A	1	1105	98 99
R11	U	0000000B	1	1106	121 122 563 595 627 659 691 723 755 797 829 861 893 925 957 989 1021 1053
R12	U	0000000C	1	1107	110 113 133 223
R13	U	0000000D	1	1108	
R14	U	0000000E	1	1109	
R15	U	0000000F	1	1110	180 214 242 252 253
R2	U	00000002	1	1097	156 157 164 165 166 171 172 173 190 191 198 199 200 205 206 207 247 248 249 266 268 274 275 276 278 285 286 555 556 557 558 561 562 587 588 589 590 593 594 619 620 621 622 625 626 651 652 653 654 657 658 683 684 685 686 689 690 715 716 717 718 721 722 747 748 749 750 753 754 789 790 791 792 795 796 821 822 823 824 827 828 853 854 855 856 859 860 885 886 887 888 891 892 917 918 919 920 923 924 949 950 951 952 955 956 981 982 983 984 987 988 1013 1014 1015 1016 1019 1020 1045 1046 1047 1048 1051 1052
R3	U	00000003	1	1098	
R4	U	00000004	1	1099	
R5	U	00000005	1	1100	113 114 119 243 251 540 565 572 597 604 629 636 661 668 693 700 725 732 757 774 799 806 831 838 863 870 895 902 927 934 959 966 991 998 1023 1030 1055
R6	U	00000006	1	1101	
R7	U	00000007	1	1102	
R8	U	00000008	1	1103	88 91 92 93 95
R9	U	00000009	1	1104	89 95 96 98
RE1	F	000011D0	4	564	548 549 552
RE10	F	00001650	4	862	846 847 850
RE11	F	000016D0	4	894	878 879 882
RE12	F	00001750	4	926	910 911 914
RE13	F	000017D0	4	958	942 943 946
RE14	F	00001850	4	990	974 975 978
RE15	F	000018D0	4	1022	1006 1007 1010
RE16	F	00001950	4	1054	1038 1039 1042
RE2	F	00001250	4	596	580 581 584
RE3	F	000012D0	4	628	612 613 616
RE4	F	00001350	4	660	644 645 648
RE5	F	000013D0	4	692	676 677 680
RE6	F	00001450	4	724	708 709 712
RE7	F	000014D0	4	756	740 741 744
RE8	F	00001550	4	798	782 783 786
RE9	F	000015D0	4	830	814 815 818
REA1	A	000011A0	4	552	
REA10	A	00001620	4	850	
REA11	A	000016A0	4	882	
REA12	A	00001720	4	914	
REA13	A	000017A0	4	946	
REA14	A	00001820	4	978	
REA15	A	000018A0	4	1010	
REA16	A	00001920	4	1042	
REA2	A	00001220	4	584	
REA3	A	000012A0	4	616	
REA4	A	00001320	4	648	
REA5	A	000013A0	4	680	
REA6	A	00001420	4	712	
REA7	A	000014A0	4	744	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA8	A	00001520	4	786	
REA9	A	000015A0	4	818	
READDR	A	00000020	4	427	129
REG2LOW	U	000000DD	1	330	
REG2PATT	U	AABBCCDD	1	329	
RELEN	A	0000001C	4	426	
RPTDWSAV	D	000003B0	8	258	247 249
RPTERROR	I	00000384	4	242	180 214
RPTSAVE	F	000003A4	4	255	242 252
RPTSVR5	F	000003A8	4	256	243 251
SVOLDPSW	U	00000140	0	53	
T1	A	00001180	4	541	1068
T10	A	00001600	4	839	1077
T11	A	00001680	4	871	1078
T12	A	00001700	4	903	1079
T13	A	00001780	4	935	1080
T14	A	00001800	4	967	1081
T15	A	00001880	4	999	1082
T16	A	00001900	4	1031	1083
T2	A	00001200	4	573	1069
T3	A	00001280	4	605	1070
T4	A	00001300	4	637	1071
T5	A	00001380	4	669	1072
T6	A	00001400	4	701	1073
T7	A	00001480	4	733	1074
T8	A	00001500	4	775	1075
T9	A	00001580	4	807	1076
TESTCC	I	0000026A	4	136	126
TESTREST	U	00000252	1	128	145
TNUM	H	00000004	2	414	156 190
TSUB	A	00000000	4	413	121
TTABLE	F	00001988	4	1067	
V0	U	00000000	1	1116	
V1	U	00000001	1	1117	120 559 560 591 592 623 624 655 656 687 688 719 720 751 752 793 794 825 826 857 858 889 890 921 922 953 954 985 986 1017 1018 1049 1050
V10	U	0000000A	1	1126	
V11	U	0000000B	1	1127	
V12	U	0000000C	1	1128	
V13	U	0000000D	1	1129	
V14	U	0000000E	1	1130	
V15	U	0000000F	1	1131	
V16	U	00000010	1	1132	
V17	U	00000011	1	1133	
V18	U	00000012	1	1134	
V19	U	00000013	1	1135	
V1FUDGE	X	00001120	16	400	120
V1INPUT	C	00001130	16	401	
V1OUTPUT	X	00001100	16	398	130 560 592 624 656 688 720 752 794 826 858 890 922 954 986 1018 1050
V2	U	00000002	1	1118	556 559 588 591 620 623 652 655 684 687 716 719 748 751 790 793 822 825 854 857 886 889 918 921 950 953 982 985 1014 1017 1046 1049
V20	U	00000014	1	1136	
V21	U	00000015	1	1137	
V22	U	00000016	1	1138	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V23	U	00000017	1	1139	
V24	U	00000018	1	1140	
V25	U	00000019	1	1141	
V26	U	0000001A	1	1142	
V27	U	0000001B	1	1143	
V28	U	0000001C	1	1144	
V29	U	0000001D	1	1145	
V2PACKED	X	0000114F	16	404	
V2VALUE	A	0000000C	4	421	
V2_1	A	0000118C	4	548	555
V2_10	A	0000160C	4	846	853
V2_11	A	0000168C	4	878	885
V2_12	A	0000170C	4	910	917
V2_13	A	0000178C	4	942	949
V2_14	A	0000180C	4	974	981
V2_15	A	0000188C	4	1006	1013
V2_16	A	0000190C	4	1038	1045
V2_2	A	0000120C	4	580	587
V2_3	A	0000128C	4	612	619
V2_4	A	0000130C	4	644	651
V2_5	A	0000138C	4	676	683
V2_6	A	0000140C	4	708	715
V2_7	A	0000148C	4	740	747
V2_8	A	0000150C	4	782	789
V2_9	A	0000158C	4	814	821
V3	U	00000003	1	1119	558 559 590 591 622 623 654 655 686 687 718 719 750 751 792 793 824 825 856 857 888 889 920 921 952 953 984 985 1016 1017 1048 1049
V30	U	0000001E	1	1146	
V31	U	0000001F	1	1147	
V3PACKED	X	0000115F	16	405	
V3VALUE	A	00000010	4	422	
V3_1	A	00001190	4	549	557
V3_10	A	00001610	4	847	855
V3_11	A	00001690	4	879	887
V3_12	A	00001710	4	911	919
V3_13	A	00001790	4	943	951
V3_14	A	00001810	4	975	983
V3_15	A	00001890	4	1007	1015
V3_16	A	00001910	4	1039	1047
V3_2	A	00001210	4	581	589
V3_3	A	00001290	4	613	621
V3_4	A	00001310	4	645	653
V3_5	A	00001390	4	677	685
V3_6	A	00001410	4	709	717
V3_7	A	00001490	4	741	749
V3_8	A	00001510	4	783	791
V3_9	A	00001590	4	815	823
V4	U	00000004	1	1120	
V5	U	00000005	1	1121	
V6	U	00000006	1	1122	
V7	U	00000007	1	1123	
V8	U	00000008	1	1124	
V9	U	00000009	1	1125	
X1	F	000011A4	4	554	541
X10	F	00001624	4	852	839

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X11	F	000016A4	4	884	871
X12	F	00001724	4	916	903
X13	F	000017A4	4	948	935
X14	F	00001824	4	980	967
X15	F	000018A4	4	1012	999
X16	F	00001924	4	1044	1031
X2	F	00001224	4	586	573
X3	F	000012A4	4	618	605
X4	F	00001324	4	650	637
X5	F	000013A4	4	682	669
X6	F	00001424	4	714	701
X7	F	000014A4	4	746	733
X8	F	00001524	4	788	775
X9	F	000015A4	4	820	807
ZVE6TST	J	00000000	6616	50	53 55 59 63 339 51
=AL2(L'MSGMSG)	R	000004BA	2	320	270
=F'1'	F	000004B0	4	317	144 220
=H'0'	H	000004B8	2	319	265
=XL4'3'	X	000004B4	4	318	151

```
 MACRO    DEFN   REFERENCES

PTTABLE    495   1066
VRI_F      439    538    570    602    634    666    698    730    772    804    836    868    900    932    964    996   1028
```

```
   DESC      SYMBOL   SIZE      POS         ADDR

Entry: 0

Image       IMAGE    6616   0000-19D7   0000-19D7
  Region             6616   0000-19D7   0000-19D7
    CSECT   ZVE6TST   6616   0000-19D7   0000-19D7
```

```
   STMT                    FILE NAME
1     /devstor/dev/tests/zvector-e6-06-VPKZR.asm

** NO ERRORS FOUND **
```