)C	OBJECT CODE	ADDR1	ADDR2	STMT
				2 **********************
				3 * 4 * Zvector E6 instruction tests for VRI-f encoded:
				5 *
				6 * E671 VAP - VECTOR ADD DECIMAL 7 * E673 VSP - VECTOR SUBTRACT DECIMAL
				8 * E678 VMP - VECTOR MULTIPLY DECIMAL
				9 * E679 VSDP - VECTOR MULTIPLY AND SHIFT DECIMAL 10 * E67A VDP - VECTOR DIVIDE DECIMAL
				11 * E67B VRP - VECTOR REMAINDER DECIMAL
				12 * E67E VSDP - VECTOR SHIFT AND DIVIDE DECIMAL 13 *
				14 * James Wekel June 2024
				15 ************************************
				17 ************************************
				18 * 19 * basic instruction tests
				20 *
				21 ************************************
				23 * packed decimal arithmetic instructions. Exceptions are not tested.
				24 * 25 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				26 * obvious coding errors. None of the tests are thorough. They are
				27 * NOT designed to test all aspects of any of the instructions. 28 *
				29 **********************
				30 * 31 * *Testcase VECTOR E6 VRI-f packed arithmetic instructions
				32 * *
				33 * * Zvector E6 tests for VRI-f encoded packed decimal arithmetic instructions:
				35 * *
				36 * * E671 VAP - VECTOR ADD DECIMAL 37 * * E673 VSP - VECTOR SUBTRACT DECIMAL
				38 * * E678 VMP - VECTOR MULTIPLY DECIMAL
				39 * * E679 VMSP - VECTOR MULTIPLY AND SHIFT DECIMAL 40 * * E67A VDP - VECTOR DIVIDE DECIMAL
				41 * * E67B VRP - VECTOR REMAINDER DECIMAL
				42 * * E67E VSDP - VECTOR SHIFT AND DIVIDE DECIMAL 43 * *
				44 * * #
				45 * * # This tests only the basic function of the instruction. 46 * * # Exceptions are NOT tested.
				47 * * #
				48 * * 49 * mainsize 2
				50 * numcpu 1
				51 * sysclear 52 * archlyl z/Arch
				53 *
				54 * loadcore "\$(testpath)/zvector-e6-05-packarith.core" 0x0 55 *
				56 * diag8cmd enable # (needed for messages to Hercules console)

	0. 7. 0 zvector- e6- (15- раскагі т			- г раске	ed ario	inmetic)	02 Jun 2024 15: 59: 21 Page
LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				58 * 59 *	di ag8c	emd	disable # (reset l	back to default)
				60 *	* Done *****	*****	*************	***********
000000		00000000 00000000	00004EEF	64		START USING	0 ZVE6TST, RO	Low core addressability
		00000140	00000000	65 66 SV	VOLDPSW	EQU	ZVE6TST+X' 140'	z/Arch Supervisor call old PSW
	00000001 80000000	00000000	000001A0	68 69 70		DC	ZVE6TST+X' 1A0' X' 0000000180000000'	z/Architecure RESTART PSW
	0000000 00000200					DC	AD(BEGIN)	
	00020001 80000000 0000000 0000DEAD	000001B0	000001D0	72 73 74		DC	ZVE6TST+X' 1D0' X' 0002000180000000' AD(X' DEAD')	z/Architecure PROGRAM CHECK PSW
0001E0		000001E0	00000200	76 77		ORG	ZVE6TST+X' 200'	Start of actual test program

T 0.0		4 DDD 4	ADDDO	CTDATE			
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				119 ******	****	******	***********
				120 *		Do tests in the	e E6TESTS table
				1~1	****	* * * * * * * * * * * * * * * *	***********
0000226	58C0 82AC		000004AC	122 123	L	R12, E6TADR	get table of test addresses
0000220	JOCO OZNO		000001/10	124	L	WIZ, LOIMDR	get tuble of test dudiesses
		0000022A	0000001	125 NEXTE6	EQU	*	
000022A	5850 C000		0000000	126	L	R5, 0(0, R12)	get test address
000022E 0000230	1255 4780 8176		00000376	127 128	LTR BZ	R5, R5 ENDTEST	have a test? done?
0000230	4700 0170		00000370	129	DL	ENDIESI	done:
0000234	B982 0000			130	XGR	RO, RO	no cc error
000000		0000000		131	HOTNO	FOREGE DE	
0000238 0000238	E710 8F20 0006	0000000	00001120	132 133	VL	E6TEST, R5 V1, V1FUDGE	
000023E	58B0 5000		00001120	133 134	VL I.	R11, TSUB	get address of test routine
0000242	05BB			135	BALR	R11, R11	do test
				136		D.	(0.11
0000244	E310 500A 0076		0000000A	137	LB	R1, CCMASK	(failure CC mask)
000024A 000024E	8910 0004 4410 806A		00000004 0000026A	138 139	SLL EX	R1, 4 R1, TESTCC	(shift to BC instr CC position) fail if
0000×1E	1110 00011		000002011	140	LIZE	WI, ILDICC	1411 11
		00000252	0000001	141 TESTREST		*	
0000252	E310 502C 0014	00001100	0000002C	142	LGF	R1, READDR	get address of expected result
0000258 000025E	D50F 8F00 1000 4770 80FE	00001100	0000000 00002FE	143 144	CLC BNE	V10UTPUT, O(R1) FAILMSG	valid? no, issue failed message
CCCC	IIIO OUIL		O O O O O E I	145	21121		no, ibbue iuiieu mebbuge
0000262	41C0 C004		0000004	146	LA	R12, 4(0, R12)	next test address
0000266	47F0 802A		0000022A	147	В	NEXTE6	
000026A	4700 806E		0000026E	148 149 TESTCC	BC	O, CCMSG	(fail if unexpected condition code)
OUUWUA	1700 000L		OUUUAUL	140 ILDICC	ь	o, combu	(Tall II unexpected condition code)

Return to caller

		301 MSGSAVE	DC	3F' 0'	Registers save area
00000413	00000000	302 MSGMVC	MVC	MSGMSG(0), O(R1)	Executed instruction

*** HERCULES MESSAGE COMMAND *** 0000040A D4E2C7D5 D6C8405C **304 MSGCMD** DC C' MSGNOH * ' 00000413 40404040 40404040 305 MSGMSG DC CL95' ' The message text to be displayed 306

CH

CH

LA

LR

EX

LA

LA

DC

BZ

DC

LM

BR

BNH

LOC

000003C4

000003C6

000003CA

000003CE

000003D2

000003D6

000003D8

000003DA

000003EA

000003EE

000003F0

000003F4

000003C0 4900 82B8

07D2

1820

0620

0000

07F2

000003DE 4120 200A

000003E2 4110 820A

000003E6 83120008

9002 81F8

4900 82BA

47D0 81D6

4100 005F

4420 8204

4780 81F0

9802 81F8

000003F8 00000000 00000000 00000404 D200 8213 1000

OBJECT CODE

ADDR1

ADDR2

000004B8

000003F8

000004BA

000003D6

000005F

00000404

000000A

0000040A

000003F0

000003F8

STM

274 *

275 *

277 278 MSG

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298 MSGRET

287 MSGOK

ASMA Ver.	0. 7. 0 zvector-e6-	05- packari tl	h (Zvector	E6 VR	I-f pack	ed arit	chmetic)	02 Jun 2024 15: 59: 21 Page	9
LOC	OBJECT CODE	ADDR1	ADDR2	STM					
				308 309 310	****** * *****	****** Nornal *****	**************************************	**************************************	
00000478	00020001 80000000			312	E0JPSW	DC	OD' O' , X' 000200	018000000', AD(0)	
00000488	B2B2 8278		00000478	314	EOJ	LPSWE	E0JPSW	Normal completion	
00000490	00020001 80000000			316	FAILPSW	DC	OD' O' , X' 000200	018000000', AD(X'BAD')	
000004A0	B2B2 8290		00000490	318	FAI LTEST	LPSWE	FAILPSW	Abnormal termination	
				320 321 322	****** * ****	****** Worki i *****	**************************************	**************************************	
000004A4	00000000			324	CTLRO	DS	F	CRO	
000004A8				325 326		DS	F		
000004AC	00004D04				E6TADR	DC	A(E6TESTS)	address of E6 test table	
000004B0 000004B0 000004B4	00000001 00000003			329 330 331		LTORG	, =F' 1' =XL4' 3'	Literals pool	
000004B8 000004BA	0000 005F			332 333 334			=H' 0' =AL2(L' MSGMSG)		
				335 336	*	some o	constants		
		00000400 00001000	00000001 00000001	337 338	K PAGE	EQU EQU	1024 (4*K)	One KB Size of one page	
		0001000 0010000	00000001 00000001	339 340	K64	EQU EQU	(64*K) (K*K)	64 KB 1 MB	
		AABBCCDD 000000DD	00000001 00000001		REG2PATT REG2LOW		X' AABBCCDD' X' DD'	Polluted Register pattern (last byte above)	

OC	OBJECT CODE	ADDR1	ADDR2	STMT			
				446 ******			***********
				447 * M 448 *	acros t	o help build test	tables
				449 * V	RI_F Ma	cro to help build	test tables
				450 ****** 451	****** MACRO		**********
				452		&I NST, &V2, &V3, &I4	
				453 . * 454 . *			&INST - VRI-f instruction under test &v2 - binary DW value for V2
				455 .*			&v3 - binary DW value for V3
				456 . * 457 . *			&i4 - i4 field &m5 - m5 field
				458 .* 459 .*			&CC - expected CC
				460	LCLA	&XCC(4) &CC has	mask values for FAILED condition codes
				461 &XCC(1) 462 &XCC(2)	SETA SETA	7 11	CC != 0 CC != 1
				463 &XCC(3)	SETA	13	CC != 2
				464 &XCC(4) 465	SETA	14	CC != 3
				466	GBLA	&TNUM	
				467 &TNUM 468	SETA	&TNUM+1	
				469	DS	OFD * DE	has for test data and test repting
				470 471	USING	*, KJ	base for test data and test routine
				472 T&TNUM 473	DC DC	A(X&TNUM) H'&TNUM	address of test routine test number
				474	DC	X' 00'	
				475 476	DC DC	HL1' &I 4' HL1' &M5'	i 4 m5
				477	DC	HL1' &CC'	cc
				478 479 V2_&TNU	DC M DC	HL1' &XCC(&CC+1) ' FD' &V2'	cc failed mask binary value for v2 packed decimal
				480 V3_&TNU	M DC	FD' &V3'	binary value for v3 packed decimal
				481 482	DC DC	CL8' &I NST' A(16)	instruction name result length
				483 REA&TNU	M DC	A(RE&TNUM)	result address
				484 .* 485 *			INSTRUCTION UNDER TEST ROUTINE
				486 X&TNUM 487	DS LG	OF R2, V2_&TNUM	convert v2
				488	CVDG	R2, V2PACKED	
				489 490	VL	V2, V2PACKED	
				491	LG	R2, V3_&TNUM	convert v3
				492 493	VL VL	R2, V3PACKED V3, V3PACKED	
				494		·	test instruction
				495 496		V1, V2, V3, &I4, &M5	test instruction
				497 498	VST FDSW	V1, V10UTPUT R2, R0	save result
				499	ST	R2, CCPSW	exptract psw to save CC
				500 501	BR	R11	return

LOC	OBJECT CODE	ADDR2	STM			thmetic)	02 Jun 2024 15: 59: 21	
			502 R 503	E&TNUM				
			503 504 505		DROP MEND	R5		

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LOC	OBJECT CODE	ADDR1	ADDR2	STMF				
				530 ******	*****	******	************	
				531 * 532 ******	E6 VR	I_F tests **********	***********	
		00000000	00004EEF	533 ZVE6TST	CSECT	•		
00001180				534	DS	OF		
				500	DDIAT	DATEA		
				536 537 *	PRINT	DATA		
				538 * 539 *	E671 E673		TOR ADD DECIMAL TOR SUBTRACT DECIMAL	
				540 *	E678	VMP - VECT	TOR MULTIPLY DECIMAL	
				541 * 542 *	E679 E67A		TOR MULTIPLY AND SHIFT DECIMAL TOR DIVIDE DECIMAL	
				543 *	E67B	VRP - VECT	TOR REMAINDER DECIMAL	
				544 * 545	E67E	vour - vect	TOR SHIFT AND DIVIDE DECIMAL	
				546 * 547 *	VRI_F	instr, v2, v3,	i 4, m5, cc 16 byte expected result	
				548		10110wed by	TO Dyce expected resurt	
				549 * 550 * VAP	 - V E	CTOR ADD DECI	MAT.	
				551 *				
				552 * VAP si 553		CC checks VAP, +10, +12,	7, 1, 2	
00001180 00001180		00001180		554+ 555+	DS USING	OFD	base for test data and test routine	
00001180	000011B0	00001100		556+T1	DC	A(X1)	address of test routine	
00001184 00001186	0001			557+ 558+	DC DC	H' 1' X' 00'	test number	
00001187	07			559 +	DC	HL1' 7'	i <u>4</u>	
00001188 00001189				560+ 561+	DC DC	HL1'1' HL1'2'	m5 CC	
0000118A	OD			562 +	DC	HL1' 13'	cc failed mask	
	00000000 0000000A 00000000 0000000C			563+V2_1 564+V3_1	DC DC	FD' +10' FD' +12'	binary value for v2 packed decimal binary value for v3 packed decimal	
	E5C1D740 40404040 00000010			565+ 566+	DC DC	CL8' VAP' A(16)	instruction name result length	
	000011EC			567+REA1	DC	A(RE1)	result address	
000011B0				568+* 569+X1	DS	OF	INSTRUCTION UNDER TEST ROUTINE	
000011B0	E320 5010 0004		00001190	570 +	LG	R2, V2_1	convert v2	
000011BC	E320 8F4F 002E E720 8F4F 0006		0000114F 0000114F	571+ 572+	VL	R2, V2PACKED V2, V2PACKED		
	E320 5018 0004 E320 8F5F 002E		00001198 0000115F	573+ 574+	LG CVDG	R2, V3_1 R2, V3PACKED	convert v3	
000011CE	E730 8F5F 0006		0000113F 0000115F	575 +	VL	V3, V3PACKED		
	E612 3010 7071 E710 8F00 000E		00001100	576+ 577+	VAP VST	V1, V2, V3, 7, 1 V1, V10UTPUT	test instruction save result	
000011E0	B98D 0020			578 +	EPSW	R2, R0	exptract psw	
000011E8	5020 8EE4 07FB		000010E4	579+ 580+	ST BR	R2, CCPSW R11	to save CC return	
000011EC 000011EC				581+RE1 582+	DC DROP	0F R5		
000011EC	00000000 00000000 0000000 0000022C			583	DC		0000000000000000000022C'	

R2, V3PACKED

CVDG

638 +

0000115F

000012C8

E320 8F5F 002E

Bill VCI.	0 0 Zvecedi ed	oo packarre	11 (2100001	•	cheu uii		
LOC	OBJECT CODE	ADDR1	ADDR2	STM			
0001480				747 +	DS	OFD	
0001480		00001480		748+	USING		base for test data and test routine
0001480	000014B0	00001100		749+T7	DC	A(X7)	address of test routine
0001484	0007			750+	DC	H' 7'	test number
0001486	00			751+	DC	X' 00'	cest number
0001480	9F			751+ 752+	DC	HL1' 159'	: A
							i 4
0001488	01			753+	DC	HL1' 1'	шб
0001489	02			754+	DC	HL1' 2'	cc
000148A	OD			755+	DC	HL1' 13'	cc failed mask
				756+V2_7	DC	FD' +9999999999999	
0001490	01634578 5D89FFFF			+			binary value for v2 packed decimal
0001498	00000000 00000001			757+V3_7	DC	FD' +1'	binary value for v3 packed decimal
00014A0	E5C1D740 40404040			758 +	DC	CL8' VAP'	instruction name
00014A8	0000010			759 +	DC	A(16)	result length
00014AC				760+REA7	DC	A(RE7)	result address
0001	33331111			761+*		()	INSTRUCTION UNDER TEST ROUTINE
00014B0				762+X7	DS	0F	THE TAXABLE OF THE PART OF THE PARTY OF THE
00014B0	E320 5010 0004		00001490	762+X7 763+	LG	R2, V2_7	convert v2
	E320 8F4F 002E			764+		R2, V2_7 R2, V2PACKED	CONVET C VA
00014B6			0000114F				
00014BC	E720 8F4F 0006		0000114F	765+	VL	V2, V2PACKED	
00014C2	E320 5018 0004		00001498	766 +	LG	R2, V3_7	convert v3
00014C8	E320 8F5F 002E		0000115F	767 +		R2, V3PACKED	
00014CE	E730 8F5F 0006		0000115F	768 +	\mathbf{VL}	V3, V3PACKED	
00014D4	E612 3019 F071			769 +	VAP	V1, V2, V3, 159, 1	test instruction
00014DA	E710 8F00 000E		00001100	770 +	VST	V1, V10UTPUT	save result
00014E0	B98D 0020			771+		R2, R0	exptract psw
00014E4	5020 8EE4		000010E4	772+	ST	R2, CCPSW	to save CC
00014E8	07FB		00001011	773+	BR	R11	return
000014EC	0.12			774+RE7	DC	0F	
00014EC				775+	DROP	R5	
00014EC	0000000 00000100			776	DC		010000000000000000C'
00014EC	0000000 00000100 00000000 0000000C			770	ЪС	ALIU UUUUUUUUUUU	010000000000000000000000000000000000000
				777			
				778	VRI_F	VAP, +999999999999	99999, +100000000000000000, 159, 1, 2
0001500				779 +	DS	OFD	
0001500		00001500		780 +	USING	*, R 5	base for test data and test routine
0001500	00001530			781+T8	DC	A(X8)	address of test routine
0001504	0008			782 +	DC	H'8'	test number
0001506	00			783+	DC	X' 00'	
0001507	9F			784 +	DC	HL1' 159'	i 4
0001507	01			785+	DC	HL1' 1'	m5
0001508	02			786+		HL1' 2'	
					DC		CC
000150A	OD			787+	DC	HL1' 13'	cc failed mask
0001510	01694570 EDOOFFEE			788+V2_8	DC	FD' +9999999999999	
0001510	01634578 5D89FFFF			+ 700. V2. 0	DC	EDI . 1000000000000	binary value for v2 packed decimal
0001510	00000000 00010000			789+V3_8	DC	FD' +1000000000000	
0001518	002386F2 6FC10000			+	T	GI OLIVADI	binary value for v3 packed decimal
0001520	E5C1D740 40404040			790+	DC	CL8' VAP'	instruction name
0001528	00000010			791+	DC	A(16)	result length
000152C	0000156C			792+REA8	DC	A(RE8)	result address
				793+*			INSTRUCTION UNDER TEST ROUTINE
0001530				794+X8	DS	OF	
0001530	E320 5010 0004		00001510	795+	LG	R2, V2_8	convert v2
0001536	E320 8F4F 002E		00001310 0000114F	796+	CVDG	R2, V2PACKED	
000153C	E720 8F4F 0006		0000114F	797+	VL	V2, V2PACKED	
							convert v2
0001542	E320 5018 0004		00001518	798+	LG	R2, V3_8	convert v3

R2, CCPSW

R11

to save CC

return

ST

BR

000016E4

000016E8

5020 8EE4

07FB

000010E4

902+

903 +

VST

EPSW R2, R0

V1, V10UTPUT

save result

exptract psw

0000195A

00001960

E710 8F00 000E

B98D 0020

00001100

1064+

1065 +

DC

1173 +

00001B04

0014

H' 20'

test number

CL8' VSP'

instruction name

DC

1277+

00001CA0

E5E2D740 40404040

R2, V2PACKED

V2, V2PACKED

CVDG

00001E36

00001E3C

E320 8F4F 002E

E720 8F4F 0006

0000114F

0000114F

1381+

1382 +

DC

1435+

00001F04

001C

H' 28'

test number

BR

R11

return

1490 +

07FB

00001FE8

LG

R2, V2 31

convert v2

00002090

1544+

000020B0

E320 5010 0004

DC

1598 +

00002188

01

HL1' 1'

m5

DS

1704+X36

0F

1757 +

00002406

00

X' 00'

1913

0000266C

00002674

0000000 00000009

9999999 999999F

R2, CCPSW

to save CC

ST

000010E4

2074+

000028E4

5020 8EE4

	•	•	E6 VRI-f pack		C11112 C1 C)	02 Jun 2024 15: 59: 21 Page 4
OBJECT CODE	ADDR1	ADDR2	STMT			
07FB			2075+ 2076+RE47	BR DC	R11 OF	return
00000000 00000000 0000000 0000008D			2078	DC DC		00000000000000000000000000000000000000
				VRI F	VDP. +100 12. 7.	1. 1
	0000000		2081+	DS	OFD	
00002930 0030	00002900		2082+ 2083+T48 2084+	DC DC	A(X48) H' 48'	base for test data and test routine address of test routine test number
00			2085+	DC DC	Х' 00'	i 4
01			2087+	DC DC	HL1' 1'	m5
01 op			2088+	DC		CC
=						cc failed mask binary value for v2 packed decimal
FFFFFFF FFFFFF4			2091+V3_48	DC	FD' - 12'	binary value for v3 packed decimal
						instruction name result length
0000010 0000296C			2094+REA48	DC	A(RE48)	result address
			2095+*	DC		INSTRUCTION UNDER TEST ROUTINE
E320 5010 0004		00002910				convert v2
E320 8F4F 002E		0000114F	2098+	CVDG	R2, V2PACKED	
						convert v3
E320 8F5F 002E E730 8F5F 0006		00002318 0000115F 0000115F	2101+ 2102+	CVDG VL	R2, V3_46 R2, V3PACKED V3, V3PACKED	Convert v3
E612 3010 707A E710 8F00 000E		00001100	2103+ 2104+	VDP VST	V1, V2, V3, 7, 1 V1, V10UTPUT	test instruction save result
B98D 0020		000010E4	2105+	EPSW	R2, R0	exptract psw
		000010E4				to save CC return
0.12			2108+RE48	DC	0F	100111
00000000 00000000 00000000 0000008D			2109+ 2110	DROP DC		00000000000000000000000000000000000000
			2111	VDI E	VDD 100 19 7	1 9
			2112 2113+	VKI_F DS	VDP, - 100, - 12, 7, OFD	1, &
00000000	00002980		2114+			base for test data and test routine
						address of test routine test number
00			2117+	DC	X' 00'	
07				DC DC		i 4 m5
02			2120+	DC	HL1' 2'	CC
OD			2121+	DC	HL1' 13'	cc failed mask
						binary value for v2 packed decimal binary value for v3 packed decimal
E5C4D740 40404040			2124+	DC	CL8' VDP'	instruction name
00000010			2125+	DC	A(16)	result length
000029EC			2126+REA49 2127+*	DC	A(RE49)	result address INSTRUCTION UNDER TEST ROUTINE
	00000000 00000000 00000000 0000008D 00002930 000 07 01 01 0B 00000000 00000064 FFFFFFFF FFFFFFF4 E5C4D740 40404040 00000010 0000296C E320 5010 0004 E320 8F4F 002E E720 8F4F 0006 E320 5018 0004 E320 8F5F 002E E730 8F5F 002E E730 8F5F 0006 E612 3010 707A E710 8F00 000E B98D 0020 5020 8EE4 07FB 00000000 000000000 00000000 000000000	00000000 000000000 000000000 000000000	00000000 00000000 00000000 00000000 0000	07FB	0.0000000	OPTB

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0002EA0	E5C4D740 4040404	n		2447+	DC	CL8' VDP'	instruction name
0002EA0	00000010	J		2447+ 2448+	DC	A(16)	result length
				2449+REA59			result address
0002EAC	00002EEC				DC	A(RE59)	
				2450+*	D.C.	O.F.	INSTRUCTION UNDER TEST ROUTINE
0002EB0				2451+X59	DS	OF	
0002EB0	E320 5010 0004		00002E90	2452+	LG	R2, V2_59	convert v2
)002EB6	E320 8F4F 002E		0000114F	2453+	CVDG	R2, V2PACKED	
0002EBC	E720 8F4F 0006		0000114F	2454+	VL	V2, V2PACKED	
0002EC2	E320 5018 0004		00002E98	2455+	LG	R2, V3_59	convert v3
0002EC8	E320 8F5F 002E		0000115F	2456 +	CVDG	$R2, V3\overline{P}ACKED$	
0002ECE	E730 8F5F 0006		0000115F	2457+	VL	V3, V3PACKED	
0002ED4	E612 30D9 F07A		00001101	2458+	VDP	V1, V2, V3, 159, 13	test instruction
002EDA	E710 8F00 000E		00001100	2459+	VST	V1, V2, V3, 133, 13 V1, V10UTPUT	save result
002EE0	B98D 0020		00001100	2460+	FDCW	R2, R0	
			000010E4				exptract psw
0002EE4	5020 8EE4		000010E4	2461+	ST	R2, CCPSW	to save CC
0002EE8	07FB			2462+	BR	R11	return
0002EEC				2463+RE59	DC	0F	
0002EEC				2464 +	DROP	R 5	
002EEC 002EF4	00000000 00000000			2465	DC	XL16' 000000000000	0000009999999999999C'
				2466	VDI T	LIDD 0000000000	00000 1 170 0 0
				2467		VDP, - 99999999999999999999999999999999999	99999, -1, 159, 3, 2 $m5=3(P1=1)$
002F00				2468+	DS	OFD	
002F00		00002F00		2469 +	USING		base for test data and test routine
002F00	00002F30			2470+T60	DC	A(X60)	address of test routine
002F04	003C			2471+	DC	H' 60'	test number
002F06	00			2472+	DC	X' 00'	
0002F07	9F			2473+	DC	HL1' 159'	i 4
0002F08	03			2474+	DC	HL1'3'	m5
0002F09	02			2475+	DC	HL1' 2'	CC
0002F0A	OD OD			2476+	DC	HL1' 13'	cc failed mask
JUULIUA	OD			2477+V2_60	DC	FD' - 99999999999999999999999999999999999	
0009E10	FFDC790D 903F000	1		_	ъс	TD - 999999999999	
				+	DC	EDI 11	binary value for v2 packed decimal
	FFFFFFF FFFFFFF			2478+V3_60	DC	FD' - 1'	binary value for v3 packed decimal
	E5C4D740 40404040)		2479+	DC	CL8' VDP'	instruction name
0002F28	0000010			2480 +	DC	A(16)	result length
0002F2C	00002F6C			2481+REA60	DC	A(RE60)	result address
				2482+*			INSTRUCTION UNDER TEST ROUTINE
0002F30				2483+X60	DS	0F	
0002F30	E320 5010 0004		00002F10	2484+	LG	R2, V2_60	convert v2
0002F36	E320 8F4F 002E		0000114F	2485+	CVDG	R2, V2PACKED	
0002F3C	E720 8F4F 0006		0000111F	2486+	VL	V2, V2PACKED	
002F42	E320 5018 0004			2487+	ĹĠ	R2, V3_60	convert v3
002F42	E320 8F5F 002E		00002118 0000115F	2488+		R2, V3_00 R2, V3PACKED	CONTOLOU
0002F4E	E730 8F5F 0006		0000115F	2489+	VL	V3, V3PACKED	toot instancelies
0002F54	E612 3039 F07A		00001100	2490+	VDP	V1, V2, V3, 159, 3	test instruction
002F5A	E710 8F00 000E		00001100	2491+	VST	V1, V10UTPUT	save result
002F60	B98D 0020			2492+	EPSW	R2, R0	exptract psw
)002F64	5020 8EE4		000010E4	2493+	ST	R2, CCPSW	to save CC
0002F68	07FB			2494+	BR	R11	return
0002F6C				2495+RE60	DC	OF	
002F6C				2496+	DROP	R5	
002F6C	00000000 00000009	9		2497	DC		00009999999999999999999999999999999999
002F74	99999999 9999999			WIUI	DC	ALIO OUOOOOOO	000000000000000000000000000000000000000
/UU&Γ / 4		·		2400			
				2498 2499 *			7 (0(TO 1 TO 1)
				0 1 (M) ×			m5=13(P2=1, P3=1)

LG

00003018

2552+

R2, V3 62

convert v3

00003042

E320 5018 0004

H' 64'

test number

2605+

00003104

BR

R11

return

2660+

07FB

000031E8

LG

R2, V2 67

convert v2

00003290

2714+

000032B0

E320 5010 0004

2768 +

HL1' 1'

m5

00003388

XL16' 0000000000000000000000000000000001C'

note RDC

2823

0000000 00000000

0000346C

LG

R2, V2 72

convert v2

E320 5010 0004

00003530

00003510

2875+

3087+T79

DC

A(X79)

address of test routine

00003880

000038B0

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LOC	OBJECT	CODE	ADDR1	ADDR2	STM			
00003AE0 00003AE4	B98D 0020 5020 8EE4			000010E4	3249+ 3250+		R2, CCPSW	exptract psw to save CC
00003AE8 00003AEC 00003AEC	07FB				3251+ 3252+RE83 3253+	DC DROP	R11 OF R5	return
00003AEC 00003AF4	00000000				3254 3255	DC	XL16' 00000000000000	00000000000000012C'
00003B00 00003B00		0	0003B00		3256 3257+ 3258+		VMSP, -100, +12, 129, OFD * P5	1,1 shamt=1 base for test data and test routine
00003B00 00003B04	00003B30 0054	· ·	ооозвоо		3259+T84 3260+	DC DC	A(X84) H' 84'	address of test routine test number
00003B08	00 81 01				3261+ 3262+ 3263+	DC DC	X' 00' HL1' 129' HL1' 1'	i 4 m5
00003B09 00003B0A 00003B10	01 0B FFFFFFF	FFFFFF9C			3264+ 3265+ 3266+V2_84	DC	HL1' 1' HL1' 11' FD' - 100'	cc cc failed mask binary value for v2 packed decimal
	00000000 E5D4E2D7 00000010	000000C			3267+V3_84 3268+ 3269+	DC DC	FD' +12' CL8' VMSP' A(16)	binary value for v3 packed decimal instruction name result length
00003B2C	0000010 00003B6C				3270+REA84 3271+*	DC	A(RE84)	result rength result address INSTRUCTION UNDER TEST ROUTINE
00003B30 00003B30 00003B36	E320 5010 E320 8F4F	002E			3272+X84 3273+ 3274+	LG CVDG	OF R2, V2_84 R2, V2PACKED	convert v2
00003B3C 00003B42 00003B48	E720 8F4F E320 5018 E320 8F5F	0004		00003B18	3275+ 3276+ 3277+	LG	V2, V2PACKED R2, V3_84 R2, V3PACKED	convert v3
00003B4E 00003B54	E730 8F5F E612 3018 E710 8F00	0006 1079			3278+ 3279+	VL VMSP	V3, V3PACKED V1, V2, V3, 129, 1 V1, V10UTPUT	test instruction save result
00003B60 00003B64	B98D 0020 5020 8EE4			00001100 000010E4	3281+ 3282+	EPSW ST	R2, R0 R2, CCPSW	exptract psw to save CC
00003B68 00003B6C 00003B6C	07FB				3283+ 3284+RE84 3285+		R11 OF R5	return
00003B6C 00003B74	00000000				3286 3287	DC	XL16' 0000000000000	00000000000000120D'
00003B80 00003B80		0	0003B80		3288 3289+ 3290+		VMSP, +100, -12, 128, OFD * P5	1,1 shamt=0 base for test data and test routine
00003B80 00003B84	00003BB0 0055		OUUJUOU		3291+T85 3292+	DC DC	A(X85) H' 85'	address of test routine test number
00003B88	00 80 01				3293+ 3294+ 3295+	DC DC	X' 00' HL1' 128' HL1' 1'	i 4 m5
00003B8A 00003B90	01 0B 00000000				3296+ 3297+ 3298+V2_85	DC DC	HL1' 1' HL1' 11' FD' +100'	cc cc failed mask binary value for v2 packed decimal
	FFFFFFF 1 E5D4E2D7 00000010				3299+V3_85 3300+ 3301+	DC	FD' - 12' CL8' VMSP' A(16)	binary value for v3 packed decimal instruction name result length
	00003BEC				3302+REA85		A(RE85)	result address

H' 87'

test number

3356 +

00003C84

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LOC	OBJECT CODE	ADDR1	ADDR2	STMI			
	00 00			3357+ 3358+	DC DC	X' 00' HL1' 0'	i 4
00003C88	01			3359+ 3360+	DC	HL1' 1' HL1' 2'	m5
00003C89 00003C8A	02 0D			3361+	DC DC	HL1' 2'	cc cc failed mask
00003C90	FFFFFFFF FFFFF9C			3362+V2_87	DC	FD' - 100'	binary value for v2 packed decimal
00003C98 00003CA0	FFFFFFF FFFFFF4 E5D4E2D7 40404040			3363+V3_87 3364+	DC DC	FD' - 12' CL8' VMSP'	binary value for v3 packed decimal instruction name
00003CA8	0000010			3365+	DC	A(16)	result length
00003CAC	00003CEC			3366+REA87 3367+*	DC	A(RE87)	result address INSTRUCTION UNDER TEST ROUTINE
00003CB0 00003CB0	E320 5010 0004		00003C90	3368+X87 3369+	DS LG	0F R2, V2_87	convent v9
00003CB0	E320 3010 0004 E320 8F4F 002E		00003C90 0000114F	3370+		R2, V2_O7 R2, V2PACKED	convert v2
00003CBC	E720 8F4F 0006		0000114F	3371+	VL LC	V2, V2PACKED	convent v2
00003CC2 00003CC8	E320 5018 0004 E320 8F5F 002E		00003C98 0000115F	3372+ 3373+	LG CVDG	R2, V3_87 R2, V3PACKED	convert v3
00003CCE	E730 8F5F 0006		0000115F	3374+	VL	V3, V3PACKED	A A - 2 A - 2
00003CD4 00003CDA	E612 3010 0079 E710 8F00 000E		00001100	3375+ 3376+	VNBP VST	V1, V2, V3, 0, 1 V1, V10UTPUT	test instruction save result
00003CE0	B98D 0020			3377+	EPSW	R2, R0	exptract psw
00003CE4 00003CE8	5020 8EE4 07FB		000010E4	3378+ 3379+	ST BR	R2, CCPSW R11	to save CC return
00003CEC				3380+RE87	DC	0F	
00003CEC 00003CEC	0000000 00000000			3381+ 3382	DROP DC	R5 XL16' 00000000000000	00000000000001200C'
00003CF4	00000000 0001200C			3383			
				3384		VMSP, -100, -10, 0, 1	shamt=0
00003D00 00003D00		00003D00		3385+ 3386+	DS USING	0FD * R5	base for test data and test routine
00003D00	00003D30	OOOOODOO		3387+T88	DC	A(X88)	address of test routine
00003D04 00003D06				3388+ 3389+	DC DC	H' 88' X' 00'	test number
00003D07	00			3390+	DC	HL1' 0'	i 4
	01 02			3391+ 3392+	DC DC	HL1' 1' HL1' 2'	m5 cc
00003D0A	OD			3393+	DC	HL1' 13'	cc failed mask
	FFFFFFFF FFFFFF6			3394+V2_88 3395+V3_88	DC DC	FD' - 100' FD' - 10'	binary value for v2 packed decimal binary value for v3 packed decimal
00003D20	E5D4E2D7 40404040			3396+	DC	CL8' VMSP'	instruction name
00003D28 00003D2C	00000010 00003D6C			3397+ 3398+REA88	DC DC	A(16) A(RE88)	result length result address
	OUUUUUU			3399+*			INSTRUCTION UNDER TEST ROUTINE
00003D30 00003D30	E320 5010 0004		00003D10	3400+X88 3401+	DS LG	0F R2, V2_88	convert v2
00003D36	E320 8F4F 002E		0000114F	3402+	CVDG	R2, V2PACKED	CONVEL VA
00003D3C 00003D42	E720 8F4F 0006 E320 5018 0004		0000114F 00003D18		VL LG	V2, V2PACKED R2, V3_88	convert v3
00003D48	E320 8F5F 002E		0000115F	3405+	CVDG	R2, V3PACKED	CONVELC VO
00003D4E 00003D54	E730 8F5F 0006		0000115F	3406+ 3407+	VL	V3, V3PACKED	tost instruction
00003D5A	E612 3010 0079 E710 8F00 000E		00001100	3407+ 3408+	VNBP VST	V1, V2, V3, 0, 1 V1, V10UTPUT	test instruction save result
00003D60	B98D 0020			3409+	EPSW	R2, R0	exptract psw
00003D64 00003D68	5020 8EE4 07FB		000010E4	3410+ 3411+	ST BR	R2, CCPSW R11	to save CC return

VMSP

V1, V2, V3, 135, 1

test instruction

3569 +

E612 3018 7079

00003FD4

DC

HL1'2'

 \mathbf{cc}

3621 +

00004089

EPSW

ST

R2, R0

R2, CCPSW

exptract psw

to save CC

3672+

3673+

000010E4

00004160

00004164

B98D 0020

5020 8EE4

DC

XL16' 00000000000000000000000000099F'

3778

000042EC

ASNA VEI.	0. 7. 0 zvector-e6-0	os- packari ci	i (Zvector	EO VKI-I Pack	eu arro	timetre)	02 Jun 2024 15: 59: 21 Page /	9
LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00004480				3887 3888+	DS	VSDP, +100, -12, 132, OFD		
00004480 00004484	000044B0	00004480		3889+ 3890+T103	USING DC	A(X103)	base for test data and test routine address of test routine	
00004484 00004486	0067 00			3891+ 3892+	DC DC	X' 00'	test number	
00004487 00004488	84 01			3893+ 3894+	DC DC		i 4 m5	
00004489 0000448A	01 0B			3895+ 3896+	DC DC		cc cc failed mask	
00004490	00000000 00000064			3897+V2_103	DC	FD' +100'	binary value for v2 packed decimal	
00004498 000044A0	FFFFFFF FFFFFF4 E5E2C4D7 40404040			3898+V3_103 3899+	DC DC	FD' - 12' CL8' VSDP'	binary value for v3 packed decimal instruction name	
000044A8 000044AC	00000010 000044EC			3900+ 3901+REA103	DC DC	A(16) A(RE103)	result length result address	
000044B0				3902+* 3903+X103	DS	0F	INSTRUCTION UNDER TEST ROUTINE	
000044B0 000044B6	E320 5010 0004 E320 8F4F 002E		00004490 0000114F	3904+ 3905+	LG		convert v2	
000044BC	E720 8F4F 0006		0000114F	3906+	VL	V2, V2PACKED		
000044C2 000044C8	E320 5018 0004 E320 8F5F 002E		00004498 0000115F	3907+ 3908+		R2, V3PACKED	convert v3	
000044CE 000044D4	E730 8F5F 0006 E612 3018 407E		0000115F	3909+ 3910+	VL VSDP		test instruction	
000044DA 000044E0	E710 8F00 000E B98D 0020		00001100	3911+ 3912+	VST EPSW	V1, V10UTPUT R2, R0	save result exptract psw	
000044E4 000044E8	5020 8EE4 07FB		000010E4	3913+ 3914+	ST BR	R2, CCPSW	to save CC return	
000044EC 000044EC	0.12			3915+RE103 3916+	DC DROP	OF R5		
000044EC 000044EC 000044F4	00000000 00000000 00000000 0083333D			3917	DC		000000000000083333D'	
				3918 3919	VRI_F	VSDP, +100, -12, 128,	1, 1 shamt=0	
00004500 00004500		00004500		3920+ 3921+	DS USING	OFD	base for test data and test routine	
00004500 00004504	00004530 0068			3922+T104 3923+	DC DC	A(X104) H' 104'	address of test routine test number	
00004506	00 80			3924+ 3925+	DC	X' 00'		
00004507 00004508	01			3926+	DC DC	HL1' 1'	i 4 m5	
00004509 0000450A	01 0B			3927+ 3928+	DC DC	HL1' 11'	cc cc failed mask	
00004510 00004518	00000000 00000064 FFFFFFF FFFFFF4			3929+V2_104 3930+V3_104	DC DC	FD' +100' FD' - 12'	binary value for v2 packed decimal binary value for v3 packed decimal	
00004520 00004528	E5E2C4D7 40404040 00000010			3931+ 3932+	DC DC	CL8' VSDP' A(16)	instruction name result length	
00004528 0000452C	0000456C			3933+REA104 3934+*	DC	A(RE104)	result address INSTRUCTION UNDER TEST ROUTINE	
00004530 00004530	E320 5010 0004		00004510	3935+X104 3936+	DS LG	0F R2, V2_104	convert v2	
00004536	E320 8F4F 002E		0000114F	3937+	CVDG	R2, V2PACKED	COHVEL VA	
0000453C 00004542	E720 8F4F 0006 E320 5018 0004		0000114F 00004518	3938+ 3939+	VL LG		convert v3	
00004548 0000454E	E320 8F5F 002E E730 8F5F 0006		0000115F 0000115F	3940+ 3941+	CVDG VL	R2, V3PACKED V3, V3PACKED		

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LOC	OBJECT	CODE	ADDR1	ADDR2	STMT						
00004554 0000455A	E612 3018 E710 8F00	000E		00001100	3942+ 3943+	VST	V1, V2, V3, 128, 1 V1, V10UTPUT	test instruction save result			
00004560 00004564 00004568	B98D 0020 5020 8EE4 07FB			000010E4	3944+ 3945+ 3946+	EPSW ST BR	R2, R0 R2, CCPSW R11	exptract psw to save CC return			
0000456C 0000456C 0000456C	0000000	00000000			3947+RE104 3948+ 3949	DC DROP DC	OF R5 XL16' 00000000000000	00000000000000000000000000000000000000			
00004574	00000000				3950 3951		VSDP, - 100, - 12, 129,		shamt=1		
00004580 00004580			00004580		3952+ 3953+	DS USING	OFD *, R5	base for test data a	and test routi	ne	
00004580 00004584 00004586	000045B0 0069 00				3954+T105 3955+ 3956+	DC DC DC	A(X105) H' 105' X' 00'	address of test rout test number	ti ne		
00004587 00004588 00004589	81 01 02				3957+ 3958+ 3959+	DC DC DC	HL1' 129' HL1' 1' HL1' 2'	i 4 m5 cc			
0000458A 00004590	OD FFFFFFF				3960+ 3961+V2_105	DC DC	HL1' 13' FD' - 100'	cc failed mask binary value for v2			
00004598 000045A0 000045A8	FFFFFFF E5E2C4D7 00000010				3962+V3_105 3963+ 3964+	DC DC DC	FD' - 12' CL8' VSDP' A(16)	binary value for v3 instruction name result length	packed decima	ıl	
000045AC 000045B0	000045EC				3965+REA105 3966+* 3967+X105	DC	A(RE105) OF	result address INSTRUCTION UNDER T	EST ROUTINE		
000045B0 000045B6	E320 5010 E320 8F4F	002E		00004590 0000114F	3968+ 3969+		R2, V2_105 R2, V2PACKED	convert v2			
000045BC 000045C2 000045C8	E720 8F4F E320 5018 E320 8F5F	0004		0000114F 00004598 0000115F	3970+ 3971+ 3972+	VL LG CVDG	V2, V2PACKED R2, V3_105 R2, V3PACKED	convert v3			
000045CE	E730 8F5F E612 3018 E710 8F00	107E		0000115F 00001100	3973+ 3974+ 3975+	VL	V3, V3PACKED V1, V2, V3, 129, 1 V1, V10UTPUT	test instruction save result			
000045E0 000045E4	B98D 0020 5020 8EE4			00001100 000010E4	3976+ 3977+	EPSW ST	R2, R0 R2, CCPSW	exptract psw to save CC			
000045E8 000045EC 000045EC	07FB				3978+ 3979+RE105 3980+		R11 OF R5	return			
000045EC 000045F4	00000000				3981 3982	DC	XL16' 00000000000000	00000000000000000083C			
00004600			00004000		3983 3984+	DS	VSDP, -100, -10, 135, OFD		shamt=7		
00004600 00004600 00004604	00004630 006A		00004600		3985+ 3986+T106 3987+	USING DC DC	*, R5 A(X106) H' 106'	base for test data a address of test rout test number		ne	
00004606 00004607 00004608	00 87 01				3988+ 3989+ 3990+	DC DC DC	X' 00' HL1' 135' HL1' 1'	i 4 m5			
00004609 0000460A	02 0D				3991+ 3992+	DC DC	HL1' 2' HL1' 13'	cc cc failed mask			
00004610 00004618 00004620	FFFFFFFF FFFFFFFF E5E2C4D7	FFFFFF6			3993+V2_106 3994+V3_106 3995+	DC DC DC	FD' - 100' FD' - 10' CL8' VSDP'	binary value for v2 binary value for v3 instruction name			

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
		00000016 00000017	00000001 00000001	4624 V22 4625 V23	EQU EQU	22 23			
		$00000018 \\ 00000019$	$00000001 \\ 00000001$	4626 V24 4627 V25	EQU EQU	24 25			
		0000001A 0000001B	00000001 00000001	4628 V26 4629 V27	EQU EQU	26 27			
		0000001C 0000001D	00000001	4630 V28 4631 V29	EQU	22 23 24 25 26 27 28 29 30 31			
		0000001E 0000001F	00000001 00000001	4633 V31	EQU EQU	30 31			
				4634 4635	END				

ASMA Ver. 0.7.0	zvector	- e6- 05- pac	karith (Zve	ctor E6	VRI - f	packe	d arit	hmetic	e)				02 Jun	2024	15: 59:	21 Pa	ıge	96
SYMB0L	ТҮРЕ	VALUE	LENGTH	DEFN	REFER	ENCES												
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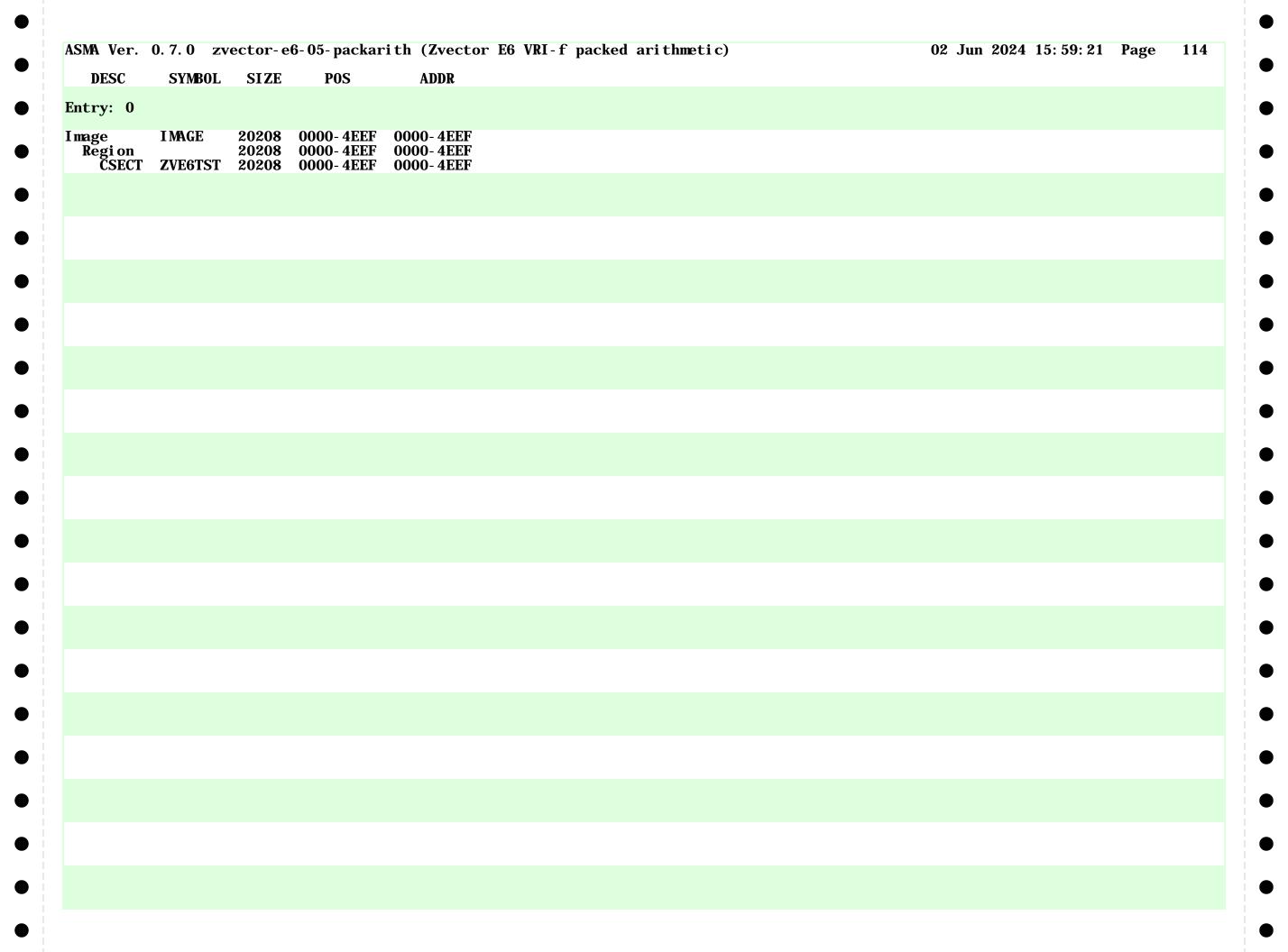
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					4397	4398	4431	4432	1200	1201	1200	1201	1200	1000	1001	1001	1000	
VALUE	F	0000018	8															
_1	F	00001198	8		573													
_10	r F	$00001618 \\ 00004318$	8	855 3802	864 3811													
_100 _101	F	00004318	8	3834	3843													
_102	F	00004418	8	3866	3875													
_103	F	00004498	8	3898	3907													
_104	F	00004518	8	3930	3939													
_105	F	00004598	8	3962	3971													
_106 _107	r F	00004618 00004698	8	3994 4026	4003 4035													
_108	F	00004038	8	4059	4068													
_109	F	00004798	8	4091	4100													
_11	F	00001698	8	887	896													
_110	<u>F</u>	00004818	8	4123	4132													
	F	00004898	8	4155	4164													
_112 	F	00004918 00004998	8	4187 4219	4196 4228													
_113 _114	F	00004998 00004A18	8	4219	4263													
	F	00004A18	8	4287	4296													
_116	F	00004B18	8	4320	4329													
	<u>F</u>	00004B98	8	4354	4363													
_118	F	00004C18	8	4387	4396													
_119	r F	00004C98 00001718	8	4421 919	4430 928													
_12 _13	F	00001718	8	955	964													
_13 _14	F	00001700	8	007	996													
_15	$ar{\mathbf{F}}$	00001898	8	1019	1028													
_16	<u>F</u>	00001918	8	1051	1060													
_17	F	00001998	8	1083	1092													
_18 _19	r F	00001A18 00001A98	8	1115 1147	1124 1156													
_19 _2	F	00001A98	8	596	605													
~	F	00001210 00001B18	8	1180	1189													
_21	F	00001B98	8	1212	1221													
_22	F	00001C18	8	1244	1253													
_23 	F	00001C98 00001D18	8	1276 1310	1285													
_24 _25	F	00001D18	8 8	1310	1319 1351													
_26	F	00001E38	8	1374	1383													
_27	$ar{\mathbf{F}}$	00001E98	8	1406	1415													
_28	F	00001F18	8	1442	1451													
_29	F	00001F98	8	1474	1483													
_3	F	00001298	8	628	637													
_30 _31	r F	$00002018 \\ 00002098$	8 8	1506 1538	1515 1547													
_31 _32	F	00002098	8	1570	1547 1579													
_33	F	00002110	8	1602	1611													
34	F	00002218	8	1634	1643													

ACRO		REFEREN		•	Ì			•		nmetic)						5: 59: 21	J	11:
TABLE I_F	512 452	4449 553 1104 1656 2209	585 1136 1688 2241	617 1169 1720 2273	649 1201 1752 2305	681 1233 1784 2337	713 1265 1818 2369	746 1299 1851 2403	778 1331 1883 2435	810 1363 1915 2467	844 1395 1948 2500	876 1431 1984 2532	908 1463 2016 2565	944 1495 2048 2601	976 1527 2080 2633	1008 1559 2112 2665	1040 1591 2144 2697	1077 1623 2170 2729
		2761 3320 3887	2793 3352 3919	2826 3384 3951	2858 3416 3983	2890 3449 4015	2922 3482 4048	2954 3514 4080	2986 3546 4112	3020 3578 4144	3052 3613 4176	3084 3647 4208	3117 3680 4243	3149 3714 4276	3181 3748 4309	3224 3791 4343	3256 3823 4376	3283 3853 4410



	zvector-e6-05-packarith (Zvector E6 VRI-f packed	arithmetic) 02 Jun 2024 15:59:21 Page 1:
STMT	FILE NAME	
/devstor/	dev/tests/zvector-e6-05-packarith.asm	
NO ERRORS FO	UND **	