```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2 ************************************************************************
                                                    3 *
                                                    4 *        Zvector E6 instruction tests for VSI encoded:
                                                    5 *
                                                    6 *        E63C VUPKZ   - VECTOR UNPACK ZONED
                                                    7 *        E63D VSTRL   - VECTOR STORE RIGHTMOST WITH LENGTH
                                                    8 *
                                                    9 *        James Wekel June 2024
                                                   10 ************************************************************************


                                                   12 ************************************************************************
                                                   13 *
                                                   14 *        basic instruction tests
                                                   15 *
                                                   16 ************************************************************************
                                                   17 *  This program tests proper functioning of the z/arch E6 VSI vector
                                                   18 *  unpack/store instructions. Exceptions are not tested.
                                                   19 *
                                                   20 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                   21 *  obvious coding errors.  None of the tests are thorough.  They are
                                                   22 *  NOT designed to test all aspects of any of the instructions.
                                                   23 *
                                                   24 ************************************************************************
                                                   25 *
                                                   26 *   *Testcase VECTOR E6 VSI unpack/store instructions
                                                   27 *   *
                                                   28 *   *    Zvector E6 instruction tests for VSI encoded:
                                                   29 *   *
                                                   30 *   *    E63C VUPKZ   - VECTOR UNPACK ZONED
                                                   31 *   *    E63D VSTRL   - VECTOR STORE RIGHTMOST WITH LENGTH
                                                   32 *   *
                                                   33 *   *    # ---------------------------------------------------------
                                                   34 *   *    #  This tests only the basic function of the instruction.
                                                   35 *   *    #  Exceptions are NOT tested.
                                                   36 *   *    # ---------------------------------------------------------
                                                   37 *   *
                                                   38 *   mainsize    2
                                                   39 *   numcpu      1
                                                   40 *   sysclear
                                                   41 *   archlvl     z/Arch
                                                   42 *
                                                   43 *   loadcore    "$(testpath)/zvector-e6-04-unpack.core" 0x0
                                                   44 *
                                                   45 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                   46 *   runtest     2
                                                   47 *   diag8cmd    disable   # (reset back to default)
                                                   48 *
                                                   49 *   *Done
                                                   50 *
                                                   51 ************************************************************************


                          00000000  000018DB     53 ZVE6TST  START 0
00000000                  00000000                 54          USING ZVE6TST,R0            Low core addressability
                                                   55
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                               00000140  00000000    56 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW

00000000                       00000000  000001A0    58          ORG   ZVE6TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                          59          DC    X'0000000180000000'
000001A8  00000000 00000200                          60          DC    AD(BEGIN)

000001B0                       000001B0  000001D0    62          ORG   ZVE6TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                          63          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                          64          DC    AD(X'DEAD')

000001E0                       000001E0  00000200    66          ORG   ZVE6TST+X'200'        Start of actual test program...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                      68
                                                      69 ********************************************************************************
                                                      70 *                The actual "ZVE6TST" program itself...
                                                      71 ********************************************************************************
                                                      72 *
                                                      73 *  Architecture Mode: z/Arch
                                                      74 *  Register Usage:
                                                      75 *
                                                      76 *   R0       (work)
                                                      77 *   R1-4     (work)
                                                      78 *   R5       Testing control table - current test base
                                                      79 *   R6-R7    (work)
                                                      80 *   R8       First base register
                                                      81 *   R9       Second base register
                                                      82 *   R10      E6TESTS register
                                                      83 *   R11      E6TEST call return
                                                      84 *   R12-R13  (work)
                                                      85 *   R14      Subroutine call
                                                      86 *   R15      Secondary Subroutine call or work
                                                      87 *
                                                      88 ********************************************************************************

00000200                          00000200            90          USING  BEGIN,R8        FIRST Base Register
00000200                          00001200            91          USING  BEGIN+4096,R9   SECOND Base Register

00000200  0580                                        93 BEGIN    BALR  R8,0             Initalize FIRST base register
00000202  0680                                        94          BCTR  R8,0             Initalize FIRST base register
00000204  0680                                        95          BCTR  R8,0             Initalize FIRST base register

00000206  4190 8800                       00000800    97          LA    R9,2048(,R8)     Initalize SECOND base register
0000020A  4190 9800                       00000800    98          LA    R9,2048(,R9)     Initalize SECOND base register
                                                      99
0000020E  B600 81EC                       000003EC   100          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
00000212  9604 81ED                       000003ED   101          OI    CTLR0+1,X'04'    Turn on AFP bit
00000216  9602 81ED                       000003ED   102          OI    CTLR0+1,X'02'    Turn on Vector bit
0000021A  B700 81EC                       000003EC   103          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                     104
                                                     105 *
0000021E  41A0 9638                       00001838   106          LA    R10,E6TESTS       get table of test addresses
                                                     107
                                  00000222  00000001   108 NEXTE6   EQU   *
00000222  5850 A000                       00000000   109          L     R5,0(0,R10)       get test address
00000226  1255                                       110          LTR   R5,R5                have a test?
00000228  4780 807C                       0000027C   111          BZ    ENDTEST                 done?
                                                     112
0000022C                          00000000           113          USING E6TEST,R5
0000022C  D20F 8E8C 8EBC          0000108C 000010BC  114          MVC   V1OUTPUT,V1FUDGE      fill output area
00000232  D20F 8E9C 8EBC          0000109C 000010BC  115          MVC   V1OUTPUT+16,V1FUDGE
                                                     116
00000238  E710 8ECC 0006                  000010CC   117          VL    V1,V1INPUT        load packed decimals
0000023E  58B0 5000                       00000000   118          L     R11,TSUB          get address of test routine
00000242  05BB                                       119          BALR  R11,R11           do test
                                                     120
00000244  E310 5014 0014                  00000014   121          LGF   R1,RESULT         get addr of expected result
0000024A  E320 5010 0014                  00000010   122          LGF   R2,RELEN          get compare length
00000250  0620                                       123          BCTR  R2,0                length-1 for clc
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00000252  4420 8062                     00000262   124          EX    R2,EXCLC          do compare
                                                    125
00000256  4770 8068                     00000268   126          BNE   FAILMSG          no, issue failed message
                                                    127
0000025A  41A0 A004                     00000004   128          LA    R10,4(0,R10)      next test address
0000025E  47F0 8022                     00000222   129          B     NEXTE6


00000262  D500 8E8C 1000      0000108C  00000000   131 EXCLC    CLC   V1OUTPUT(0),0(R1)    valid?


                                                    133 *
                                                    134 * test failed: issue message with test number, instruction under test
                                                    135 *               and instruction I3
                                                    136 *
                              00000268  00000001    137 FAILMSG  EQU   *
00000268  45F0 808A                     0000028A   138          BAL   R15,RPTERROR
0000026C  5800 81F4                     000003F4   139          L     R0,=F'1'          set failed test indicator
00000270  5000 8E00                     00001000   140          ST    R0,FAILED
                                                    141
00000274  41A0 A004                     00000004   142          LA    R10,4(0,R10)      next test address
00000278  47F0 8022                     00000222   143          B     NEXTE6
                                                    144
                              0000027C  00000001    145 ENDTEST  EQU   *
0000027C  5810 8E00                     00001000   146          L     R1,FAILED         did a test fail?
00000280  1211                                     147          LTR   R1,R1
00000282  4780 81D0                     000003D0   148          BZ    EOJ               No, exit
00000286  47F0 81E8                     000003E8   149          B     FAILTEST          Yes, exit with BAD PSW
                                                    150
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    152 ********************************************************************************
                                                    153 *        RPTERROR                  Report instruction test in error
                                                    154 ********************************************************************************

0000028A  50F0 80F0                       000002F0  156 RPTERROR ST    R15,RPTSAVE          Save return address
0000028E  5050 80F4                       000002F4  157          ST    R5,RPTSVR5           Save R5
                                                    158 *
00000292  4820 5004                       00000004  159          LH    R2,TNUM              get test number and convert
00000296  4E20 8E6E                       0000106E  160          CVD   R2,DECNUM
0000029A  D211 8E58 8E42      00001058    00001042  161          MVC   PRT3,EDIT
000002A0  DE11 8E58 8E6E      00001058    0000106E  162          ED    PRT3,DECNUM
000002A6  D202 8E14 8E65      00001014    00001065  163          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    164
000002AC  D207 8E2F 5008      0000102F    00000008  165          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    166 *
000002B2  B982 0022                               167          XGR   R2,R2
000002B6  4320 5007                       00000007  168          IC    R2,I3                get I3 and convert
000002BA  4E20 8E6E                       0000106E  169          CVD   R2,DECNUM
000002BE  D211 8E58 8E42      00001058    00001042  170          MVC   PRT3,EDIT
000002C4  DE11 8E58 8E6E      00001058    0000106E  171          ED    PRT3,DECNUM
000002CA  D201 8E40 8E66      00001040    00001066  172          MVC   PRTI3(2),PRT3+14     fill in message with i3 field

                                                    174 *
                                                    175 *        Use Hercules Diagnose for Message to console
                                                    176 *
000002D0  9002 80F8                       000002F8  177          STM   R0,R2,RPTDWSAV       save regs used by MSG
000002D4  4100 003E                       0000003E  178          LA    R0,PRTLNG            message length
000002D8  4110 8E04                       00001004  179          LA    R1,PRTLINE           messagfe address
000002DC  4520 8108                       00000308  180          BAL   R2,MSG               call Hercules console MSG display
000002E0  9802 80F8                       000002F8  181          LM    R0,R2,RPTDWSAV       restore regs


000002E4  5850 80F4                       000002F4  183          L     R5,RPTSVR5           Restore R5
000002E8  58F0 80F0                       000002F0  184          L     R15,RPTSAVE          Restore return address
000002EC  07FF                                      185          BR    R15                  Return to caller

000002F0  00000000                                  187 RPTSAVE  DC    F'0'                 R15 save area
000002F4  00000000                                  188 RPTSVR5  DC    F'0'                 R5 save area

000002F8  00000000 00000000                         190 RPTDWSAV DC    2D'0'                R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    192 ************************************************************************
                                                    193 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    194 *              R2 = return address
                                                    195 ************************************************************************
00000308  4900 81F8                  000003F8      197 MSG      CH    R0,=H'0'                Do we even HAVE a message?
0000030C  07D2                                     198          BNHR  R2                      No, ignore

0000030E  9002 8140                  00000340      200          STM   R0,R2,MSGSAVE           Save registers

00000312  4900 81FA                  000003FA      202          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
00000316  47D0 811E                  0000031E      203          BNH   MSGOK                   Yes, continue
0000031A  4100 005F                  0000005F      204          LA    R0,L'MSGMSG             No, set to maximum

0000031E  1820                                     206 MSGOK    LR    R2,R0                   Copy length to work register
00000320  0620                                     207          BCTR  R2,0                    Minus-1 for execute
00000322  4420 814C                  0000034C      208          EX    R2,MSGMVC               Copy message to O/P buffer

00000326  4120 200A                  0000000A      210          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
0000032A  4110 8152                  00000352      211          LA    R1,MSGCMD               Point to true command

0000032E  83120008                                 213          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
00000332  4780 8138                  00000338      214          BZ    MSGRET                  Return if successful
00000336  0000                                     215          DC    H'0'                    CRASH for debugging purposes

00000338  9802 8140                  00000340      217 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
0000033C  07F2                                     218          BR    R2                      Return to caller



00000340  00000000 00000000                        220 MSGSAVE  DC    3F'0'                   Registers save area
0000034C  D200 815B 1000      0000035B  00000000   221 MSGMVC   MVC   MSGMSG(0),0(R1)         Executed instruction


00000352  D4E2C7D5 D6C8405C                        223 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
0000035B  40404040 40404040                        224 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                   225
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     227 ********************************************************************************
                                                     228 *        Normal completion or Abnormal termination PSWs
                                                     229 ********************************************************************************

000003C0  00020001 80000000                          231 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)
000003D0  B2B2 81C0                  000003C0        233 EOJ      LPSWE EOJPSW                Normal completion

000003D8  00020001 80000000                          235 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')
000003E8  B2B2 81D8                  000003D8        237 FAILTEST LPSWE FAILPSW               Abnormal termination

                                                     239 ********************************************************************************
                                                     240 *        Working Storage
                                                     241 ********************************************************************************

000003EC  00000000                                   243 CTLR0    DS    F                    CR0
000003F0  00000000                                   244          DS    F

000003F4                                             246          LTORG ,                    Literals pool
000003F4  00000001                                   247                =F'1'
000003F8  0000                                       248                =H'0'
000003FA  005F                                       249                =AL2(L'MSGMSG)
                                                     250
                                                     251 *        some constants
                                                     252
                          00000400  00000001         253 K        EQU   1024                 One KB
                          00001000  00000001         254 PAGE     EQU   (4*K)                Size of one page
                          00010000  00000001         255 K64      EQU   (64*K)               64 KB
                          00100000  00000001         256 MB       EQU   (K*K)                 1 MB
                                                     257
                          AABBCCDD  00000001         258 REG2PATT EQU   X'AABBCCDD'    Polluted Register pattern
                          000000DD  00000001         259 REG2LOW  EQU         X'DD'    (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    261 *=========================================================================
                                                    262 *
                                                    263 *  NOTE: start data on an address that is easy to display
                                                    264 *        within Hercules
                                                    265 *
                                                    266 *=========================================================================
                                                    267
000003FC                      000003FC  00001000    268          ORG   ZVE6TST+X'1000'
00001000  00000000                                  269 FAILED   DC    F'0'                       some test failed?


                                                    271 *
                                                    272 *        failed message and associated editting
                                                    273 *
00001004  40404040 40404040                         274 PRTLINE  DC    C'         Test # '
00001014  A7A7A7                                    275 PRTNUM   DC    C'xxx'
00001017  40868189 93858440                         276          DC    c' failed for instruction '
0000102F  A7A7A7A7 A7A7A7A7                         277 PRTNAME  DC    CL8'xxxxxxxx'
00001037  40A689A3 884089F3                         278          DC    C' with i3='
00001040  A7                                        279 PRTI3    DC    C'x'
00001041  4B                                        280          DC    C'.'
                              0000003E  00000001    281 PRTLNG   EQU   *-PRTLINE
00001042  40212020 20202020                        282 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                    283
00001054  7E7E7E6E                                  284          DC    C'===>'
00001058  40404040 40404040                         285 PRT3     DC    CL18' '
0000106A  4C7E7E7E                                  286          DC    C'<===='
0000106E  00000000 00000000                         287 DECNUM   DS    CL16


                                                    289 *
                                                    290 *        Vector instruction results, pollution and input
                                                    291 *
0000107E  E5F140D6 A4A397A4                         292          DC    C'V1 Output ===>'
0000108C                                            293          DS    0F
0000108C  00000000 00000000                         294 V1OUTPUT DS    XL16                                        V1 OUTPUT
0000109C  00000000 00000000                         295          DS    XL16
000010AC  00000000 00000000                         296          DS    XL16                                  a gap between
000010BC  FFFFFFFF FFFFFFFF                         297 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010CC  12345678 90123456                         298 V1INPUT  DC    XL16'1234567890123456789012345678901D'    V1 input
000010DC  00000000 00000000                         299          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     301 ************************************************************************
                                                     302 *        E6TEST DSECT
                                                     303 ************************************************************************


                                                     305 E6TEST   DSECT ,
00000000  00000000                                   306 TSUB     DC    A(0)           pointer  to test
00000004  0000                                       307 TNUM     DC    H'00'          Test Number
00000006  00                                         308          DC    X'00'
00000007  00                                         309 I3       DC    HL1'00'        i3 used
                                                     310
00000008  40404040 40404040                          311 OPNAME   DC    CL8' '         E6 name
00000010  00000000                                   312 RELEN    DC    A(0)           RESULT LENGTH
00000014  00000000                                   313 RESULT   DC    A(0)
                                                     314 *        EXPECTED RESULT
                                                     315 **
                                                     316 *        test routine will be here (from VSI macro)


                          00000000  000018DB         318 ZVE6TST  CSECT ,
000010EC                                             319          DS    0F


                                                     321 ************************************************************************
                                                     322 *     Macros to help build test tables
                                                     323 ************************************************************************


                                                     325 *
                                                     326 * macro to generate individual test
                                                     327 *
                                                     328          MACRO
                                                     329          VSI   &INST,&I3
                                                     330          LCLA  &A3
                                                     331 &A3      SETA  &I3
                                                     332 .*                              &INST - VSI instruction under test
                                                     333 .*                              &i3   - i3 field
                                                     334          GBLA  &TNUM
                                                     335 &TNUM    SETA  &TNUM+1
                                                     336 .*                              set result compare length
                                                     337          LCLA  &RLEN
                                                     338 &RLEN    SETA  16
                                                     339          AIF   (&A3 LE 15).GEN
                                                     340 &RLEN    SETA  32
                                                     341 .GEN     ANOP
                                                     342 .*         MNOTE 0,'Result compare length = &RLEN.'
                                                     343
                                                     344          DS    0FD
                                                     345          USING *,R5               base for test data and test routine
                                                     346
                                                     347 T&TNUM   DC    A(X&TNUM)          address of test routine
                                                     348          DC    H'&TNUM'           test number
                                                     349          DC    X'00'
                                                     350          DC    HL1'&I3'            i3
                                                     351          DC    CL8'&INST'         instruction name
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      352          DC    A(&RLEN)          result length
                                                      353          DC    A(RE&TNUM)        address of expected result
                                                      354 .*
                                                      355 *
                                                      356 X&TNUM   DS    0F
                                                      357          &INST V1,V1OUTPUT,&I3    test instruction
                                                      358          BR    R11               return
                                                      359 .*
                                                      360 RE&TNUM  DS    0F           expected  16 or 32 byte result
                                                      361
                                                      362          DROP  R5
                                                      363          MEND



                                                      365 *
                                                      366 * macro to generate table of pointers to individual tests
                                                      367 *
                                                      368          MACRO
                                                      369          PTTABLE
                                                      370          GBLA  &TNUM
                                                      371          LCLA  &CUR
                                                      372 &CUR     SETA  1
                                                      373 .*
                                                      374 TTABLE   DS    0F
                                                      375 .LOOP    ANOP
                                                      376 .*
                                                      377          DC    A(T&CUR)          TEST &CUR
                                                      378 .*
                                                      379 &CUR     SETA  &CUR+1
                                                      380          AIF   (&CUR LE &TNUM).LOOP
                                                      381 *
                                                      382          DC    A(0)              END OF TABLE
                                                      383          DC    A(0)
                                                      384 .*
                                                      385          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    387 ********************************************************************************
                                                    388 *        E6 VSI UNPACK/STORE load tests
                                                    389 ********************************************************************************
                                                    390          PRINT DATA
                                                    391
                                                    392 *        E63C VUPKZ   - VECTOR UNPACK ZONED
                                                    393 *        E63D VSTRL   - VECTOR STORE RIGHTMOST WITH LENGTH
                                                    394
                                                    395 *--------------------------------------------------------------------
                                                    396 * VUPKZ   - VECTOR UNPACK ZONED
                                                    397 *--------------------------------------------------------------------
                                                    398 *   VSI   instruction, i3
                                                    399 *   followed by 16 (i3 <=15 ) or 32 (i3 >= 16) byte expected result
                                                    400 *        (Note: FF initialized)
                                                    401
                                                    402          VSI   VUPKZ,00
000010F0                                            403+         DS    0FD
000010F0                        000010F0            404+         USING *,R5              base for test data and test routine
000010F0  00001108                                  405+T1       DC    A(X1)             address of test routine
000010F4  0001                                      406+         DC    H'1'              test number
000010F6  00                                        407+         DC    X'00'
000010F7  00                                        408+         DC    HL1'00'            i3
000010F8  E5E4D7D2 E9404040                         409+         DC    CL8'VUPKZ'        instruction name
00001100  00000010                                  410+         DC    A(16)             result length
00001104  00001110                                  411+         DC    A(RE1)            address of expected result
                                                    412+*
00001108                                            413+X1       DS    0F
00001108  E600 8E8C 103C                0000108C    414+         VUPKZ V1,V1OUTPUT,00     test instruction
0000110E  07FB                                      415+         BR    R11               return
00001110                                            416+RE1      DS    0F           expected  16 or 32 byte result
00001110                                            417+         DROP  R5
00001110  D1FFFFFF FFFFFFFF                        418          DC    XL16'D1FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001118  FFFFFFFF FFFFFFFF
                                                    419
                                                    420          VSI   VUPKZ,01
00001120                                            421+         DS    0FD
00001120                        00001120            422+         USING *,R5              base for test data and test routine
00001120  00001138                                  423+T2       DC    A(X2)             address of test routine
00001124  0002                                      424+         DC    H'2'              test number
00001126  00                                        425+         DC    X'00'
00001127  01                                        426+         DC    HL1'01'            i3
00001128  E5E4D7D2 E9404040                         427+         DC    CL8'VUPKZ'        instruction name
00001130  00000010                                  428+         DC    A(16)             result length
00001134  00001140                                  429+         DC    A(RE2)            address of expected result
                                                    430+*
00001138                                            431+X2       DS    0F
00001138  E601 8E8C 103C                0000108C    432+         VUPKZ V1,V1OUTPUT,01     test instruction
0000113E  07FB                                      433+         BR    R11               return
00001140                                            434+RE2      DS    0F           expected  16 or 32 byte result
00001140                                            435+         DROP  R5
00001140  F0D1FFFF FFFFFFFF                        436          DC    XL16'F0D1FFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001148  FFFFFFFF FFFFFFFF
                                                    437
                                                    438          VSI   VUPKZ,02
00001150                                            439+         DS    0FD
00001150                        00001150            440+         USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001150  00001168                            441+T3       DC    A(X3)              address of test routine
00001154  0003                                442+         DC    H'3'               test number
00001156  00                                  443+         DC    X'00'
00001157  02                                  444+         DC    HL1'02'             i3
00001158  E5E4D7D2 E9404040                   445+         DC    CL8'VUPKZ'         instruction name
00001160  00000010                            446+         DC    A(16)              result length
00001164  00001170                            447+         DC    A(RE3)             address of expected result
                                              448+*
00001168                                      449+X3       DS    0F
00001168  E602 8E8C 103C              0000108C 450+         VUPKZ V1,V1OUTPUT,02     test instruction
0000116E  07FB                                451+         BR    R11                return
00001170                                      452+RE3      DS    0F           expected  16 or 32 byte result
00001170                                      453+         DROP  R5
00001170  F9F0D1FF FFFFFFFF                   454          DC    XL16'F9F0D1FFFFFFFFFFFFFFFFFFFFFFFF'
00001178  FFFFFFFF FFFFFFFF
                                              455
                                              456          VSI   VUPKZ,03
00001180                                      457+         DS    0FD
00001180                      00001180        458+         USING *,R5               base for test data and test routine
00001180  00001198                            459+T4       DC    A(X4)              address of test routine
00001184  0004                                460+         DC    H'4'               test number
00001186  00                                  461+         DC    X'00'
00001187  03                                  462+         DC    HL1'03'             i3
00001188  E5E4D7D2 E9404040                   463+         DC    CL8'VUPKZ'         instruction name
00001190  00000010                            464+         DC    A(16)              result length
00001194  000011A0                            465+         DC    A(RE4)             address of expected result
                                              466+*
00001198                                      467+X4       DS    0F
00001198  E603 8E8C 103C              0000108C 468+         VUPKZ V1,V1OUTPUT,03     test instruction
0000119E  07FB                                469+         BR    R11                return
000011A0                                      470+RE4      DS    0F           expected  16 or 32 byte result
000011A0                                      471+         DROP  R5
000011A0  F8F9F0D1 FFFFFFFF                   472          DC    XL16'F8F9F0D1FFFFFFFFFFFFFFFFFFFFFFFF'
000011A8  FFFFFFFF FFFFFFFF
                                              473
                                              474          VSI   VUPKZ,04
000011B0                                      475+         DS    0FD
000011B0                      000011B0        476+         USING *,R5               base for test data and test routine
000011B0  000011C8                            477+T5       DC    A(X5)              address of test routine
000011B4  0005                                478+         DC    H'5'               test number
000011B6  00                                  479+         DC    X'00'
000011B7  04                                  480+         DC    HL1'04'             i3
000011B8  E5E4D7D2 E9404040                   481+         DC    CL8'VUPKZ'         instruction name
000011C0  00000010                            482+         DC    A(16)              result length
000011C4  000011D0                            483+         DC    A(RE5)             address of expected result
                                              484+*
000011C8                                      485+X5       DS    0F
000011C8  E604 8E8C 103C              0000108C 486+         VUPKZ V1,V1OUTPUT,04     test instruction
000011CE  07FB                                487+         BR    R11                return
000011D0                                      488+RE5      DS    0F           expected  16 or 32 byte result
000011D0                                      489+         DROP  R5
000011D0  F7F8F9F0 D1FFFFFF                   490          DC    XL16'F7F8F9F0D1FFFFFFFFFFFFFFFFFFFFFF'
000011D8  FFFFFFFF FFFFFFFF
                                              491
                                              492          VSI   VUPKZ,05
000011E0                                      493+         DS    0FD
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000011E0                     000011E0               494+         USING *,R5              base for test data and test routine
000011E0  000011F8                                  495+T6       DC    A(X6)             address of test routine
000011E4  0006                                      496+         DC    H'6'              test number
000011E6  00                                        497+         DC    X'00'
000011E7  05                                        498+         DC    HL1'05'            i3
000011E8  E5E4D7D2 E9404040                         499+         DC    CL8'VUPKZ'        instruction name
000011F0  00000010                                  500+         DC    A(16)             result length
000011F4  00001200                                  501+         DC    A(RE6)            address of expected result
                                                    502+*
000011F8                                            503+X6       DS    0F
000011F8  E605 8E8C 103C                0000108C    504+         VUPKZ V1,V1OUTPUT,05     test instruction
000011FE  07FB                                      505+         BR    R11               return
00001200                                            506+RE6      DS    0F           expected  16 or 32 byte result
00001200                                            507+         DROP  R5
00001200  F6F7F8F9 F0D1FFFF                         508          DC    XL16'F6F7F8F9F0D1FFFFFFFFFFFFFFFFFFFF'
00001208  FFFFFFFF FFFFFFFF
                                                    509
                                                    510          VSI   VUPKZ,06
00001210                                            511+         DS    0FD
00001210                     00001210               512+         USING *,R5              base for test data and test routine
00001210  00001228                                  513+T7       DC    A(X7)             address of test routine
00001214  0007                                      514+         DC    H'7'              test number
00001216  00                                        515+         DC    X'00'
00001217  06                                        516+         DC    HL1'06'            i3
00001218  E5E4D7D2 E9404040                         517+         DC    CL8'VUPKZ'        instruction name
00001220  00000010                                  518+         DC    A(16)             result length
00001224  00001230                                  519+         DC    A(RE7)            address of expected result
                                                    520+*
00001228                                            521+X7       DS    0F
00001228  E606 8E8C 103C                0000108C    522+         VUPKZ V1,V1OUTPUT,06     test instruction
0000122E  07FB                                      523+         BR    R11               return
00001230                                            524+RE7      DS    0F           expected  16 or 32 byte result
00001230                                            525+         DROP  R5
00001230  F5F6F7F8 F9F0D1FF                         526          DC    XL16'F5F6F7F8F9F0D1FFFFFFFFFFFFFFFFFF'
00001238  FFFFFFFF FFFFFFFF
                                                    527
                                                    528          VSI   VUPKZ,07
00001240                                            529+         DS    0FD
00001240                     00001240               530+         USING *,R5              base for test data and test routine
00001240  00001258                                  531+T8       DC    A(X8)             address of test routine
00001244  0008                                      532+         DC    H'8'              test number
00001246  00                                        533+         DC    X'00'
00001247  07                                        534+         DC    HL1'07'            i3
00001248  E5E4D7D2 E9404040                         535+         DC    CL8'VUPKZ'        instruction name
00001250  00000010                                  536+         DC    A(16)             result length
00001254  00001260                                  537+         DC    A(RE8)            address of expected result
                                                    538+*
00001258                                            539+X8       DS    0F
00001258  E607 8E8C 103C                0000108C    540+         VUPKZ V1,V1OUTPUT,07     test instruction
0000125E  07FB                                      541+         BR    R11               return
00001260                                            542+RE8      DS    0F           expected  16 or 32 byte result
00001260                                            543+         DROP  R5
00001260  F4F5F6F7 F8F9F0D1                         544          DC    XL16'F4F5F6F7F8F9F0D1FFFFFFFFFFFFFFFF'
00001268  FFFFFFFF FFFFFFFF
                                                    545
                                                    546          VSI   VUPKZ,08
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001270                                           547+          DS    0FD
00001270                     00001270              548+          USING *,R5              base for test data and test routine
00001270  00001288                                 549+T9        DC    A(X9)             address of test routine
00001274  0009                                     550+          DC    H'9'              test number
00001276  00                                       551+          DC    X'00'
00001277  08                                       552+          DC    HL1'08'            i3
00001278  E5E4D7D2 E9404040                        553+          DC    CL8'VUPKZ'        instruction name
00001280  00000010                                 554+          DC    A(16)             result length
00001284  00001290                                 555+          DC    A(RE9)            address of expected result
                                                   556+*
00001288                                           557+X9        DS    0F
00001288  E608 8E8C 103C               0000108C    558+          VUPKZ V1,V1OUTPUT,08     test instruction
0000128E  07FB                                     559+          BR    R11               return
00001290                                           560+RE9       DS    0F           expected  16 or 32 byte result
00001290                                           561+          DROP  R5
00001290  F3F4F5F6 F7F8F9F0                        562           DC    XL16'F3F4F5F6F7F8F9F0D1FFFFFFFFFFFFFF'
00001298  D1FFFFFF FFFFFFFF
                                                   563
                                                   564           VSI   VUPKZ,09
000012A0                                           565+          DS    0FD
000012A0                     000012A0              566+          USING *,R5              base for test data and test routine
000012A0  000012B8                                 567+T10       DC    A(X10)            address of test routine
000012A4  000A                                     568+          DC    H'10'             test number
000012A6  00                                       569+          DC    X'00'
000012A7  09                                       570+          DC    HL1'09'            i3
000012A8  E5E4D7D2 E9404040                        571+          DC    CL8'VUPKZ'        instruction name
000012B0  00000010                                 572+          DC    A(16)             result length
000012B4  000012C0                                 573+          DC    A(RE10)           address of expected result
                                                   574+*
000012B8                                           575+X10       DS    0F
000012B8  E609 8E8C 103C               0000108C    576+          VUPKZ V1,V1OUTPUT,09     test instruction
000012BE  07FB                                     577+          BR    R11               return
000012C0                                           578+RE10      DS    0F           expected  16 or 32 byte result
000012C0                                           579+          DROP  R5
000012C0  F2F3F4F5 F6F7F8F9                        580           DC    XL16'F2F3F4F5F6F7F8F9F0D1FFFFFFFFFFFF'
000012C8  F0D1FFFF FFFFFFFF
                                                   581
                                                   582           VSI   VUPKZ,10
000012D0                                           583+          DS    0FD
000012D0                     000012D0              584+          USING *,R5              base for test data and test routine
000012D0  000012E8                                 585+T11       DC    A(X11)            address of test routine
000012D4  000B                                     586+          DC    H'11'             test number
000012D6  00                                       587+          DC    X'00'
000012D7  0A                                       588+          DC    HL1'10'            i3
000012D8  E5E4D7D2 E9404040                        589+          DC    CL8'VUPKZ'        instruction name
000012E0  00000010                                 590+          DC    A(16)             result length
000012E4  000012F0                                 591+          DC    A(RE11)           address of expected result
                                                   592+*
000012E8                                           593+X11       DS    0F
000012E8  E60A 8E8C 103C               0000108C    594+          VUPKZ V1,V1OUTPUT,10     test instruction
000012EE  07FB                                     595+          BR    R11               return
000012F0                                           596+RE11      DS    0F           expected  16 or 32 byte result
000012F0                                           597+          DROP  R5
000012F0  F1F2F3F4 F5F6F7F8                        598           DC    XL16'F1F2F3F4F5F6F7F8F9F0D1FFFFFFFFFF'
000012F8  F9F0D1FF FFFFFFFF
                                                   599
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     600          VSI   VUPKZ,11
00001300                                             601+         DS    0FD
00001300                       00001300              602+         USING *,R5              base for test data and test routine
00001300  00001318                                   603+T12      DC    A(X12)            address of test routine
00001304  000C                                       604+         DC    H'12'             test number
00001306  00                                         605+         DC    X'00'
00001307  0B                                         606+         DC    HL1'11'            i3
00001308  E5E4D7D2 E9404040                         607+         DC    CL8'VUPKZ'        instruction name
00001310  00000010                                   608+         DC    A(16)             result length
00001314  00001320                                   609+         DC    A(RE12)           address of expected result
                                                     610+*
00001318                                             611+X12      DS    0F
00001318  E60B 8E8C 103C                0000108C     612+         VUPKZ V1,V1OUTPUT,11     test instruction
0000131E  07FB                                       613+         BR    R11               return
00001320                                             614+RE12     DS    0F           expected  16 or 32 byte result
00001320                                             615+         DROP  R5
00001320  F0F1F2F3 F4F5F6F7                          616          DC    XL16'F0F1F2F3F4F5F6F7F8F9F0D1FFFFFFFF'
00001328  F8F9F0D1 FFFFFFFF
                                                     617
                                                     618          VSI   VUPKZ,12
00001330                                             619+         DS    0FD
00001330                       00001330              620+         USING *,R5              base for test data and test routine
00001330  00001348                                   621+T13      DC    A(X13)            address of test routine
00001334  000D                                       622+         DC    H'13'             test number
00001336  00                                         623+         DC    X'00'
00001337  0C                                         624+         DC    HL1'12'            i3
00001338  E5E4D7D2 E9404040                         625+         DC    CL8'VUPKZ'        instruction name
00001340  00000010                                   626+         DC    A(16)             result length
00001344  00001350                                   627+         DC    A(RE13)           address of expected result
                                                     628+*
00001348                                             629+X13      DS    0F
00001348  E60C 8E8C 103C                0000108C     630+         VUPKZ V1,V1OUTPUT,12     test instruction
0000134E  07FB                                       631+         BR    R11               return
00001350                                             632+RE13     DS    0F           expected  16 or 32 byte result
00001350                                             633+         DROP  R5
00001350  F9F0F1F2 F3F4F5F6                          634          DC    XL16'F9F0F1F2F3F4F5F6F7F8F9F0D1FFFFFF'
00001358  F7F8F9F0 D1FFFFFF
                                                     635
                                                     636          VSI   VUPKZ,13
00001360                                             637+         DS    0FD
00001360                       00001360              638+         USING *,R5              base for test data and test routine
00001360  00001378                                   639+T14      DC    A(X14)            address of test routine
00001364  000E                                       640+         DC    H'14'             test number
00001366  00                                         641+         DC    X'00'
00001367  0D                                         642+         DC    HL1'13'            i3
00001368  E5E4D7D2 E9404040                         643+         DC    CL8'VUPKZ'        instruction name
00001370  00000010                                   644+         DC    A(16)             result length
00001374  00001380                                   645+         DC    A(RE14)           address of expected result
                                                     646+*
00001378                                             647+X14      DS    0F
00001378  E60D 8E8C 103C                0000108C     648+         VUPKZ V1,V1OUTPUT,13     test instruction
0000137E  07FB                                       649+         BR    R11               return
00001380                                             650+RE14     DS    0F           expected  16 or 32 byte result
00001380                                             651+         DROP  R5
00001380  F8F9F0F1 F2F3F4F5                          652          DC    XL16'F8F9F0F1F2F3F4F5F6F7F8F9F0D1FFFF'
00001388  F6F7F8F9 F0D1FFFF
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     653
                                                     654          VSI   VUPKZ,14
00001390                                             655+         DS    0FD
00001390                       00001390              656+         USING *,R5              base for test data and test routine
00001390  000013A8                                   657+T15      DC    A(X15)            address of test routine
00001394  000F                                       658+         DC    H'15'             test number
00001396  00                                         659+         DC    X'00'
00001397  0E                                         660+         DC    HL1'14'            i3
00001398  E5E4D7D2 E9404040                          661+         DC    CL8'VUPKZ'        instruction name
000013A0  00000010                                   662+         DC    A(16)             result length
000013A4  000013B0                                   663+         DC    A(RE15)           address of expected result
                                                     664+*
000013A8                                             665+X15      DS    0F
000013A8  E60E 8E8C 103C                0000108C     666+         VUPKZ V1,V1OUTPUT,14     test instruction
000013AE  07FB                                       667+         BR    R11               return
000013B0                                             668+RE15     DS    0F           expected  16 or 32 byte result
000013B0                                             669+         DROP  R5
000013B0  F7F8F9F0 F1F2F3F4                          670          DC    XL16'F7F8F9F0F1F2F3F4F5F6F7F8F9F0D1FF'
000013B8  F5F6F7F8 F9F0D1FF
                                                     671
                                                     672          VSI   VUPKZ,15
000013C0                                             673+         DS    0FD
000013C0                       000013C0              674+         USING *,R5              base for test data and test routine
000013C0  000013D8                                   675+T16      DC    A(X16)            address of test routine
000013C4  0010                                       676+         DC    H'16'             test number
000013C6  00                                         677+         DC    X'00'
000013C7  0F                                         678+         DC    HL1'15'            i3
000013C8  E5E4D7D2 E9404040                          679+         DC    CL8'VUPKZ'        instruction name
000013D0  00000010                                   680+         DC    A(16)             result length
000013D4  000013E0                                   681+         DC    A(RE16)           address of expected result
                                                     682+*
000013D8                                             683+X16      DS    0F
000013D8  E60F 8E8C 103C                0000108C     684+         VUPKZ V1,V1OUTPUT,15     test instruction
000013DE  07FB                                       685+         BR    R11               return
000013E0                                             686+RE16     DS    0F           expected  16 or 32 byte result
000013E0                                             687+         DROP  R5
000013E0  F6F7F8F9 F0F1F2F3                          688          DC    XL16'F6F7F8F9F0F1F2F3F4F5F6F7F8F9F0D1'
000013E8  F4F5F6F7 F8F9F0D1
                                                     689
                                                     690          VSI   VUPKZ,16
000013F0                                             691+         DS    0FD
000013F0                       000013F0              692+         USING *,R5              base for test data and test routine
000013F0  00001408                                   693+T17      DC    A(X17)            address of test routine
000013F4  0011                                       694+         DC    H'17'             test number
000013F6  00                                         695+         DC    X'00'
000013F7  10                                         696+         DC    HL1'16'            i3
000013F8  E5E4D7D2 E9404040                          697+         DC    CL8'VUPKZ'        instruction name
00001400  00000020                                   698+         DC    A(32)             result length
00001404  00001410                                   699+         DC    A(RE17)           address of expected result
                                                     700+*
00001408                                             701+X17      DS    0F
00001408  E610 8E8C 103C                0000108C     702+         VUPKZ V1,V1OUTPUT,16     test instruction
0000140E  07FB                                       703+         BR    R11               return
00001410                                             704+RE17     DS    0F           expected  16 or 32 byte result
00001410                                             705+         DROP  R5
00001410  F5F6F7F8 F9F0F1F2                          706          DC    XL16'F5F6F7F8F9F0F1F2F3F4F5F6F7F8F9F0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001418  F3F4F5F6 F7F8F9F0
00001420  D1FFFFFF FFFFFFFF                          707          DC    XL16'D1FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001428  FFFFFFFF FFFFFFFF
                                                     708
                                                     709          VSI   VUPKZ,17
00001430                                             710+         DS    0FD
00001430                     00001430                711+         USING *,R5              base for test data and test routine
00001430  00001448                                   712+T18      DC    A(X18)            address of test routine
00001434  0012                                       713+         DC    H'18'             test number
00001436  00                                         714+         DC    X'00'
00001437  11                                         715+         DC    HL1'17'            i3
00001438  E5E4D7D2 E9404040                         716+         DC    CL8'VUPKZ'        instruction name
00001440  00000020                                   717+         DC    A(32)             result length
00001444  00001450                                   718+         DC    A(RE18)           address of expected result
                                                     719+*
00001448                                             720+X18      DS    0F
00001448  E611 8E8C 103C               0000108C      721+         VUPKZ V1,V1OUTPUT,17     test instruction
0000144E  07FB                                       722+         BR    R11               return
00001450                                             723+RE18     DS    0F           expected  16 or 32 byte result
00001450                                             724+         DROP  R5
00001450  F4F5F6F7 F8F9F0F1                          725          DC    XL16'F4F5F6F7F8F9F0F1F2F3F4F5F6F7F8F9'
00001458  F2F3F4F5 F6F7F8F9
00001460  F0D1FFFF FFFFFFFF                          726          DC    XL16'F0D1FFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001468  FFFFFFFF FFFFFFFF
                                                     727
                                                     728          VSI   VUPKZ,18
00001470                                             729+         DS    0FD
00001470                     00001470                730+         USING *,R5              base for test data and test routine
00001470  00001488                                   731+T19      DC    A(X19)            address of test routine
00001474  0013                                       732+         DC    H'19'             test number
00001476  00                                         733+         DC    X'00'
00001477  12                                         734+         DC    HL1'18'            i3
00001478  E5E4D7D2 E9404040                         735+         DC    CL8'VUPKZ'        instruction name
00001480  00000020                                   736+         DC    A(32)             result length
00001484  00001490                                   737+         DC    A(RE19)           address of expected result
                                                     738+*
00001488                                             739+X19      DS    0F
00001488  E612 8E8C 103C               0000108C      740+         VUPKZ V1,V1OUTPUT,18     test instruction
0000148E  07FB                                       741+         BR    R11               return
00001490                                             742+RE19     DS    0F           expected  16 or 32 byte result
00001490                                             743+         DROP  R5
00001490  F3F4F5F6 F7F8F9F0                          744          DC    XL16'F3F4F5F6F7F8F9F0F1F2F3F4F5F6F7F8'
00001498  F1F2F3F4 F5F6F7F8
000014A0  F9F0D1FF FFFFFFFF                          745          DC    XL16'F9F0D1FFFFFFFFFFFFFFFFFFFFFFFFFF'
000014A8  FFFFFFFF FFFFFFFF
                                                     746
                                                     747 ** SKIPPING TO
                                                     748
                                                     749          VSI   VUPKZ,29
000014B0                                             750+         DS    0FD
000014B0                     000014B0                751+         USING *,R5              base for test data and test routine
000014B0  000014C8                                   752+T20      DC    A(X20)            address of test routine
000014B4  0014                                       753+         DC    H'20'             test number
000014B6  00                                         754+         DC    X'00'
000014B7  1D                                         755+         DC    HL1'29'            i3
000014B8  E5E4D7D2 E9404040                         756+         DC    CL8'VUPKZ'        instruction name
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000014C0  00000020                             757+         DC    A(32)             result length
000014C4  000014D0                             758+         DC    A(RE20)           address of expected result
                                               759+*
000014C8                                       760+X20      DS    0F
000014C8  E61D 8E8C 103C                0000108C 761+         VUPKZ V1,V1OUTPUT,29     test instruction
000014CE  07FB                                 762+         BR    R11               return
000014D0                                       763+RE20     DS    0F           expected  16 or 32 byte result
000014D0                                       764+         DROP  R5
000014D0  F2F3F4F5 F6F7F8F9                    765          DC    XL16'F2F3F4F5F6F7F8F9F0F1F2F3F4F5F6F7'
000014D8  F0F1F2F3 F4F5F6F7
000014E0  F8F9F0F1 F2F3F4F5                    766          DC    XL16'F8F9F0F1F2F3F4F5F6F7F8F9F0D1FFFF'
000014E8  F6F7F8F9 F0D1FFFF
                                               767
                                               768          VSI   VUPKZ,30
000014F0                                       769+         DS    0FD
000014F0                       000014F0        770+         USING *,R5              base for test data and test routine
000014F0  00001508                             771+T21      DC    A(X21)            address of test routine
000014F4  0015                                 772+         DC    H'21'             test number
000014F6  00                                   773+         DC    X'00'
000014F7  1E                                   774+         DC    HL1'30'            i3
000014F8  E5E4D7D2 E9404040                    775+         DC    CL8'VUPKZ'        instruction name
00001500  00000020                             776+         DC    A(32)             result length
00001504  00001510                             777+         DC    A(RE21)           address of expected result
                                               778+*
00001508                                       779+X21      DS    0F
00001508  E61E 8E8C 103C                0000108C 780+         VUPKZ V1,V1OUTPUT,30     test instruction
0000150E  07FB                                 781+         BR    R11               return
00001510                                       782+RE21     DS    0F           expected  16 or 32 byte result
00001510                                       783+         DROP  R5
00001510  F1F2F3F4 F5F6F7F8                    784          DC    XL16'F1F2F3F4F5F6F7F8F9F0F1F2F3F4F5F6'
00001518  F9F0F1F2 F3F4F5F6
00001520  F7F8F9F0 F1F2F3F4                    785          DC    XL16'F7F8F9F0F1F2F3F4F5F6F7F8F9F0D1FF'
00001528  F5F6F7F8 F9F0D1FF
                                               786
                                               787 *-------------------------------------------------------------------
                                               788 *  VSTRL   - VECTOR STORE RIGHTMOST WITH LENGTH
                                               789 *-------------------------------------------------------------------
                                               790 *        VSI   instruction, i3
                                               791 *        followed by 32 bytes expected result (Note: FF initialized)
                                               792
                                               793          VSI   VSTRL,00
00001530                                       794+         DS    0FD
00001530                       00001530        795+         USING *,R5              base for test data and test routine
00001530  00001548                             796+T22      DC    A(X22)            address of test routine
00001534  0016                                 797+         DC    H'22'             test number
00001536  00                                   798+         DC    X'00'
00001537  00                                   799+         DC    HL1'00'            i3
00001538  E5E2E3D9 D3404040                    800+         DC    CL8'VSTRL'        instruction name
00001540  00000010                             801+         DC    A(16)             result length
00001544  00001550                             802+         DC    A(RE22)           address of expected result
                                               803+*
00001548                                       804+X22      DS    0F
00001548  E600 8E8C 103D                0000108C 805+         VSTRL V1,V1OUTPUT,00     test instruction
0000154E  07FB                                 806+         BR    R11               return
00001550                                       807+RE22     DS    0F           expected  16 or 32 byte result
00001550                                       808+         DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
00001550  1DFFFFFF FFFFFFFF                    809          DC    XL16'1DFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001558  FFFFFFFF FFFFFFFF
                                               810
                                               811          VSI   VSTRL,01
00001560                                       812+         DS    0FD
00001560                      00001560         813+         USING *,R5              base for test data and test routine
00001560  00001578                             814+T23      DC    A(X23)            address of test routine
00001564  0017                                 815+         DC    H'23'             test number
00001566  00                                   816+         DC    X'00'
00001567  01                                   817+         DC    HL1'01'            i3
00001568  E5E2E3D9 D3404040                    818+         DC    CL8'VSTRL'        instruction name
00001570  00000010                             819+         DC    A(16)             result length
00001574  00001580                             820+         DC    A(RE23)           address of expected result
                                               821+*
00001578                                       822+X23      DS    0F
00001578  E601 8E8C 103D              0000108C 823+         VSTRL V1,V1OUTPUT,01     test instruction
0000157E  07FB                                 824+         BR    R11               return
00001580                                       825+RE23     DS    0F           expected  16 or 32 byte result
00001580                                       826+         DROP  R5
00001580  901DFFFF FFFFFFFF                    827          DC    XL16'901DFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00001588  FFFFFFFF FFFFFFFF
                                               828
                                               829          VSI   VSTRL,02
00001590                                       830+         DS    0FD
00001590                      00001590         831+         USING *,R5              base for test data and test routine
00001590  000015A8                             832+T24      DC    A(X24)            address of test routine
00001594  0018                                 833+         DC    H'24'             test number
00001596  00                                   834+         DC    X'00'
00001597  02                                   835+         DC    HL1'02'            i3
00001598  E5E2E3D9 D3404040                    836+         DC    CL8'VSTRL'        instruction name
000015A0  00000010                             837+         DC    A(16)             result length
000015A4  000015B0                             838+         DC    A(RE24)           address of expected result
                                               839+*
000015A8                                       840+X24      DS    0F
000015A8  E602 8E8C 103D              0000108C 841+         VSTRL V1,V1OUTPUT,02     test instruction
000015AE  07FB                                 842+         BR    R11               return
000015B0                                       843+RE24     DS    0F           expected  16 or 32 byte result
000015B0                                       844+         DROP  R5
000015B0  78901DFF FFFFFFFF                    845          DC    XL16'78901DFFFFFFFFFFFFFFFFFFFFFFFF'
000015B8  FFFFFFFF FFFFFFFF
                                               846
                                               847          VSI   VSTRL,03
000015C0                                       848+         DS    0FD
000015C0                      000015C0         849+         USING *,R5              base for test data and test routine
000015C0  000015D8                             850+T25      DC    A(X25)            address of test routine
000015C4  0019                                 851+         DC    H'25'             test number
000015C6  00                                   852+         DC    X'00'
000015C7  03                                   853+         DC    HL1'03'            i3
000015C8  E5E2E3D9 D3404040                    854+         DC    CL8'VSTRL'        instruction name
000015D0  00000010                             855+         DC    A(16)             result length
000015D4  000015E0                             856+         DC    A(RE25)           address of expected result
                                               857+*
000015D8                                       858+X25      DS    0F
000015D8  E603 8E8C 103D              0000108C 859+         VSTRL V1,V1OUTPUT,03     test instruction
000015DE  07FB                                 860+         BR    R11               return
000015E0                                       861+RE25     DS    0F           expected  16 or 32 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
000015E0                                            862+          DROP  R5
000015E0  5678901D FFFFFFFF                         863           DC    XL16'5678901DFFFFFFFFFFFFFFFFFFFFFFFF'
000015E8  FFFFFFFF FFFFFFFF
                                                    864
                                                    865           VSI   VSTRL,04
000015F0                                            866+          DS    0FD
000015F0                      000015F0              867+          USING *,R5              base for test data and test routine
000015F0  00001608                                  868+T26       DC    A(X26)            address of test routine
000015F4  001A                                      869+          DC    H'26'             test number
000015F6  00                                        870+          DC    X'00'
000015F7  04                                        871+          DC    HL1'04'            i3
000015F8  E5E2E3D9 D3404040                         872+          DC    CL8'VSTRL'        instruction name
00001600  00000010                                  873+          DC    A(16)             result length
00001604  00001610                                  874+          DC    A(RE26)           address of expected result
                                                    875+*
00001608                                            876+X26       DS    0F
00001608  E604 8E8C 103D                0000108C    877+          VSTRL V1,V1OUTPUT,04     test instruction
0000160E  07FB                                      878+          BR    R11               return
00001610                                            879+RE26      DS    0F           expected  16 or 32 byte result
00001610                                            880+          DROP  R5
00001610  34567890 1DFFFFFF                         881           DC    XL16'345678901DFFFFFFFFFFFFFFFFFFFFFF'
00001618  FFFFFFFF FFFFFFFF
                                                    882
                                                    883           VSI   VSTRL,05
00001620                                            884+          DS    0FD
00001620                      00001620              885+          USING *,R5              base for test data and test routine
00001620  00001638                                  886+T27       DC    A(X27)            address of test routine
00001624  001B                                      887+          DC    H'27'             test number
00001626  00                                        888+          DC    X'00'
00001627  05                                        889+          DC    HL1'05'            i3
00001628  E5E2E3D9 D3404040                         890+          DC    CL8'VSTRL'        instruction name
00001630  00000010                                  891+          DC    A(16)             result length
00001634  00001640                                  892+          DC    A(RE27)           address of expected result
                                                    893+*
00001638                                            894+X27       DS    0F
00001638  E605 8E8C 103D                0000108C    895+          VSTRL V1,V1OUTPUT,05     test instruction
0000163E  07FB                                      896+          BR    R11               return
00001640                                            897+RE27      DS    0F           expected  16 or 32 byte result
00001640                                            898+          DROP  R5
00001640  12345678 901DFFFF                         899           DC    XL16'12345678901DFFFFFFFFFFFFFFFFFFFF'
00001648  FFFFFFFF FFFFFFFF
                                                    900
                                                    901           VSI   VSTRL,06
00001650                                            902+          DS    0FD
00001650                      00001650              903+          USING *,R5              base for test data and test routine
00001650  00001668                                  904+T28       DC    A(X28)            address of test routine
00001654  001C                                      905+          DC    H'28'             test number
00001656  00                                        906+          DC    X'00'
00001657  06                                        907+          DC    HL1'06'            i3
00001658  E5E2E3D9 D3404040                         908+          DC    CL8'VSTRL'        instruction name
00001660  00000010                                  909+          DC    A(16)             result length
00001664  00001670                                  910+          DC    A(RE28)           address of expected result
                                                    911+*
00001668                                            912+X28       DS    0F
00001668  E606 8E8C 103D                0000108C    913+          VSTRL V1,V1OUTPUT,06     test instruction
0000166E  07FB                                      914+          BR    R11               return
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001670                                            915+RE28     DS    0F           expected  16 or 32 byte result
00001670                                            916+         DROP  R5
00001670  90123456 78901DFF                         917          DC    XL16'9012345678901DFFFFFFFFFFFFFFFF'
00001678  FFFFFFFF FFFFFFFF
                                                    918
                                                    919          VSI   VSTRL,07
00001680                                            920+         DS    0FD
00001680                      00001680              921+         USING *,R5               base for test data and test routine
00001680  00001698                                  922+T29      DC    A(X29)             address of test routine
00001684  001D                                      923+         DC    H'29'              test number
00001686  00                                        924+         DC    X'00'
00001687  07                                        925+         DC    HL1'07'             i3
00001688  E5E2E3D9 D3404040                         926+         DC    CL8'VSTRL'         instruction name
00001690  00000010                                  927+         DC    A(16)              result length
00001694  000016A0                                  928+         DC    A(RE29)            address of expected result
                                                    929+*
00001698                                            930+X29      DS    0F
00001698  E607 8E8C 103D                0000108C    931+         VSTRL V1,V1OUTPUT,07     test instruction
0000169E  07FB                                      932+         BR    R11                return
000016A0                                            933+RE29     DS    0F           expected  16 or 32 byte result
000016A0                                            934+         DROP  R5
000016A0  78901234 5678901D                         935          DC    XL16'789012345678901DFFFFFFFFFFFFFFFF'
000016A8  FFFFFFFF FFFFFFFF
                                                    936
                                                    937          VSI   VSTRL,08
000016B0                                            938+         DS    0FD
000016B0                      000016B0              939+         USING *,R5               base for test data and test routine
000016B0  000016C8                                  940+T30      DC    A(X30)             address of test routine
000016B4  001E                                      941+         DC    H'30'              test number
000016B6  00                                        942+         DC    X'00'
000016B7  08                                        943+         DC    HL1'08'             i3
000016B8  E5E2E3D9 D3404040                         944+         DC    CL8'VSTRL'         instruction name
000016C0  00000010                                  945+         DC    A(16)              result length
000016C4  000016D0                                  946+         DC    A(RE30)            address of expected result
                                                    947+*
000016C8                                            948+X30      DS    0F
000016C8  E608 8E8C 103D                0000108C    949+         VSTRL V1,V1OUTPUT,08     test instruction
000016CE  07FB                                      950+         BR    R11                return
000016D0                                            951+RE30     DS    0F           expected  16 or 32 byte result
000016D0                                            952+         DROP  R5
000016D0  56789012 34567890                         953          DC    XL16'5678901234567890DFFFFFFFFFFFFFFF'
000016D8  1DFFFFFF FFFFFFFF
                                                    954
                                                    955          VSI   VSTRL,09
000016E0                                            956+         DS    0FD
000016E0                      000016E0              957+         USING *,R5               base for test data and test routine
000016E0  000016F8                                  958+T31      DC    A(X31)             address of test routine
000016E4  001F                                      959+         DC    H'31'              test number
000016E6  00                                        960+         DC    X'00'
000016E7  09                                        961+         DC    HL1'09'             i3
000016E8  E5E2E3D9 D3404040                         962+         DC    CL8'VSTRL'         instruction name
000016F0  00000010                                  963+         DC    A(16)              result length
000016F4  00001700                                  964+         DC    A(RE31)            address of expected result
                                                    965+*
000016F8                                            966+X31      DS    0F
000016F8  E609 8E8C 103D                0000108C    967+         VSTRL V1,V1OUTPUT,09     test instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000016FE  07FB                                968+         BR    R11               return
00001700                                      969+RE31     DS    0F           expected  16 or 32 byte result
00001700                                      970+         DROP  R5
00001700  34567890 12345678                   971          DC    XL16'3456789012345678901DFFFFFFFFFFFF'
00001708  901DFFFF FFFFFFFF
                                              972
                                              973          VSI   VSTRL,10
00001710                                      974+         DS    0FD
00001710                      00001710        975+         USING *,R5              base for test data and test routine
00001710  00001728                            976+T32      DC    A(X32)            address of test routine
00001714  0020                                977+         DC    H'32'             test number
00001716  00                                  978+         DC    X'00'
00001717  0A                                  979+         DC    HL1'10'            i3
00001718  E5E2E3D9 D3404040                   980+         DC    CL8'VSTRL'        instruction name
00001720  00000010                            981+         DC    A(16)             result length
00001724  00001730                            982+         DC    A(RE32)           address of expected result
                                              983+*
00001728                                      984+X32      DS    0F
00001728  E60A 8E8C 103D              0000108C 985+         VSTRL V1,V1OUTPUT,10     test instruction
0000172E  07FB                                986+         BR    R11               return
00001730                                      987+RE32     DS    0F           expected  16 or 32 byte result
00001730                                      988+         DROP  R5
00001730  12345678 90123456                   989          DC    XL16'1234567890123456789012345678901DFFFFFFFFFFF'
00001738  78901DFF FFFFFFFF
                                              990
                                              991          VSI   VSTRL,11
00001740                                      992+         DS    0FD
00001740                      00001740        993+         USING *,R5              base for test data and test routine
00001740  00001758                            994+T33      DC    A(X33)            address of test routine
00001744  0021                                995+         DC    H'33'             test number
00001746  00                                  996+         DC    X'00'
00001747  0B                                  997+         DC    HL1'11'            i3
00001748  E5E2E3D9 D3404040                   998+         DC    CL8'VSTRL'        instruction name
00001750  00000010                            999+         DC    A(16)             result length
00001754  00001760                           1000+         DC    A(RE33)           address of expected result
                                             1001+*
00001758                                     1002+X33      DS    0F
00001758  E60B 8E8C 103D              0000108C 1003+         VSTRL V1,V1OUTPUT,11     test instruction
0000175E  07FB                               1004+         BR    R11               return
00001760                                     1005+RE33     DS    0F           expected  16 or 32 byte result
00001760                                     1006+         DROP  R5
00001760  90123456 78901234                  1007          DC    XL16'9012345678901234567890DFFFFFFFF'
00001768  5678901D FFFFFFFF
                                             1008
                                             1009          VSI   VSTRL,12
00001770                                     1010+         DS    0FD
00001770                      00001770       1011+         USING *,R5              base for test data and test routine
00001770  00001788                           1012+T34      DC    A(X34)            address of test routine
00001774  0022                               1013+         DC    H'34'             test number
00001776  00                                 1014+         DC    X'00'
00001777  0C                                 1015+         DC    HL1'12'            i3
00001778  E5E2E3D9 D3404040                  1016+         DC    CL8'VSTRL'        instruction name
00001780  00000010                           1017+         DC    A(16)             result length
00001784  00001790                           1018+         DC    A(RE34)           address of expected result
                                             1019+*
00001788                                     1020+X34      DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001788  E60C 8E8C 103D                 0000108C  1021+          VSTRL V1,V1OUTPUT,12     test instruction
0000178E  07FB                                     1022+          BR    R11                return
00001790                                           1023+RE34      DS    0F           expected  16 or 32 byte result
00001790                                           1024+          DROP  R5
00001790  78901234 56789012                        1025           DC    XL16'789012345678901234567890 1DFFFFFF'
00001798  34567890 1DFFFFFF
                                                   1026
                                                   1027           VSI   VSTRL,13
000017A0                                           1028+          DS    0FD
000017A0                       000017A0            1029+          USING *,R5               base for test data and test routine
000017A0  000017B8                                 1030+T35       DC    A(X35)             address of test routine
000017A4  0023                                     1031+          DC    H'35'              test number
000017A6  00                                       1032+          DC    X'00'
000017A7  0D                                       1033+          DC    HL1'13'             i3
000017A8  E5E2E3D9 D3404040                        1034+          DC    CL8'VSTRL'         instruction name
000017B0  00000010                                 1035+          DC    A(16)              result length
000017B4  000017C0                                 1036+          DC    A(RE35)            address of expected result
                                                   1037+*
000017B8                                           1038+X35       DS    0F
000017B8  E60D 8E8C 103D                 0000108C  1039+          VSTRL V1,V1OUTPUT,13     test instruction
000017BE  07FB                                     1040+          BR    R11                return
000017C0                                           1041+RE35      DS    0F           expected  16 or 32 byte result
000017C0                                           1042+          DROP  R5
000017C0  56789012 34567890                        1043           DC    XL16'567890123456789012345678901DFFFF'
000017C8  12345678 901DFFFF
                                                   1044
                                                   1045           VSI   VSTRL,14
000017D0                                           1046+          DS    0FD
000017D0                       000017D0            1047+          USING *,R5               base for test data and test routine
000017D0  000017E8                                 1048+T36       DC    A(X36)             address of test routine
000017D4  0024                                     1049+          DC    H'36'              test number
000017D6  00                                       1050+          DC    X'00'
000017D7  0E                                       1051+          DC    HL1'14'             i3
000017D8  E5E2E3D9 D3404040                        1052+          DC    CL8'VSTRL'         instruction name
000017E0  00000010                                 1053+          DC    A(16)              result length
000017E4  000017F0                                 1054+          DC    A(RE36)            address of expected result
                                                   1055+*
000017E8                                           1056+X36       DS    0F
000017E8  E60E 8E8C 103D                 0000108C  1057+          VSTRL V1,V1OUTPUT,14     test instruction
000017EE  07FB                                     1058+          BR    R11                return
000017F0                                           1059+RE36      DS    0F           expected  16 or 32 byte result
000017F0                                           1060+          DROP  R5
000017F0  34567890 12345678                        1061           DC    XL16'345678901234567890123456789 01DFF'
000017F8  90123456 78901DFF
                                                   1062
                                                   1063           VSI   VSTRL,15
00001800                                           1064+          DS    0FD
00001800                       00001800            1065+          USING *,R5               base for test data and test routine
00001800  00001818                                 1066+T37       DC    A(X37)             address of test routine
00001804  0025                                     1067+          DC    H'37'              test number
00001806  00                                       1068+          DC    X'00'
00001807  0F                                       1069+          DC    HL1'15'             i3
00001808  E5E2E3D9 D3404040                        1070+          DC    CL8'VSTRL'         instruction name
00001810  00000010                                 1071+          DC    A(16)              result length
00001814  00001820                                 1072+          DC    A(RE37)            address of expected result
                                                   1073+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001818                                           1074+X37      DS    0F
00001818  E60F 8E8C 103D                 0000108C  1075+          VSTRL V1,V1OUTPUT,15     test instruction
0000181E  07FB                                     1076+          BR    R11                return
00001820                                           1077+RE37     DS    0F            expected  16 or 32 byte result
00001820                                           1078+          DROP  R5
00001820  12345678 90123456                        1079           DC    XL16'1234567890123456789012345678901D'
00001828  78901234 5678901D
                                                   1080
                                                   1081
00001830  00000000                                 1082           DC    F'0'     END OF TABLE
00001834  00000000                                 1083           DC    F'0'
                                                   1084 *
                                                   1085 * table of pointers to individual load test
                                                   1086 *
00001838                                           1087 E6TESTS  DS    0F
                                                   1088           PTTABLE
00001838                                           1089+TTABLE   DS    0F
00001838  000010F0                                 1090+          DC    A(T1)              TEST &CUR
0000183C  00001120                                 1091+          DC    A(T2)              TEST &CUR
00001840  00001150                                 1092+          DC    A(T3)              TEST &CUR
00001844  00001180                                 1093+          DC    A(T4)              TEST &CUR
00001848  000011B0                                 1094+          DC    A(T5)              TEST &CUR
0000184C  000011E0                                 1095+          DC    A(T6)              TEST &CUR
00001850  00001210                                 1096+          DC    A(T7)              TEST &CUR
00001854  00001240                                 1097+          DC    A(T8)              TEST &CUR
00001858  00001270                                 1098+          DC    A(T9)              TEST &CUR
0000185C  000012A0                                 1099+          DC    A(T10)             TEST &CUR
00001860  000012D0                                 1100+          DC    A(T11)             TEST &CUR
00001864  00001300                                 1101+          DC    A(T12)             TEST &CUR
00001868  00001330                                 1102+          DC    A(T13)             TEST &CUR
0000186C  00001360                                 1103+          DC    A(T14)             TEST &CUR
00001870  00001390                                 1104+          DC    A(T15)             TEST &CUR
00001874  000013C0                                 1105+          DC    A(T16)             TEST &CUR
00001878  000013F0                                 1106+          DC    A(T17)             TEST &CUR
0000187C  00001430                                 1107+          DC    A(T18)             TEST &CUR
00001880  00001470                                 1108+          DC    A(T19)             TEST &CUR
00001884  000014B0                                 1109+          DC    A(T20)             TEST &CUR
00001888  000014F0                                 1110+          DC    A(T21)             TEST &CUR
0000188C  00001530                                 1111+          DC    A(T22)             TEST &CUR
00001890  00001560                                 1112+          DC    A(T23)             TEST &CUR
00001894  00001590                                 1113+          DC    A(T24)             TEST &CUR
00001898  000015C0                                 1114+          DC    A(T25)             TEST &CUR
0000189C  000015F0                                 1115+          DC    A(T26)             TEST &CUR
000018A0  00001620                                 1116+          DC    A(T27)             TEST &CUR
000018A4  00001650                                 1117+          DC    A(T28)             TEST &CUR
000018A8  00001680                                 1118+          DC    A(T29)             TEST &CUR
000018AC  000016B0                                 1119+          DC    A(T30)             TEST &CUR
000018B0  000016E0                                 1120+          DC    A(T31)             TEST &CUR
000018B4  00001710                                 1121+          DC    A(T32)             TEST &CUR
000018B8  00001740                                 1122+          DC    A(T33)             TEST &CUR
000018BC  00001770                                 1123+          DC    A(T34)             TEST &CUR
000018C0  000017A0                                 1124+          DC    A(T35)             TEST &CUR
000018C4  000017D0                                 1125+          DC    A(T36)             TEST &CUR
000018C8  00001800                                 1126+          DC    A(T37)             TEST &CUR
                                                   1127+*
000018CC  00000000                                 1128+          DC    A(0)               END OF TABLE
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000018D0  00000000                          1129+         DC    A(0)
                                            1130
000018D4  00000000                          1131          DC    F'0'     END OF TABLE
000018D8  00000000                          1132          DC    F'0'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1134 ********************************************************************************
                                                    1135 *        Register equates
                                                    1136 ********************************************************************************

                                00000000  00000001  1138 R0       EQU   0
                                00000001  00000001  1139 R1       EQU   1
                                00000002  00000001  1140 R2       EQU   2
                                00000003  00000001  1141 R3       EQU   3
                                00000004  00000001  1142 R4       EQU   4
                                00000005  00000001  1143 R5       EQU   5
                                00000006  00000001  1144 R6       EQU   6
                                00000007  00000001  1145 R7       EQU   7
                                00000008  00000001  1146 R8       EQU   8
                                00000009  00000001  1147 R9       EQU   9
                                0000000A  00000001  1148 R10      EQU   10
                                0000000B  00000001  1149 R11      EQU   11
                                0000000C  00000001  1150 R12      EQU   12
                                0000000D  00000001  1151 R13      EQU   13
                                0000000E  00000001  1152 R14      EQU   14
                                0000000F  00000001  1153 R15      EQU   15


                                                    1155 ********************************************************************************
                                                    1156 *        Register equates
                                                    1157 ********************************************************************************


                              00000000  00000001  1159 V0       EQU   0
                              00000001  00000001  1160 V1       EQU   1
                              00000002  00000001  1161 V2       EQU   2
                              00000003  00000001  1162 V3       EQU   3
                              00000004  00000001  1163 V4       EQU   4
                              00000005  00000001  1164 V5       EQU   5
                              00000006  00000001  1165 V6       EQU   6
                              00000007  00000001  1166 V7       EQU   7
                              00000008  00000001  1167 V8       EQU   8
                              00000009  00000001  1168 V9       EQU   9
                              0000000A  00000001  1169 V10      EQU   10
                              0000000B  00000001  1170 V11      EQU   11
                              0000000C  00000001  1171 V12      EQU   12
                              0000000D  00000001  1172 V13      EQU   13
                              0000000E  00000001  1173 V14      EQU   14
                              0000000F  00000001  1174 V15      EQU   15
                              00000010  00000001  1175 V16      EQU   16
                              00000011  00000001  1176 V17      EQU   17
                              00000012  00000001  1177 V18      EQU   18
                              00000013  00000001  1178 V19      EQU   19
                              00000014  00000001  1179 V20      EQU   20
                              00000015  00000001  1180 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                00000016  00000001  1181 V22       EQU   22
                                00000017  00000001  1182 V23       EQU   23
                                00000018  00000001  1183 V24       EQU   24
                                00000019  00000001  1184 V25       EQU   25
                                0000001A  00000001  1185 V26       EQU   26
                                0000001B  00000001  1186 V27       EQU   27
                                0000001C  00000001  1187 V28       EQU   28
                                0000001D  00000001  1188 V29       EQU   29
                                0000001E  00000001  1189 V30       EQU   30
                                0000001F  00000001  1190 V31       EQU   31
                                                    1191
                                                    1192           END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	00000200	2	93	60 90 91
CTLR0	F	000003EC	4	243	100 101 102 103
DECNUM	C	0000106E	16	287	160 162 169 171
E6TEST	4	00000000	24	305	113
E6TESTS	F	00001838	4	1087	106
EDIT	X	00001042	18	282	161 170
ENDTEST	U	0000027C	1	145	111
EOJ	I	000003D0	4	233	148
EOJPSW	D	000003C0	8	231	233
EXCLC	I	00000262	6	131	124
FAILED	F	00001000	4	269	140 146
FAILMSG	U	00000268	1	137	126
FAILPSW	D	000003D8	8	235	237
FAILTEST	I	000003E8	4	237	149
I3	U	00000007	1	309	168
IMAGE	1	00000000	6364	0	
K	U	00000400	1	253	254 255 256
K64	U	00010000	1	255	
MB	U	00100000	1	256	
MSG	I	00000308	4	197	180
MSGCMD	C	00000352	9	223	210 211
MSGMSG	C	0000035B	95	224	204 221 202
MSGMVC	I	0000034C	6	221	208
MSGOK	I	0000031E	2	206	203
MSGRET	I	00000338	4	217	214
MSGSAVE	F	00000340	4	220	200 217
NEXTE6	U	00000222	1	108	129 143
OPNAME	C	00000008	8	311	165
PAGE	U	00001000	1	254	
PRT3	C	00001058	18	285	161 162 163 170 171 172
PRTI3	C	00001040	1	279	172
PRTLINE	C	00001004	16	274	281 179
PRTLNG	U	0000003E	1	281	178
PRTNAME	C	0000102F	8	277	165
PRTNUM	C	00001014	3	275	163
R0	U	00000000	1	1138	54 100 103 139 140 177 178 181 197 200 202 204 206 217
R1	U	00000001	1	1139	121 131 146 147 179 211 221
R10	U	0000000A	1	1148	106 109 128 142
R11	U	0000000B	1	1149	118 119 415 433 451 469 487 505 523 541 559 577 595 613 631 649 667 685 703 722 741 762 781 806 824 842 860 878 896 914 932 950 968 986 1004 1022 1040 1058 1076
R12	U	0000000C	1	1150	
R13	U	0000000D	1	1151	
R14	U	0000000E	1	1152	
R15	U	0000000F	1	1153	138 156 184 185
R2	U	00000002	1	1140	122 123 124 159 160 167 168 169 177 180 181 198 200 206 207 208 210 217 218
R3	U	00000003	1	1141	
R4	U	00000004	1	1142	
R5	U	00000005	1	1143	109 110 113 157 183 404 417 422 435 440 453 458 471 476 489 494 507 512 525 530 543 548 561 566 579 584 597 602 615 620 633 638 651 656 669 674 687 692 705 711 724 730 743 751 764 770 783 795 808 813 826 831 844 849 862 867 880 885 898 903 916 921 934 939 952 957 970 975 988 993 1006 1011 1024 1029 1042 1047 1060 1065

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
					1078					
R6	U	00000006	1	1144						
R7	U	00000007	1	1145						
R8	U	00000008	1	1146	90	93	94	95	97	
R9	U	00000009	1	1147	91	97	98			
RE1	F	00001110	4	416	411					
RE10	F	000012C0	4	578	573					
RE11	F	000012F0	4	596	591					
RE12	F	00001320	4	614	609					
RE13	F	00001350	4	632	627					
RE14	F	00001380	4	650	645					
RE15	F	000013B0	4	668	663					
RE16	F	000013E0	4	686	681					
RE17	F	00001410	4	704	699					
RE18	F	00001450	4	723	718					
RE19	F	00001490	4	742	737					
RE2	F	00001140	4	434	429					
RE20	F	000014D0	4	763	758					
RE21	F	00001510	4	782	777					
RE22	F	00001550	4	807	802					
RE23	F	00001580	4	825	820					
RE24	F	000015B0	4	843	838					
RE25	F	000015E0	4	861	856					
RE26	F	00001610	4	879	874					
RE27	F	00001640	4	897	892					
RE28	F	00001670	4	915	910					
RE29	F	000016A0	4	933	928					
RE3	F	00001170	4	452	447					
RE30	F	000016D0	4	951	946					
RE31	F	00001700	4	969	964					
RE32	F	00001730	4	987	982					
RE33	F	00001760	4	1005	1000					
RE34	F	00001790	4	1023	1018					
RE35	F	000017C0	4	1041	1036					
RE36	F	000017F0	4	1059	1054					
RE37	F	00001820	4	1077	1072					
RE4	F	000011A0	4	470	465					
RE5	F	000011D0	4	488	483					
RE6	F	00001200	4	506	501					
RE7	F	00001230	4	524	519					
RE8	F	00001260	4	542	537					
RE9	F	00001290	4	560	555					
REG2LOW	U	000000DD	1	259						
REG2PATT	U	AABBCCDD	1	258						
RELEN	A	00000010	4	312	122					
RESULT	A	00000014	4	313	121					
RPTDWSAV	D	000002F8	8	190	177	181				
RPTERROR	I	0000028A	4	156	138					
RPTSAVE	F	000002F0	4	187	156	184				
RPTSVR5	F	000002F4	4	188	157	183				
SVOLDPSW	U	00000140	0	56						
T1	A	000010F0	4	405	1090					
T10	A	000012A0	4	567	1099					
T11	A	000012D0	4	585	1100					
T12	A	00001300	4	603	1101					
T13	A	00001330	4	621	1102					

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T14	A	00001360	4	639	1103
T15	A	00001390	4	657	1104
T16	A	000013C0	4	675	1105
T17	A	000013F0	4	693	1106
T18	A	00001430	4	712	1107
T19	A	00001470	4	731	1108
T2	A	00001120	4	423	1091
T20	A	000014B0	4	752	1109
T21	A	000014F0	4	771	1110
T22	A	00001530	4	796	1111
T23	A	00001560	4	814	1112
T24	A	00001590	4	832	1113
T25	A	000015C0	4	850	1114
T26	A	000015F0	4	868	1115
T27	A	00001620	4	886	1116
T28	A	00001650	4	904	1117
T29	A	00001680	4	922	1118
T3	A	00001150	4	441	1092
T30	A	000016B0	4	940	1119
T31	A	000016E0	4	958	1120
T32	A	00001710	4	976	1121
T33	A	00001740	4	994	1122
T34	A	00001770	4	1012	1123
T35	A	000017A0	4	1030	1124
T36	A	000017D0	4	1048	1125
T37	A	00001800	4	1066	1126
T4	A	00001180	4	459	1093
T5	A	000011B0	4	477	1094
T6	A	000011E0	4	495	1095
T7	A	00001210	4	513	1096
T8	A	00001240	4	531	1097
T9	A	00001270	4	549	1098
TNUM	H	00000004	2	307	159
TSUB	A	00000000	4	306	118
TTABLE	F	00001838	4	1089	
V0	U	00000000	1	1159	
V1	U	00000001	1	1160	117 414 432 450 468 486 504 522 540 558 576 594 612 630 648 666 684 702 721 740 761 780 805 823 841 859 877 895 913 931 949 967 985 1003 1021 1039 1057 1075
V10	U	0000000A	1	1169	
V11	U	0000000B	1	1170	
V12	U	0000000C	1	1171	
V13	U	0000000D	1	1172	
V14	U	0000000E	1	1173	
V15	U	0000000F	1	1174	
V16	U	00000010	1	1175	
V17	U	00000011	1	1176	
V18	U	00000012	1	1177	
V19	U	00000013	1	1178	
V1FUDGE	X	000010BC	16	297	114 115
V1INPUT	X	000010CC	16	298	117
V1OUTPUT	X	0000108C	16	294	114 115 131 414 432 450 468 486 504 522 540 558 576 594 612 630 648 666 684 702 721 740 761 780 805 823 841 859 877 895 913 931 949 967 985 1003 1021 1039 1057 1075
V2	U	00000002	1	1161	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V20	U	00000014	1	1179	
V21	U	00000015	1	1180	
V22	U	00000016	1	1181	
V23	U	00000017	1	1182	
V24	U	00000018	1	1183	
V25	U	00000019	1	1184	
V26	U	0000001A	1	1185	
V27	U	0000001B	1	1186	
V28	U	0000001C	1	1187	
V29	U	0000001D	1	1188	
V3	U	00000003	1	1162	
V30	U	0000001E	1	1189	
V31	U	0000001F	1	1190	
V4	U	00000004	1	1163	
V5	U	00000005	1	1164	
V6	U	00000006	1	1165	
V7	U	00000007	1	1166	
V8	U	00000008	1	1167	
V9	U	00000009	1	1168	
X1	F	00001108	4	413	405
X10	F	000012B8	4	575	567
X11	F	000012E8	4	593	585
X12	F	00001318	4	611	603
X13	F	00001348	4	629	621
X14	F	00001378	4	647	639
X15	F	000013A8	4	665	657
X16	F	000013D8	4	683	675
X17	F	00001408	4	701	693
X18	F	00001448	4	720	712
X19	F	00001488	4	739	731
X2	F	00001138	4	431	423
X20	F	000014C8	4	760	752
X21	F	00001508	4	779	771
X22	F	00001548	4	804	796
X23	F	00001578	4	822	814
X24	F	000015A8	4	840	832
X25	F	000015D8	4	858	850
X26	F	00001608	4	876	868
X27	F	00001638	4	894	886
X28	F	00001668	4	912	904
X29	F	00001698	4	930	922
X3	F	00001168	4	449	441
X30	F	000016C8	4	948	940
X31	F	000016F8	4	966	958
X32	F	00001728	4	984	976
X33	F	00001758	4	1002	994
X34	F	00001788	4	1020	1012
X35	F	000017B8	4	1038	1030
X36	F	000017E8	4	1056	1048
X37	F	00001818	4	1074	1066
X4	F	00001198	4	467	459
X5	F	000011C8	4	485	477
X6	F	000011F8	4	503	495
X7	F	00001228	4	521	513
X8	F	00001258	4	539	531
X9	F	00001288	4	557	549

```
     SYMBOL          TYPE    VALUE       LENGTH    DEFN   REFERENCES

ZVE6TST               J     00000000        6364      53     56     58     62     66    268     54
=AL2(L'MSGMSG)        R     000003FA           2     249    202
=F'1'                 F     000003F4           4     247    139
=H'0'                 H     000003F8           2     248    197
```

```
 MACRO    DEFN   REFERENCES

PTTABLE    369    1088
VSI        329     402     420     438     456     474     492     510     528     546     564     582     600     618     636     654     672     690
                   709     728     749     768     793     811     829     847     865     883     901     919     937     955     973     991    1009
                  1027    1045    1063
```

```
   DESC      SYMBOL   SIZE     POS         ADDR

Entry: 0

Image       IMAGE    6364  0000-18DB  0000-18DB
  Region             6364  0000-18DB  0000-18DB
    CSECT   ZVE6TST  6364  0000-18DB  0000-18DB
```

```
   STMT                    FILE NAME
1     /devstor/dev/tests/zvector-e6-04-unpack.asm

** NO ERRORS FOUND **
```