


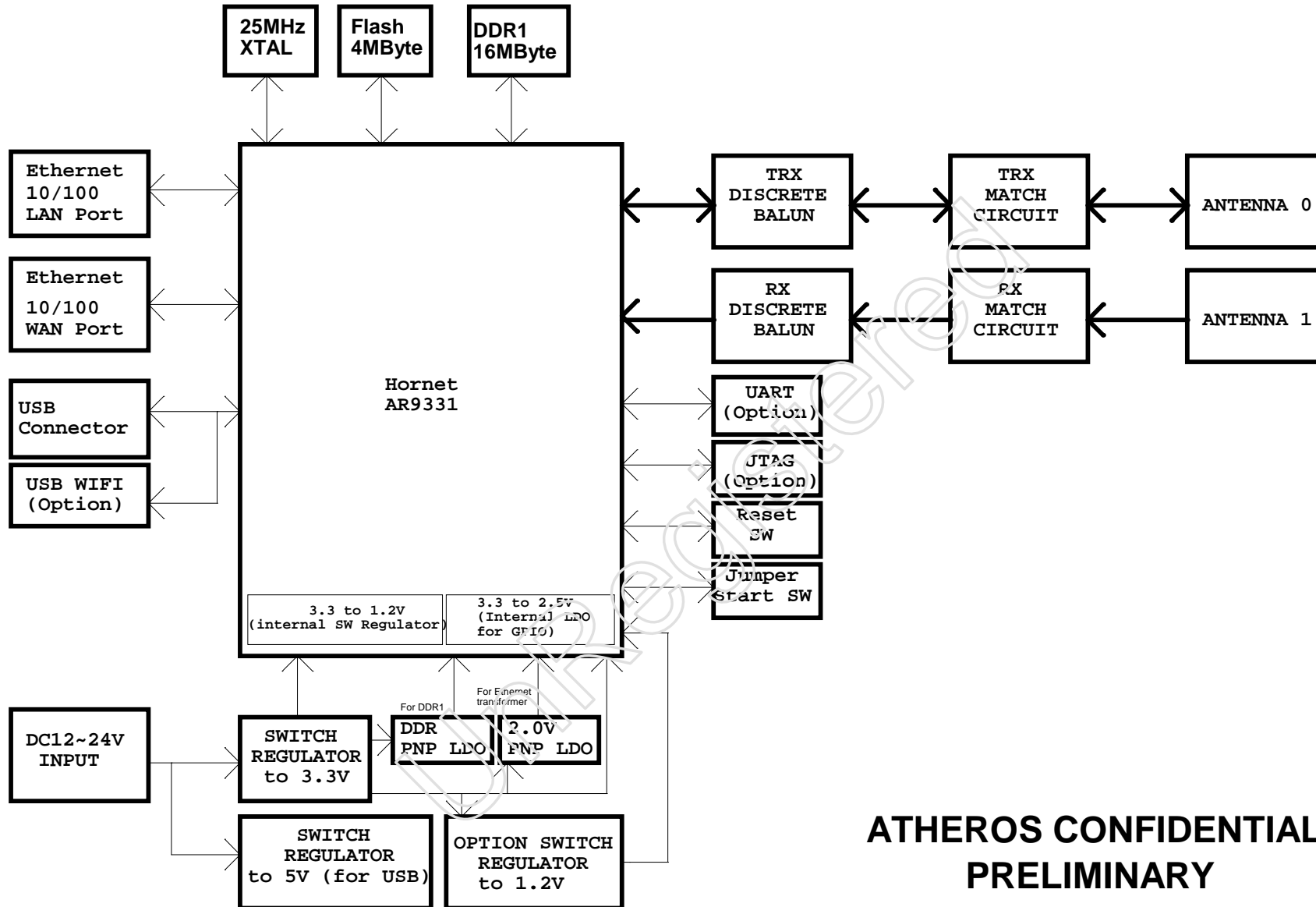
DATE	REVISION NUMBER	INITIALS	DESCRIPTION
March, 24, 2010	245-01951-010	JC	AP121-010
June, 24, 2010	245-01951-020	JC	<p>1.Delete DC1.2V option.</p> <p>2.Delete R3, R210, R206, C158, C159, C165, C166, R207, R11, R209, C35</p> <p>3.Change C3 from 27pF to 10pF, change C4 from 33pF to 10pF, change C66 C67 from 1.5pF to 10pF, change C65 from 1.2pF to 1pF, change C68 C69 C70 C71 from 1.2pF to 2pF, change L1 L2 from 3nH to 2nH, change L18 L20 from 1.5nH to 2.0nH, change C97 from 2pF to 1pF, change C177 from No Load to 0.75pF, change C89 C90 from 4.7pF to 10pF, change L5 L6 from 2.2nH to 2.0nH, change C91 C92 from 1.5pF to 1.2pF, change C93 from No Load to 1pF, change L14 from 4.7uH to 15uH, change L22 from 4.7uH to 10uH, change C157 C143 from 390pF to 3.9nF, change R201 from No Load to 6.81K, change R166 from 16.2K to 26.1K, change R168 from 5.1K to 10K, change C144 from 10pF to 10nF, change R149 from 5.1K to 10K, change C167 from 33pF to No Load, change C27 from 0.01uF to 0.1uF, change R9 from 10K to No Load, change R12 from 100K to No Load, change C55 from 1uF to 22uF, change C152 from 10uF to 22uF, change C72 from No Load to 1pF, change C30 from 4.7uF to 10uF, change R5 from 56K to 10K</p> <p>4.Add C203 2pF, R201 12K, C168 No Load, R215 56K, 1.2V option</p>
June, 28, 2010	245-01951-030	JC	<p>1.Add 1.2V option</p> <p>2.Change C14 C15 C19 C20 from 0.01uF to No Load, change C54 C21 from 0.01uF to 1uF, change C32 from 0.01uF to 470pF, change R12 from No Load to 1uF, change C65 from 1.2pF to 0.75pF, change C203 from 2pF to 1.5pF, change C72 from 1pF to No Load, change C177 from 0.75pF to 0.5pF, change C91 C92 from 1.2pF to 1pF,</p>
August, 2, 2010	245-01951-031	JC	<p>1.Change R4 R64 R65 R189 R194 R196 R198 R214 from 56K to 10K, change R188 from 56K to No Load, change R187 from No Load to 10K, change R12 from 1uF to 0.22uF, change R215 from 56K to No Load, change C68 C69 from 2.0pF to 1.8pF, change C65 from 0.75pF to 0.5pF, change L17 L19 from 4.7nH to 3.6nH, change C97 from 1pF to 1.5pF, change L5 L6 from 2.0nH to 2.2nH</p> <p>2.Remove C93 C117</p>
August, 30, 2010	245-01951-040	JC	<p>1.Add L21, C204</p> <p>2.Remove C34</p> <p>3.Change R92 from 330 ohm to 270 ohm, change C187 from 10K to No Load, change C188 from No Load to 10K, change C74 from 10pF to 0.75pF, change C75 from No Load to 6.8nH, change C94 from No Load to 0.5pF, change C95 from 10pF to 2.7nH</p>
October, 1, 2010	245-01951-041	JC	1.Change C65 from 0.5pF to No Load, C68 C69 from 1.8pF to 1pF, C70 C71 from 2pF to 1pF, C72 from No Load to 1pF, C97 from 1.5pF to 1.2pF, C26 from 0.01uF to No Load, L1 L2 from 2nH to 2.2nH, L17 L19 from 3.9nH to 4.7nH, L5 L6 from 2.2nH to 2.7nH
October, 15, 2010	245-01951-050	JC	1.Add R202 10K, R203 No Load, change C97 from 1.2pF to 1.5pF, change L11 from 10nH to 8ohm, change C204 from 0.1uF to 1nF, change C26 from No Load to 0.01uF, change R5 from 10F to No Load, change R215 from No Load to 10K, change JP1 to No Load, change J2 to No Load
February, 14, 2011	245-01951-060	JC	<p>1.Del L21, TP8, TP10, TP11, TP12, TP13, C176, C177, C20</p> <p>2.Change C54 from 1uF/0402 to 10pF/0201, change C97 from 1.5pF to 1.2pF, change C144 C129 from 0.01uF to 0.1uF, change C143 C157 from 3900pF to 3300pF, change R201 from 6.18K to 12K, change R210 from 12K to 20K, change R166 from 26.1K to 71.5K, change R168 from 10K to 22K, L17 L19 from 4.7uH to 3.9nH, change R148 from 45.3K to 62K, change R149 from 10K to 11.8K, change L15 L16 from 10nH to 4.7nH, change C68 C69 C70 C71 C91 C92 from 1pF to 1.2pF, change C89 C90 from 10pF to 3.9pF, change C31 from 1uF to 1nF, change C93 from No Load to 0.75pF, change C204 from 1nF to 1uF, change L18 L20 from 2.0nH to 1.8nH, change C181 C182 from 10pF to 0.1uF</p> <p>3.Add C31, C34, C35, L21, L23</p>
April, 14, 2011	245-01951-061	JC	1. update UI symbol
May, 9, 2011	245-01951-062	JC	1. update no USB support

# AP121 802.11b/g/n 1x1 2.4GHz Access Point AR9331 4LAN + 1WAN 10/100 Router Reference Design

ATHEROS CONFIDENTIAL  
PRELIMINARY



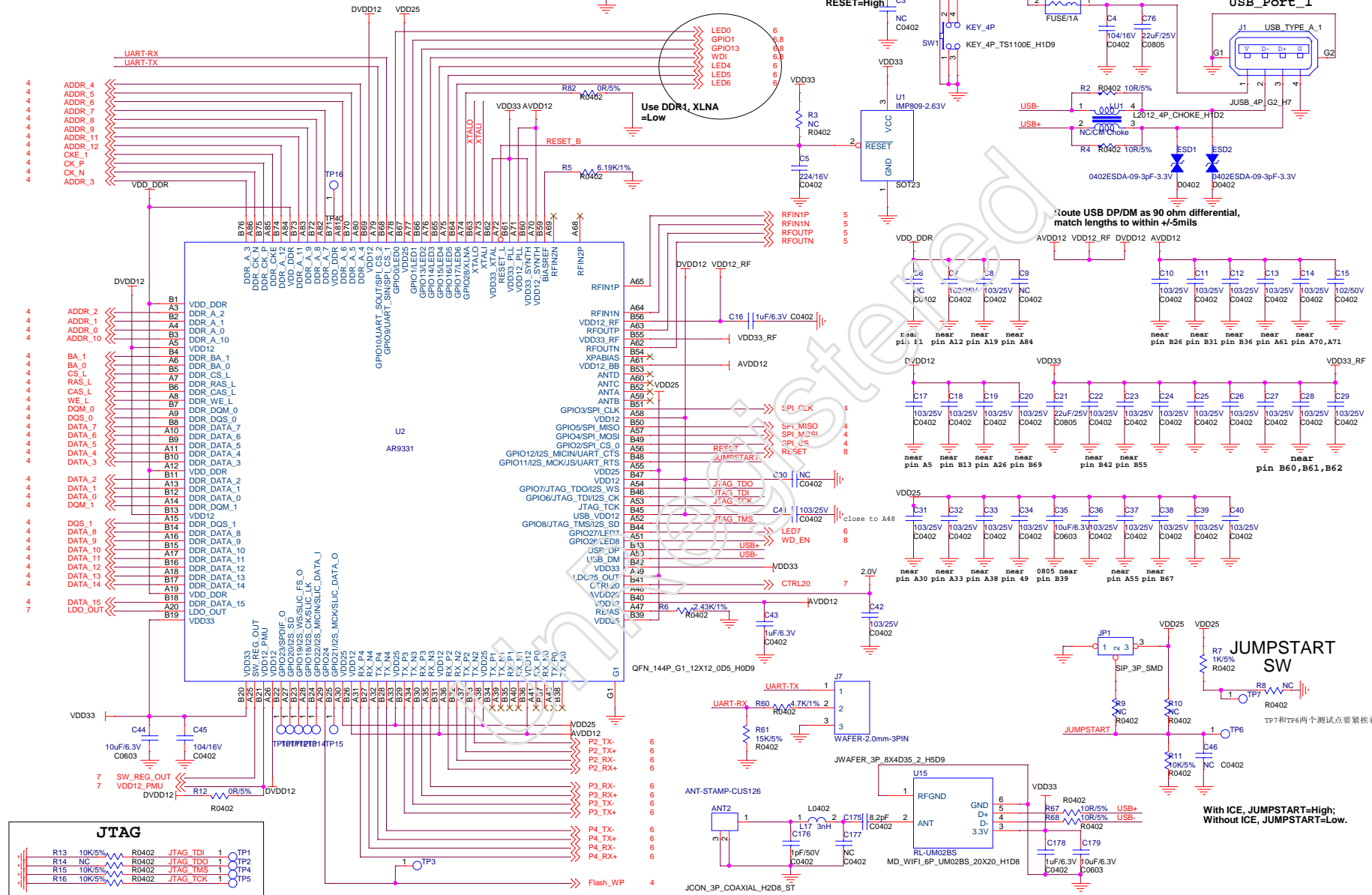
 <b>Atheros Communications, Inc.</b> 5480 Great America Parkway Santa Clara, CA 95054		<b>Title and Revision History</b>			
Date Thursday, August 02, 2012	Size C	Rev 000	Sheet 1 of 8	DWG NO	AP121-245-01951-062



**ATHEROS CONFIDENTIAL  
PRELIMINARY**

Note: Pin name is 0.99 (20100316)

CK\_P, DQS\_0, DQS1 short together if use SDRAM.



Note: Hornet Digital IO pads(Flash, UART,JTAG, LED) are 2.5V CMOS logic, don't apply >2.9V on it otherwise might damage the IC.

Memory bus clock speed and voltage:  
 SDRAM: 166MHz, 3.0V  
 DDR1:200MHz, 2.5V  
 DDR2:200MHz, 1.8V

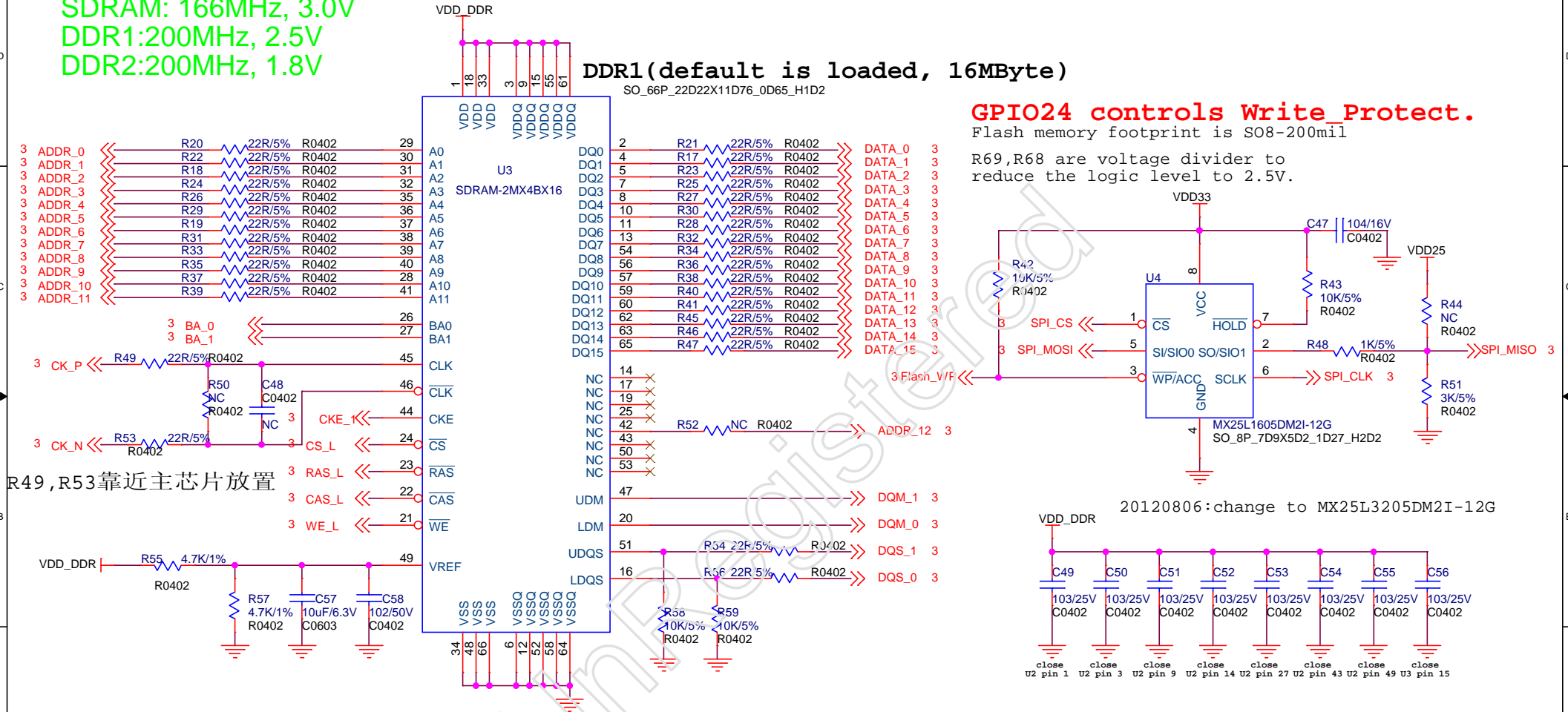
DDR1(default is loaded, 16MByte)

SO\_66P\_22D22X11D76\_0D65\_H1D2

**GPI024 controls Write Protect.**

Flash memory footprint is SO8-200mil

R69,R68 are voltage divider to  
 reduce the logic level to 2.5V.



R49,R53靠近主芯片放置

20120806:change to MX25L3205DM2I-12G



**Atheros Communications, Inc.**

5480 Great America Parkway  
 Santa Clara, CA 95054

Title

**AP121 Memory**

Date Monday, August 06, 2012

Size Custom

Rev 000

Sheet

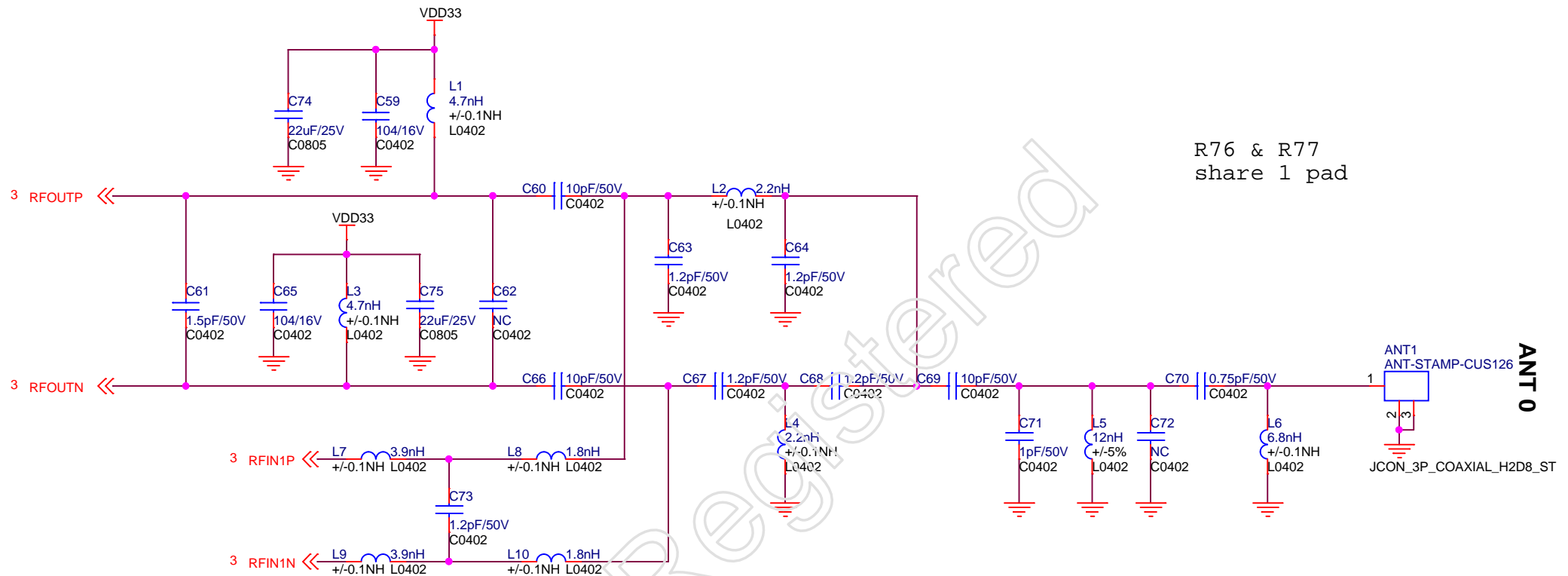
4

of

8

DWG NO

L15, L16 recommend using low DCR  
 Psat power current 150mA~180mA



**Atheros Communications, Inc.**

5480 Great America Parkway  
 Santa Clara, CA 95054

Title

**AP121 RF**

Date Thursday, August 02, 2012

Size Custom

Rev 000

Sheet

**5**

of

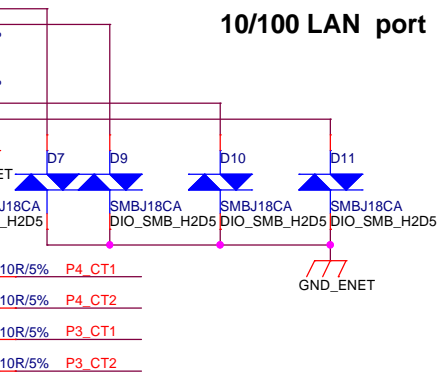
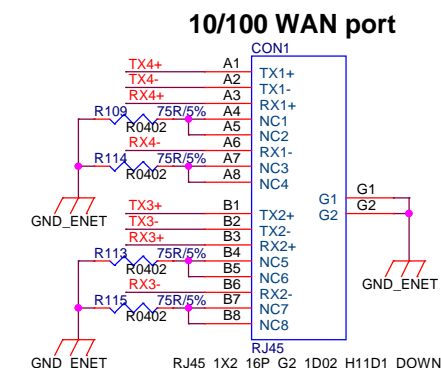
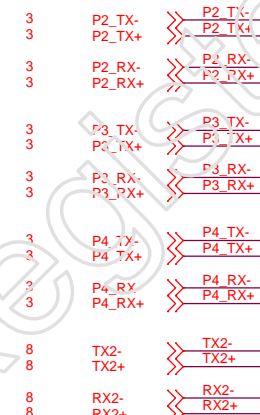
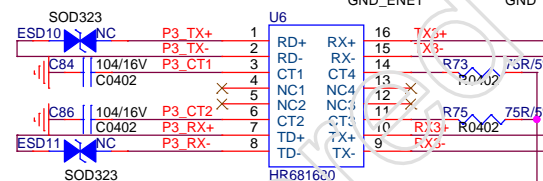
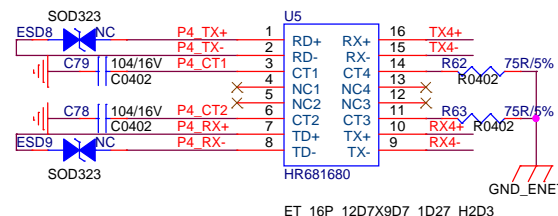
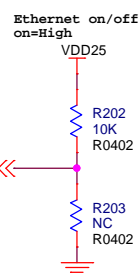
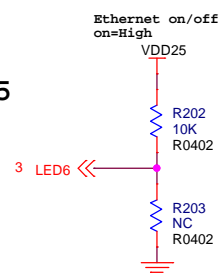
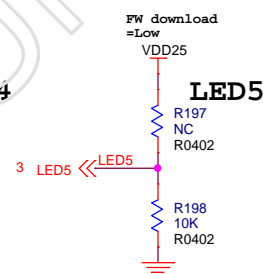
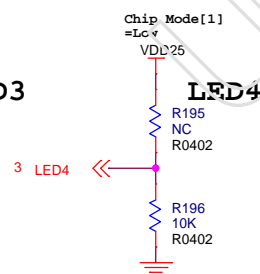
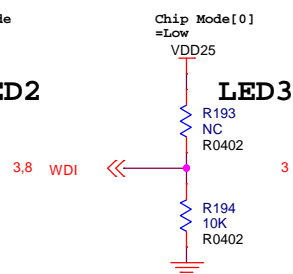
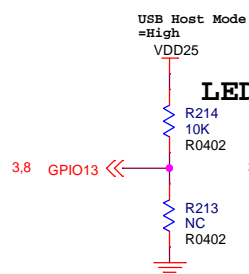
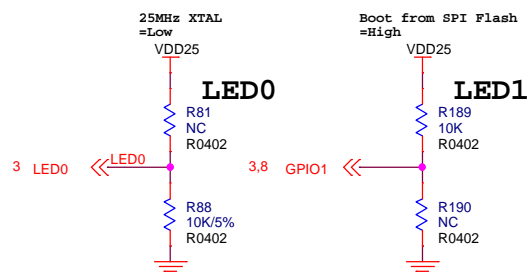
**8**

DWG NO

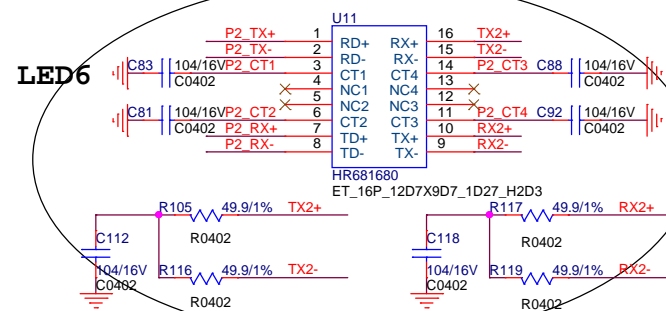
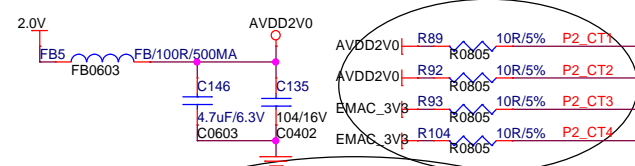
Nets name LED0, LED1, LED2, LED3, LED4, LED6 are also for Boot-strap during power on.  
To avoid wrong voltage applied on the IO pin from LED, these GPIOs should be source current only.  
The rest LEDs are using sink current mode to reduce the Hornet internal 2.5V LDO loading (thermal).

The diagram shows four LEDs connected to a microcontroller. Each LED is connected to a microcontroller pin (LED0, LED5, LED7, LED7) through a resistor (R65, R69, R72, R76) and a current-limiting resistor (R0402). The LEDs are connected to VDD3.3 and GND.

- WIRELESS\_LED1:** Connected to LED0 (R65, 270R/5%) and LED2 (LED\_2P\_4D2\_2D54).
- PORT4\_LED:** Connected to LED5 (R69, 270R/5%) and LED2 (LED\_2P\_4D2\_2D54).
- SYS:** Connected to LED7 (R72, 330R/5%) and LED3 (LED\_2P\_4D2\_2D54).
- Power\_LED:** Connected to LED7 (R76, 330R/5%) and LED4 (LED\_2P\_4D2\_2D54).



All WAN and LAN ports support Auto-MDIX.



**Atheros Communications, Inc.**  
5480 Great America Parkway  
Santa Clara, CA 95054

## AP121 Ethernet Interface

DWG NO
--------





