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5.04

The fetch-execute cycle(the fetch, decode and execute cycle):

Fetching:

1) put the location of the next instruction into the 'address' of the program memory
2) get the instruction code itself by reading the memory contents at that location

Executing: (the instruction code specifies about 'what to do')

1) different subsets of the bits control different aspects of operation
2) executing the operation involves also accessing registers and(/or) data memory.

Step:

1)An instruction is fetched from memory into the CPU
2)The instruction is decoded
3)The instruction is executed

5.05

Register transfer notation:

Def: A coded representation of data transfer and manipulation through the stages of the fetch-decode-execute cycle

form: Destination ← [source]
Destination: a register
source: the source contents(arithmetic can be associated with the source contents)

5.06

Interrupt handling

To identifying the type of interrupt:

1) interrupt register in the CPU--i) only detected at the end of a fetch-execute cycle
ii) allows the current program to be interrupted and left in a defined state which can be returned to later
2) interrupt service routine (ISR)-- i) immediate check to see if further interrupts need handling
ii) safely stored contents of the registers are restored to the CPU and the originally running program is resumed.