H3C CRPS PSU In-System Firmware Upload

1 In-System Firmware Upload

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the primary or secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is allowed that all the new FW will not take effect until PSU output restart.

1.1 FW Image Mapping

The power supply firmware image shall be made up of two parts; 1)Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1. Boot Loader: This is the part of the power supply firmware that is never updated by the system.
2. Main Program: This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

1.2 Summary of Commands & Capabilities supported in Boot Loader mode

When the power supply is in FW Upload mode the following commands shall be supported.

Code	Command	SMBus Transaction Type
19h	CAPABILITY	Read Byte with PEC
1Ah	QUERY (used with any command)	Block Write Block Read Process Call with PEC
98h	PMBUS_REVISION	Read Byte with PEC
99h	MFR_ID	Block Read
9Ah	MFR_MODEL	Block Read
D4h	MFR_HW_COMPATIBILITY	Read Word with PEC
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte with PEC
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte with PEC
D7h	MFR_FWUPLOAD	Bloack Write with PEC
D8h	MFR_FWUPLOAD_STATUS	Read Word with PEC
D9h	MFR_FW_REVISION	Block Read with PEC (3 bytes)

1.3 LED Status

While the PSU FW image is being updated the PSU shall blink the Green LED at a 2Hz rate.

1.4 Firmware Image Header

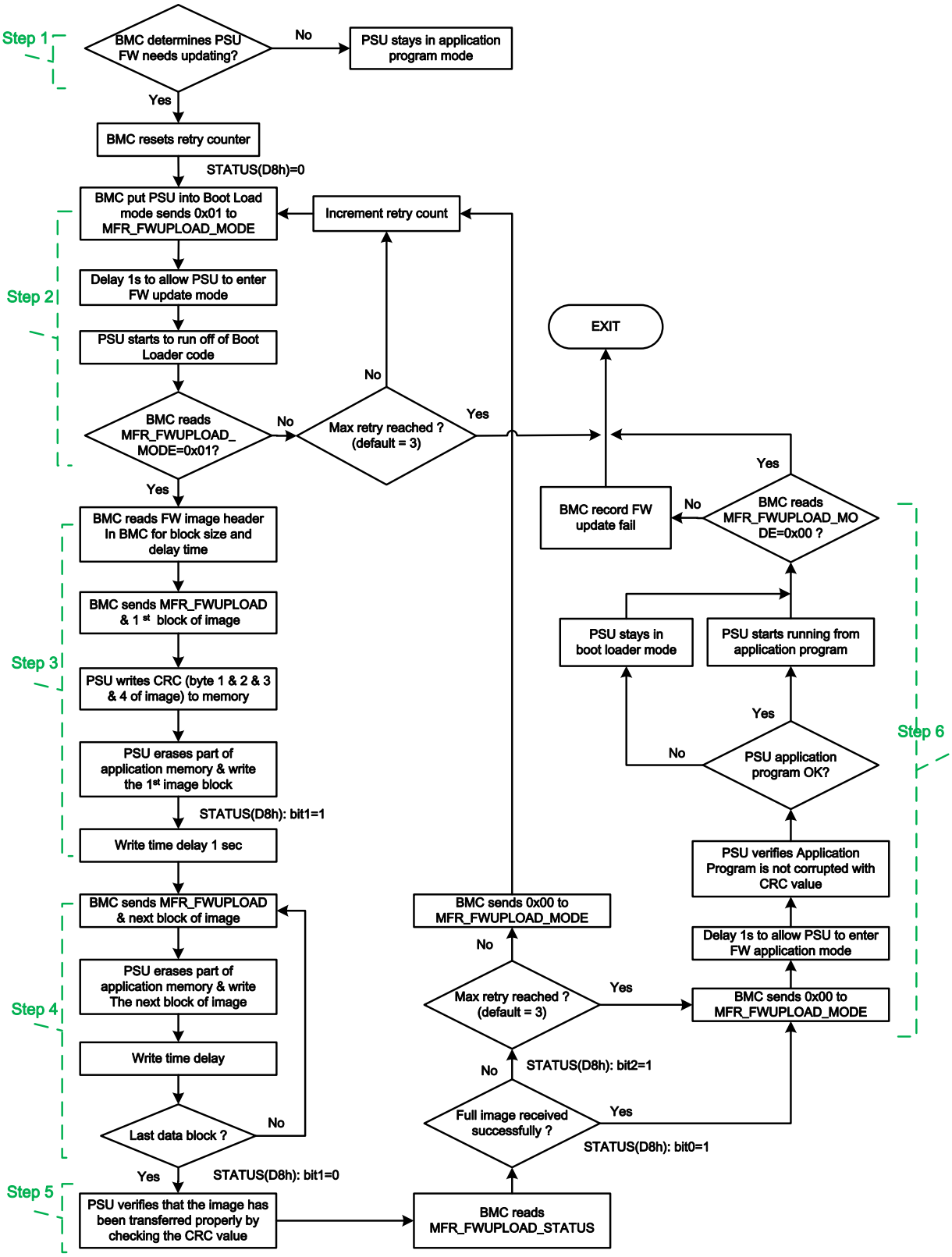
ADDR	Content	comments
BYTE 1	CRC LowByte_primary	升级初级代码校验码
BYTE 2	CRC HighByte_primary	
BYTE 3	CRC LowByte_secondary	升级次级代码校验码
BYTE 4	CRC HighByte_secondary	
BYTE 5	Set Upload MCU (Primary or secondary)	设定升级软件位置 0x01：Primary 0x02：Secondary 0x03：Primary+Secondary
BYTE 6	Image Information	Reserved for PSU supplier use
BYTE 7	Image Information	
BYTE 8	Image Information	
BYTE 9	P	PSU model name 区域 从 BYTE9 开始，未使用完的字节填写“0x00”空字符 null（ASCII 码）
BYTE 10	S	
BYTE 11	R	
BYTE 12	2	
BYTE 13	0	
BYTE 14	0	
BYTE 15	0	
BYTE 16	-	
BYTE 17	1	
BYTE 18	2	
BYTE 19	A	
BYTE 20	-	
BYTE 21	B	
BYTE 22		
BYTE 23		
BYTE 24	FW_MAJOR	0x00
BYTE 25	FW_MINOR_PRIMARY	
BYTE 26	FW_MINOR_SECONDARY	
BYTE 27	HW_COMPATIBILITY_FIRST	举例:PSU HW rev 为 S2 FIRST=S; SECOND=2
BYTE 28	HW_COMPATIBILITY_SECOND	
BYTE 29	BLOCK SIZE LowByte	Unite:byte
BYTE 30	BLOCK SIZE HighByte	
BYTE 31	Write Time LowByte	前一个 Block 结束，到下一个 block 开始的间隔时间。 单位：ms
BYTE 32	Write Time HighByte	

1.5 Firmware Image

The firmware image shall be provided as a binary data file of the data to be sent to the PSU.All data contained in the binary file will be transmitted to the PSU using the protocol defined in this document. The binary file will not be post-processed in any way by the Host System.The binary shall have data on data block boundaries such that the total number of data bytes is divisible by the “Block Size” in Firmware Image Header with no remainder. The “Block Size” must be divisible by 16 with no remainder the PSU FW image is being updated .

Note: there is no checksum or address information stored in a binary file. That is why it is important for a checksum to be embedded in the binary file for the device to check after downloading the image.

1.6 Firmware update process


Step 1
BMC determines PSU FW needs updating?
No
PSU stays in application program mode
Yes
BMC resets retry counter
STATUS(D8h)=0
Step 2
BMC put PSU into Boot Load mode sends 0x01 to MFR_FWUPLOAD_MODE
Increment retry count
Delay 1s to allow PSU to enter FW update mode
PSU starts to run off of Boot Loader code
BMC reads MFR_FWUPLOAD_MODE=0x01?
No
Max retry reached ? (default = 3)
No
Yes
EXIT
Yes
Step 3
BMC reads FW image header In BMC for block size and delay time
BMC sends MFR_FWUPLOAD & 1 st block of image
PSU writes CRC (byte 1 & 2 & 3 & 4 of image) to memory
PSU erases part of application memory & write the 1st image block
STATUS(D8h): bit1=1
Write time delay 1 sec
Step 4
BMC sends MFR_FWUPLOAD & next block of image
PSU erases part of application memory & write The next block of image
Write time delay
Last data block ?
No
Yes
STATUS(D8h): bit1=0
Step 5
PSU verifies that the image has been transferred properly by checking the CRC value
BMC reads MFR_FWUPLOAD_STATUS
Full image received successfully ?
No
Yes
STATUS(D8h): bit0=1
STATUS(D8h): bit2=1
Max retry reached ? (default = 3)
No
Yes
BMC sends 0x00 to MFR_FWUPLOAD_MODE
BMC record FW update fail
No
BMC reads MFR_FWUPLOAD_MODE=0x00 ?
Yes
Step 6
PSU stays in boot loader mode
PSU starts running from application program
PSU application program OK?
No
Yes
PSU verifies Application Program is not corrupted with CRC value
Delay 1s to allow PSU to enter FW application mode
BMC sends 0x00 to MFR_FWUPLOAD_MODE

step1：BMC uses below commands to determine of FW needs updating. BMC will does not to update PSU FW until all below information mate completely

Command code	Command Name
D9h	MFR_FW_REVISION
99h	MFR_ID
9Ah	MFR_MODEL
D6h	MFR_FW_UPLOAD_MODE
D4h	MFR_HW_COMPATIBILITY
D5h	MFR_FW_UPLOAD_CAPABILITY

Step2：PSU transfer to boot loader mode.

Step3：Set FW update parameters and PSU is prepare to update

Step4：BMC write the updating code into PSU

Step5：PSU verifies the updating result

Step6：PSU transfer to application mode

note1：PSU may be in standby mode or ON mode during FW update process

note2：If the FW update process is interrupted at any point during the process; the PSU must always be able to receive new FW update process.

note3：The PSU must always check that the application program is not corrupted before starting to run from the application program

note4：During the FW upload process the PSU must always respond to any communication on the bus; acknowledging its address and the supporting commands without holding the bus. For unsupported commands(not include in PMBUS firmware programming commands) the PSU may respond with Not Acknowledge or 00h.

1.7 Power supply commands

Name: MFR_HW_COMPATIBILITY

Format: Read Word

Code: D4h

Bytes	Value	Description
low	ASCI code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCI code for second letter/number of the PSU HW compatibility.	

Name: MFR_FW_UPLOAD_CAPABILITY

Format: Read Byte

Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

Bit	Value	Description
0	1 = PSU support FW uploading in standby mode only	
1	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.	
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

Name: MFR_FW_UPLOAD_MODE

Format: Read/Write Byte

Code: D6h

Bit	Value	Description
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1 st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7	/	Reserved

Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

Bytes	Value	Description
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 1.5 The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.

Reset: all bits get reset to '0' when the power supply enters FW upload mode

Bit	Description
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3(for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5-15	Reserved

Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

Code: D9h

Bytes	Value	Description	Comments
0	0-255	Minor revision; secondary	Start from 20 while PSU MP
1	0-255	Minor revision; primary	Start from 20 while PSU MP
2	0-255	Bit 7: 1-->Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed, but recommended to follow. 0-->No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision	0x00

MFR_ID (existing PMBus command)
Code: 99h
MFR_MODEL (existing PMBus command)
Code: 9Ah
MFR_REVISION (existing PMBus command)
Code: 9Bh

Revision Record:

Data	Version	Description	Author
2018-9-27	V1.0	Finished refer to intel CRPS design guide rev2.0	Xianke Xiao
2018-10-8	V2.0	Update flow chart	Xianke Xiao
2018-10-22	V3.0	update image header comment	Xianke Xiao