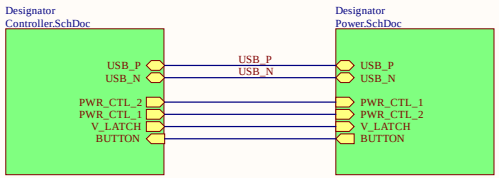
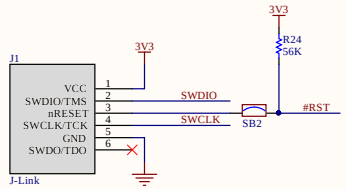
Block Diagram Here

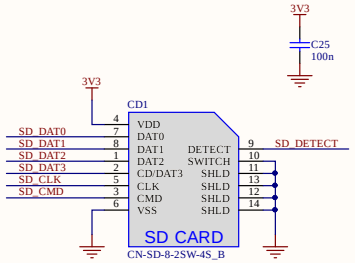


Top		
Variant name	***[No Variations]***	
Number:	Strain Logger	Revision: 0.10
Date:	2018-07-16	Sheet 1 of 4
Drawn by	Jamie Stepanian	
Verified by:		

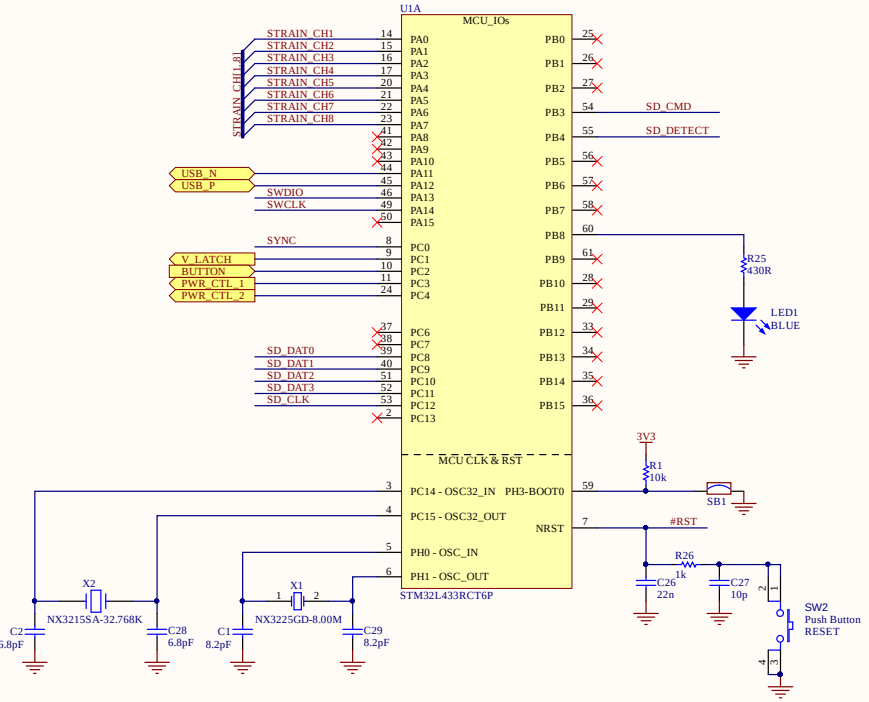
J-LINK TAG-CONNECT DEBUG



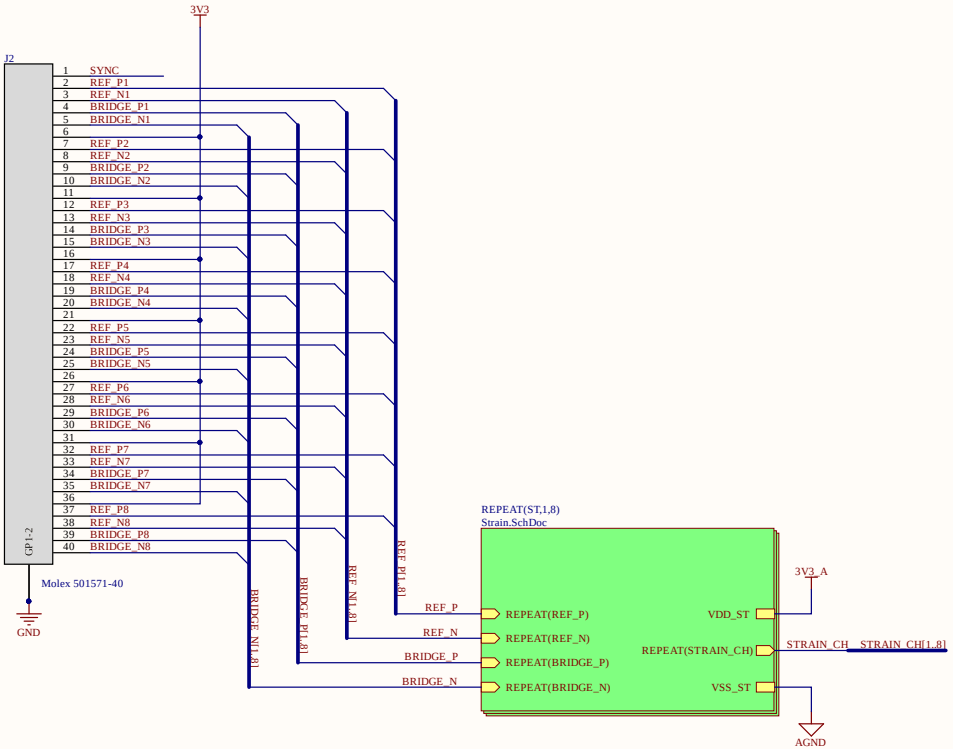
SD CARD



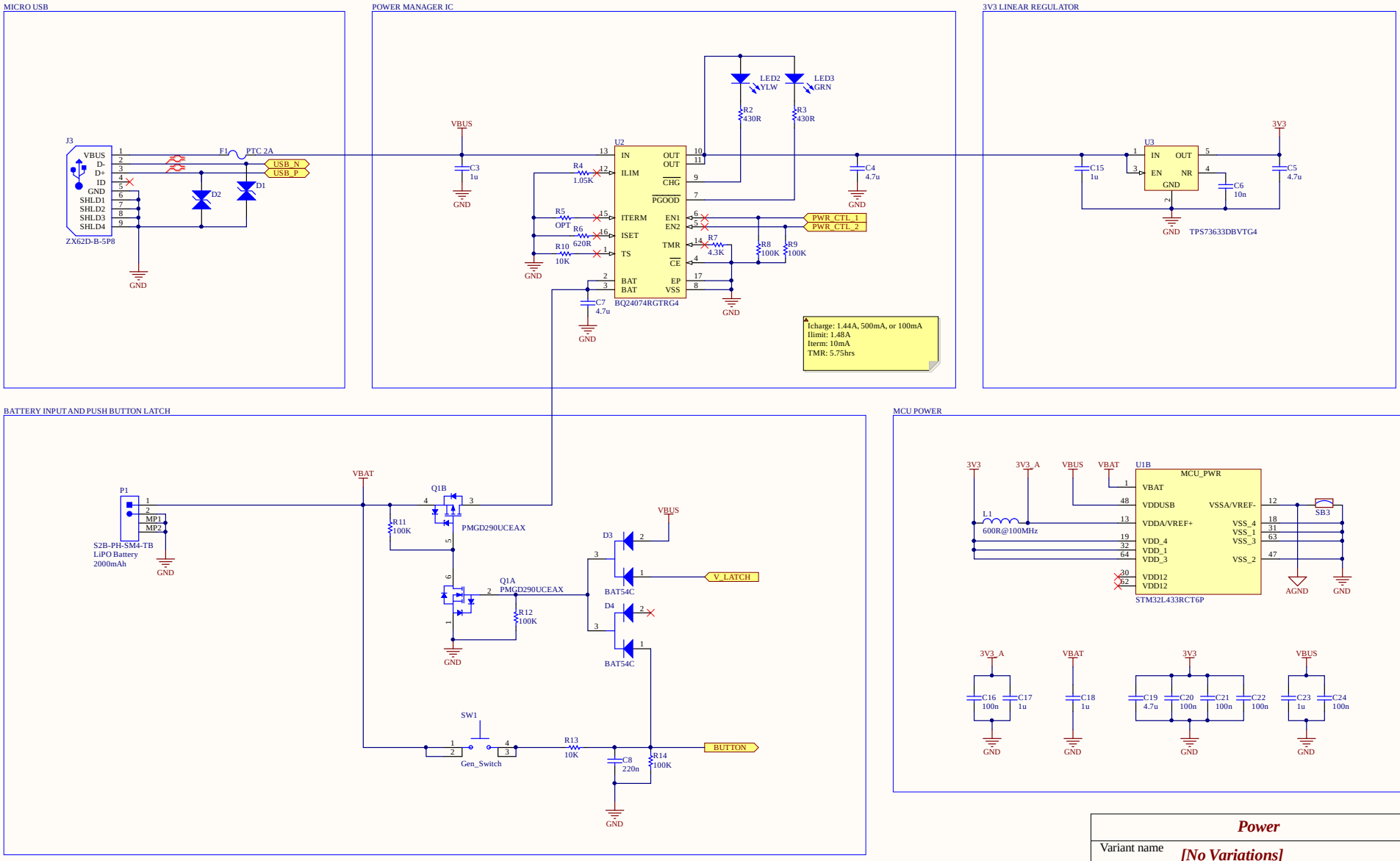
MCU



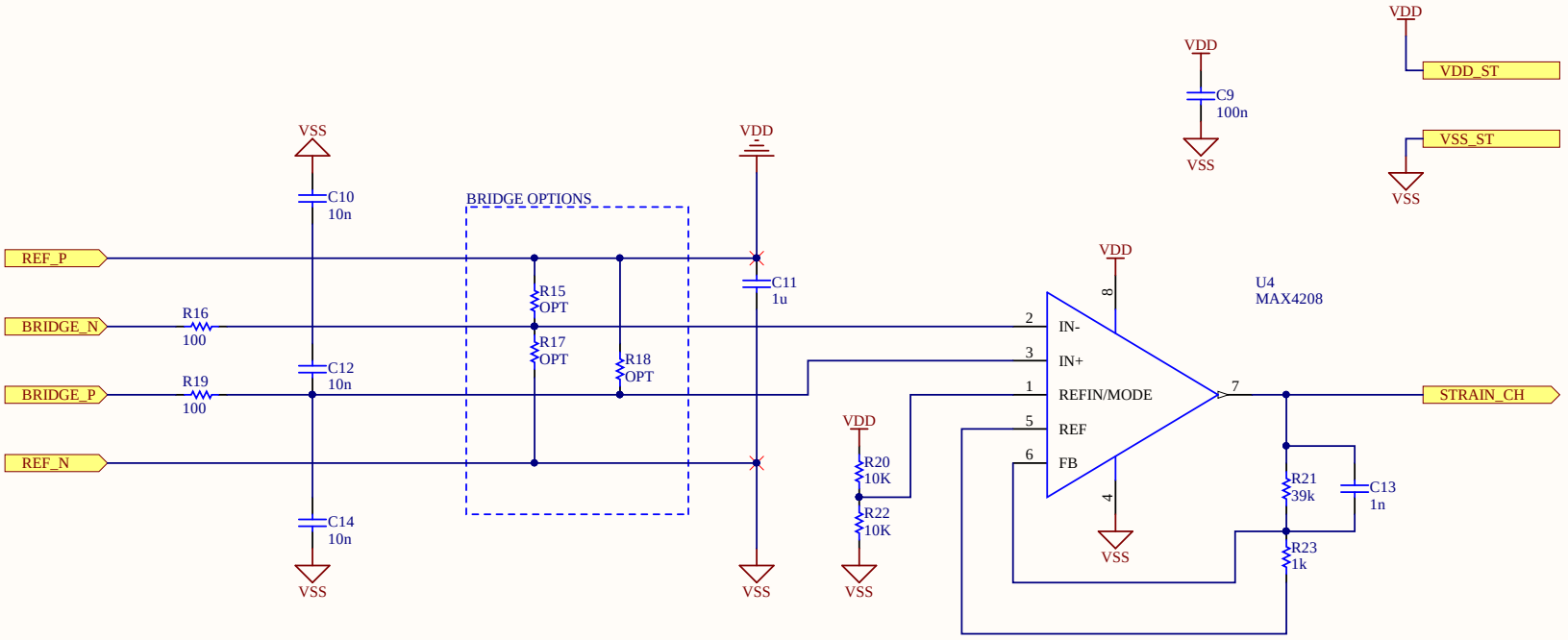
STRAIN GAUGES AND SYNC LINE



Controller		
Variant name	*[No Variations]*	
Number:	Strain Logger	Revision: 0.10
Date:	2018-07-16	Sheet 2 of 4



Power		
Variant name	*[No Variations]*	
Number:	Strain Logger	Revision: 0.10
Date:	2018-07-16	Sheet 3 of 4



Full Bridge (4 wire): Do not populate R15, R17, and R18.
Half Bridge (3 wire): Populate R15 and R17 with 350R 0.01%.
Quarter Bridge (2 wire): Populate R15, R17, and R18 with 350R 0.01%.

AMP SETTINGS
Vref: 1.65V
Gain: 40

Strain Gauge Frontend		
Variant name	***[No Variations]***	
Number:	Strain Logger	Revision: 0.10
Date:	2018-07-16	Sheet 4 of 4