Exploration: The Data Link Layer

Introduction

Welcome to the Data Link layer. The link layer is implemented in every host in the network, every router, and every addressable hardware device in the entire internet.

When we discuss the link layer, we are going to refer to the hosts and routers as nodes, and the communication channels that connect them are called links. We have wired and wireless links, and sometimes the network itself can act as a link.

In this exploration we will examine:

- Layering abstractions (recapping the difference between layers)
- Link-layer responsibilities, protocols, and implementation
- Hardware and the NIC card
- Error detection and parity checks

Layering abstractions

First, we will compare the data-link layer with the transport and network layers in terms of description, responsibilities, and data units:

transport layer: logical communication between processes

- relies on, enhances, network layer services
- the transport-layer unit is called a segment

network layer: logical communication between hosts

- relies on, enhances, link layer services
- the network-layer unit is called a datagram

data-link layer: logical communication between adjacent nodes

- relies on, enhances, physical layer services
- the link-layer unit is called a frame

Link-layer responsibilities

- Provide the hardware addresses used in frame headers
- Encapsulate the IP datagram into frame
- Get access to the shared medium
- Control flow between adjacent sending and receiving nodes
- Detect/correct errors (bit-level at receiver)

Link-layer protocols

The protocol standards for the link layer are dependent on the actual link, which is where the hardware meets the software. Frames may be delivered by different link-layer protocols over different links, for instance, Ethernet on first link, frame-relay on intermediate links, and 802.11 on the final link.

The Link-layer protocols may provide different services, again depending on the link. For instance, they may or may not provide reliable data transfer (similar to TCP with ACK's and retransmission). Reliable delivery between adjacent nodes is rarely used on low bit-error link (fiber, most twisted pair), but often used on wireless links because of high error rates.

Hardware and the NIC card

The link layer is required on every host, and implements the interface to the physical media. It is implemented mostly in hardware and resides on the Network Interface Controller (NIC) card.

A NIC card is almost a computer itself: It has a processing unit. It has hardware, software, and firmware. It connects into the system bus and can take advantage of Direct Memory Access (DMA). DMA can strip out the data from a datagram and fill up a buffer in computer memory without involving the computer's cpu. A NIC card is also capable of doing checksum processing as far up as the transport layer.

To sum up, a NIC card is a very powerful sub-computer that connects the host computer to the physical layer of the network.

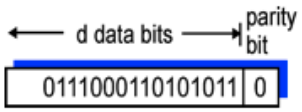
Error detection / correction and parity checks

There are several types of error detection / correction that occur in the link-layer. Examples include parity checks (both 1 and 2 dimensional), checksums, cyclic redundancy check (CRC) and Hamming codes. Here we discuss parity checks.

Parity checks count the number of "1" bits in data bytes or words. A parity bit is added and included in the count. The parity bit will be set to 1 or 0 to make the count even or odd, depending on the type of parity check used. Here are several examples:

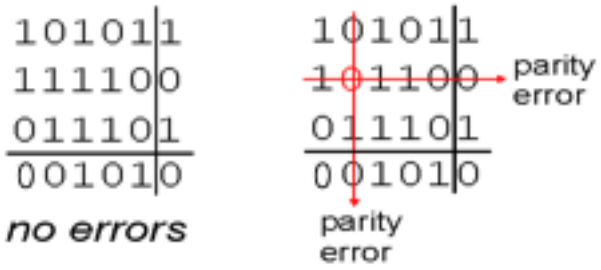
7 bits of data	Count of 1 bits	Even parity byte	Odd parity byte
0000000	0	0 0000000	1 0000000
1010001	3	1 1010001	0 1010001
1101001	4	0 1101001	1 1101001
1111111	7	1 1111111	0 1111111

In practice, the sender will calculate the parity bit for every d data bits, then send the data to the receiver. The receiver need only perform the count and check the parity bit to see if an error has occurred.



This data word has a bit count of 9. If we are using an even parity check, and since the parity bit is 0, we can say that an error has occurred somewhere in the d data bits (or the parity bit itself).

A 1-dimensional parity check has an obvious problem. Two errors in the same checked set of bits will go undetected. A more robust approach with error-correction capabilities, is the 2-dimensional parity check. With 2D parity, checks are performed on rows and columns of data. When there is an error, it should be detected in both a row and column. Where the row and column cross defines the error bit, which may now be corrected.

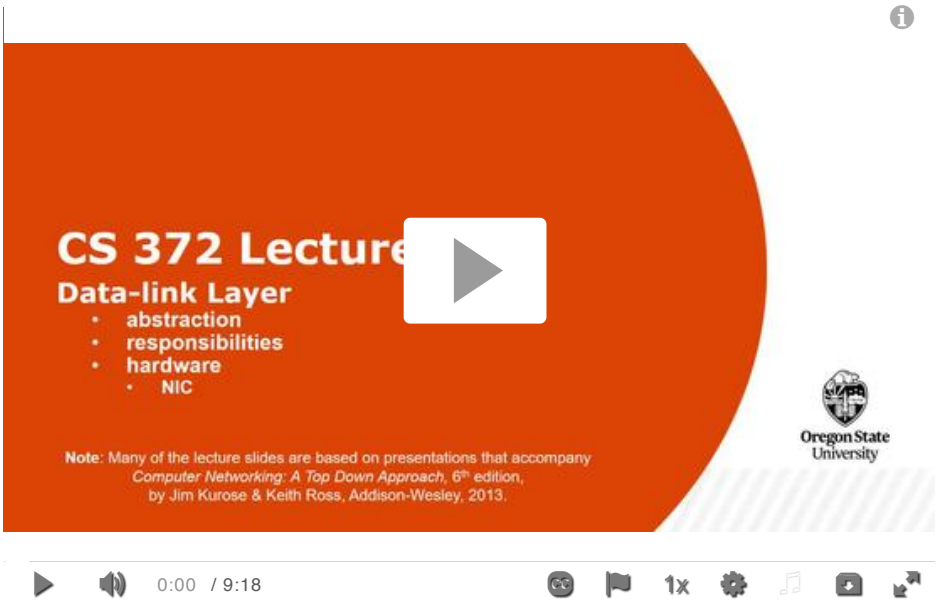


In both images, the bottom row and right-most column are the parity bits. In the right image, the row and column with errors point to the bit that flipped in transmission.

For more on the Link-layer, including a more in-depth discussion of error-checking, be sure to watch the video lecture, then test your knowledge with the Self-Check exercises below.

Video Lecture

Data Link Layer



(PDF (https://oregonstate.instructure.com/courses/1798856/files/83165297/download?wrap=1) (https://oregonstate.instructure.com/courses/1798856/files/83165297/download?wrap=1) |PPT (https://oregonstate.instructure.com/courses/1798856/files/83165038/download?wrap=1) (https://oregonstate.instructure.com/courses/1798856/files/83165038/download?wrap=1))

Self-Check Exercises

What are some of the responsibilities of the link layer?

Turn

Card 1 of 4

A datagram may be encapsulated into multiple different types of frames as it transits the internet.

○ True ○ False

Here are 7 consecutive bytes in a datagram that uses 2-dimensional even parity for error detection/correction.

Byte #	Code	Parity
1	1001110	0
2	1000101	1
3	1010100	1
4	1010111	1
5	1000011	0
6	1010010	1
7	1001011	0
Parity	1011010	0

Which byte has an error?

Turn

Card 1 of 2

Reuse <> Embed

Resources

IGCSE Computer Science - Parity Checking