# ALLEGREX<sup>TM</sup> FPU Instruction List

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### **MIPS Instruction List**

Inst.	Description	Category
add	Add	MIPS I
addi	Add Immediate	MIPS I
addiu	Add Immediate Unsigned	MIPS I
addu	Add Unsigned	MIPS I
and	AND	MIPS I
andi	AND Immediate	MIPS I
beq	Branch on Equal	MIPS I
beql	Branch on Equal Likely	MIPS II
bgez	Branch on Greater than or Equal to Zero	MIPS I
bgezal	Branch on Greater than or Equal to Zero And Link	MIPS I
bgezall	Branch on Greater than or Equal to Zero And Link Likely	MIPS II
bgezl	Branch on Greater than or Equal to Zero Likely	MIPS II
bgtz	Branch on Greater Than Zero	MIPS I
bgtzl	Branch on Greater Than Zero Likely	MIPS II
blez	Branch on Less than or Equal to Zero	MIPS I
blezl	Branch on Less than or Equal to Zero Likely	MIPS II
bltz	Branch on Less Than Zero	MIPS I
bltzal	Branch on Less Than Zero And Link	MIPS I
bltzall	Branch on Less Than Zero And Link Likely	MIPS II
bltzl	Branch on Less Than Zero Likely	MIPS II
bne	Branch on Not Equal	MIPS I
bnel	Branch on Not Equal Likely	MIPS II
break	Break Point	MIPS I
div	Divide	MIPS I
divu	Divide Unsigned	MIPS I
eret	Exception Return	MIPS III
j	Jump	MIPS I
jal	Jump And Link	MIPS I
jalr	Jump And Link Register	MIPS I
jr	Jump Register	MIPS I
lb	Load Byte	MIPS I
lbu	Load Byte Unsigned	MIPS I
lh	Load HalfWORD	MIPS I
lhu	Load HalfWORD Unsigned	MIPS I
lui	Load Upper Immediate	MIPS I
lw	Load WORD	MIPS I
lwl	Load WORD Left	MIPS I
lwr	Load WORD Right	MIPS I
mfc0	Move From Coprocessor0	MIPS I
mfhi	Move From HI Register	MIPS I
mflo	Move From LO Register	MIPS I
mtc0	Move To Coprocessor0	MIPS I
mthi	Move To HI Register	MIPS I
mtlo	Move To LO Register	MIPS I
mult	Multiply	MIPS I
multu	Multiply Unsigned	MIPS I
nop	No Operation	MIPS I

Inst.	Description	Category
nor	NOR	MIPS I
or	OR	MIPS I
ori	OR Immediate	MIPS I
sb	Store Byte	MIPS I
sh	Store HalfWORD	MIPS I
sll	Shift Left Logical	MIPS I
sllv	Shift Left Logical Variable	MIPS I
slt	Set on Less Than	MIPS I
slti	Set on Less Than Immediate	MIPS I
sltiu	Set on Less Than Immediate Unsigned	MIPS I
sltu	Set on Less Than Unsigned	MIPS I
sra	Shift Right Arithmetic	MIPS I
srav	Shift Right Arithmetic Variable	MIPS I
srl	Shift Right Logical	MIPS I
srlv	Shift Right Logical Variable	MIPS I
sub	Subtract	MIPS I
subu	Subtract Unsigned	MIPS I
sw	Store WORD	MIPS I
swl	Store WORD Left	MIPS I
swr	Store Word Right	MIPS I
syscall	System Call	MIPS I
xor	XOR	MIPS I
xori	Exclusive OR Immediate	MIPS I

### **ALLEGREX™** Instruction List

Inst.	Description	Category
clo	Count Leading One	$ALLEGREX^{TM}$
clz	Count Leading Zero	ALLEGREX <sup>TM</sup>
madd	Multiply Add	ALLEGREX <sup>TM</sup>
maddu	Multiply Add Unsigned	ALLEGREX <sup>TM</sup>
msub	Multiply Substract	ALLEGREX <sup>TM</sup>
msubu	Multiply Substract Unsigned	ALLEGREX <sup>TM</sup>
max	Select Max	ALLEGREX <sup>TM</sup>
min	Select Min	$ALLEGREX^{TM}$
movn	Move Conditional on Zero	$ALLEGREX^{TM}$
movz	Move Conditional on Not Zero	ALLEGREXTM
ext	Extract Bit Field	ALLEGREX <sup>TM</sup>
ins	Insert Bit Field	ALLEGREX™
seb	Sign-Extend Byte	ALLEGREX™
seh	Sign-Extend Halfword	ALLEGREX™
bitrev	Bit Reverse	ALLEGREX™
rotr	Rotate Word Right	$ALLEGREX^{TM}$
rotrv	Rotate Word Right Variable	$ALLEGREX^{TM}$
wsbh	Word Swap Bytes within Halfward	ALLEGREX™
wsbw	Word Swap Bytes within Word	ALLEGREX™
cache	Index Invalidate (I)	ALLEGREX™
cache	Index Unlock (I)	ALLEGREX™
cache	Hit Invalidate (I)	$ALLEGREX^{TM}$
cache	Fill (I)	$ALLEGREX^{TM}$
cache	Fill with Lock (I)	$ALLEGREX^{TM}$
cache	Index Writeback Invalidate (D)	$ALLEGREX^{TM}$
cache	Index Unlock (D)	$ALLEGREX^{TM}$
cache	Create Dirty Exclusive (D)	$ALLEGREX^{TM}$
cache	Hit Invalidate (D)	$ALLEGREX^{TM}$
cache	Hit WriteBack (D)	$ALLEGREX^{TM}$
cache	Hit WriteBack Invalidate(D)	$ALLEGREX^{TM}$
cache	Create Dirty Exclusive with Lock (D)	$ALLEGREX^{TM}$
cache	Fill (D)	ALLEGREX <sup>TM</sup>
cache	Fill with Lock (D)	$ALLEGREX^{TM}$
sync	Synchronize Shared Memory	$ALLEGREX^{TM}$
11	Load Linked	ALLEGREX <sup>TM</sup>
sc	Store Conditional	$ALLEGREX^{TM}$

### **FPU Instruction List**

Inst.	Description	Category
abs.s	Floating-point Absolute Value	FPU
add.s	Floating-point Add	FPU
bc1f	Branch on FPU False	MIPS I
5011	Branch on 11 6 1 also	FPU
bc1fl	Branch on FPU False Likely	MIPS II
DCIII	Branch on 11 of talse Entery	FPU
bc1t	Branch on FPU True	MIPS I
DCTU	Branch on 11 6 1146	FPU
bc1tl	Branch on FPU True Likely	MIPS II
50101	Branch on 11 6 11 de Britory	FPU
c.f.s	Floating-point Compare (False)	FPU
c.un.s	Floating-point Compare (Unordered)	FPU
	Floating point Compare (Equal)	FPU
c.eq.s	Floating point Compare (Equal)  Floating-point Compare (Unordered or Equal)	FPU
c.ueq.s	Floating point Compare (Ordered Less Than)	FPU
c.ult.s	Floating-point Compare (Ordered Less Than)  Floating-point Compare	FPU
c.uit.s	(Unordered or Less Than)	FPU
c.ole.s	· · · · · · · · · · · · · · · · · · ·	FPU
c.oie.s	Floating-point Compare (Ordered Less Than or Equal)	FPU
1	*	EDII
c.ule.s	Floating-point Compare	FPU
C -	(Unordered or Less than or Equal)	FPU
c.sf.s	Floating-point Compare (Signaling False)	_
c.ngle.s	Floating-point Compare	FPU
	(Not Greater than or Less than or Equal)	EDII
c.seq.s	Floating-point Compare (Signaling Equal)	FPU
c.ngl.s	Floating-point Compare	FPU
1,	(Not Greater than or Less than)	DDII
c.lt.s	Floating-point Compare (Less Than)	FPU
c.nge.s	Floating-point Compare	FPU
1	(Not Greater than or Equal)	DDII
c.le.s	Floating-point Compare (Less than or Equal)	FPU
c.ngt.s	Floating-point Compare (Not Greater Than)	FPU
ceil.w.s	Ceiling to Word from Single	FPU
cfc1	Move Control from FPU	MIPS I
		FPU
ctc1	Move Control to FPU	MIPS I
		FPU
cvt.s.w	Convert To Single from Word	FPU
cvt.w.s	Convert To Word from Single	FPU
div.s	Floating-point Divide	FPU
floor.w.s	Floor to Word from Single	FPU
lwc1	Load Word to FPU	MIPS I
		FPU
mfc1	Move From FPU	MIPS I
		FPU
mov.s	Floating-point Move	FPU
mtc1	Move To FPU	MIPS I
		FPU

Inst.	Description	Category
mul.s	Floating-point Multiply	FPU
neg.s	Floating-point Negate	FPU
round.w.s	Round To Word from Single	FPU
sqrt.s	Floating-point Square Root	FPU
sub.s	Floating-point Subtract	FPU
swc1	Store Word from FPU	MIPS I
		FPU
trunc.w.s	Truncate To Word from Single	FPU