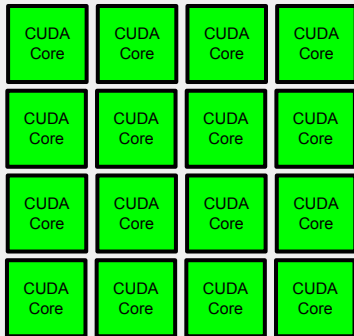
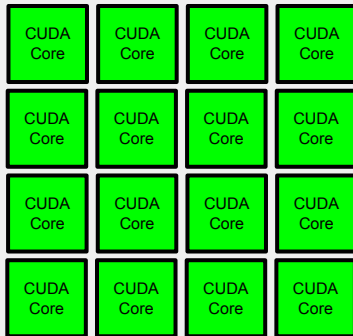


SM 1



L1 cache / shared
memory

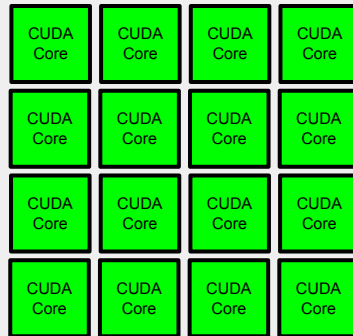
SM 2



L1 cache / shared
memory



SM N



L1 cache / shared
memory

L2 cache

Global memory