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32-Bit Microcontroller FM4 Family Peripheral Manual Analog Macro Part

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Preface

Thank you for your continued use of Cypress products.

Read this manual and the data sheet thoroughly before using products in this family.

Purpose of This Manual / Intended Readers

This manual explains the functions and operations of this family and describes how they are used. The manual is intended for engineers engaged in the actual development of products using this family.

For the descriptions of the Analog macro, Timer, and Communication Macro, see the respective separate peripheral manuals.

Note:

- This manual explains the configuration and operation of the peripheral functions, but does not cover the specifics of each device in the series.
 - Users should refer to the respective data sheets of devices for device-specific details.
- Whether a peripheral function is on board or not is dependent on product type. See data sheets for details.

Sample Programs and Development Environment

Cypress offers sample programs free of charge for using the peripheral functions of the FM4 family. Cypress also makes available descriptions of the development environment required for this family. Feel free to use them to verify the operational specifications and usage of this Cypress microcontroller.

Microcontroller Support Information:

https://community.cypress.com/community/MCU

Note:

 Note that the sample programs are subject to change without notice. Since they are offered as a way to demonstrate standard operations and usage, evaluate them sufficiently before running them on your system.

Cypress assumes no responsibility for any damage that may occur as a result of using a sample program.

Overall Organization of This Manual

Peripheral Manual Analog macro part has 2 chapters and Appendixes as shown below.

CHAPTER 1-1: A/D Converter

CHAPTER 1-2: 12-bit A/D Converter

CHAPTER 1-3: A/D Timer Trigger Selection

CHAPTER 2: 12-bit D/A Converter

Appendixes



Related Manuals

The manuals related to this family are listed below. See the manual appropriate to the applicable conditions.

The contents of these manuals are subject to change without notice. Contact us to check the latest versions available.

Peripheral Manual

■ FM4 Family Peripheral Manual (002-04856)

Called Peripheral Manual hereafter

■ FM4 Family Peripheral Manual Timer Part (002-04858)

Called Timer Part hereafter

■ FM4 Family Peripheral Manual Analog Macro Part (this manual)

Called Analog Macro Part hereafter

■ FM4 Family Peripheral Manual Communication Macro Part (002-04862)

Called Communication Macro Part hereafter

■ FM4 Family Peripheral Manual GDC Part (002-04917)

Called GDC Part hereafter

Data Sheet

For details about device-specific, electrical characteristics, package dimensions, ordering information etc., see the following document.

■ 32-bit Microcontroller FM4 Family Data Sheet

Note:

The data sheets for each series are provided.
 See the appropriate data sheet for the series that you are using.

CPU Programming Manual

For details about Arm Cortex-M4F core, see the following documents that can be obtained from http://www.arm.com/.

- Cortex-M4 Technical Reference Manual
- Arm v7-M Architecture Application Level Reference Manual

Flash Programming Manual

For details about the functions and operations of the built-in flash memory, see the following document.

■ FM4 Family Flash Programming Manual

Note:

Flash programming manuals for each series are provided.
 See the appropriate flash programming manual for the series that you are using.



How to Use This Manual

Finding a Function

The following methods can be used to search for the explanation of a desired function in this manual:

■ Search from the table of the contents

The table of the contents lists the manual contents in the order of description.

■ Search from the register

The address where each register is located is not described in the text. To verify the address of a register, see A. Register Map in Appendixes.

About the Chapters

Basically, this manual explains 1 peripheral function per chapter.

Terminology

This manual uses the following terminology.

Term	Explanation
Word	Indicates access in units of 32 bits.
Half word	Indicates access in units of 16 bits.
Byte	Indicates access in units of 8 bits.

Notations

■ The notations in bit configuration of the register explanation of this manual are written as follows.

bit: bit numberField: bit field name

- Attribute: Attributes for read and write of each bit

R: Read onlyW: Write only

• R/W: Readable/Writable

· -: Undefined

- Initial value: Initial value of the register after reset

0: Initial value is 01: Initial value is 1

• X: Initial value is undefined

- The multiple bits are written as follows in this manual.
- Example: bit7:0 indicates the bits from bit7 to bit0
- The values such as for addresses are written as follows in this manual.

Hexadecimal number: 0x is attached in the beginning of a value as a prefix (example : 0xFFFF)
 Binary number: 0b is attached in the beginning of a value as a prefix (example: 0b1111)

- Decimal number: Written using numbers only (example: 1000)



The Target Products in This Manual

■ In this manual, the products are classified into the following groups and are described follows.

For the descriptions such as "TYPE1-M4", see the relevant items of the target product in the list below.

Table 1 TYPE1-M4 Product List

Description in	Description in Flash memory size		
this manual	1024 Kbytes	768 Kbytes	512 Kbytes
TYPE1-M4	MB9BF568M	MB9BF567M	MB9BF566M
	MB9BF568N	MB9BF567N	MB9BF566N
	MB9BF568R	MB9BF567R	MB9BF566R
	MB9BF568RF	CY9BF567M	CY9BF566M
	CY9BF568M	CY9BF567N	CY9BF566N
	CY9BF568N	CY9BF567R	CY9BF566R
	CY9BF568R		
	CY9BF568RF		
	MB9BF468M	MB9BF467M	MB9BF466M
	MB9BF468N	MB9BF467N	MB9BF466N
	MB9BF468R	MB9BF467R	MB9BF466R
	CY9BF468M	CY9BF467M	CY9BF466M
	CY9BF468N	CY9BF467N	CY9BF466N
	CY9BF468R	CY9BF467R	CY9BF466R
	MB9BF368M	MB9BF367M	MB9BF366M
	MB9BF368N	MB9BF367N	MB9BF366N
	MB9BF368R	MB9BF367R	MB9BF366R
	CY9BF368M	CY9BF367M	CY9BF366M
	CY9BF368N	CY9BF367N	CY9BF366N
	CY9BF368R	CY9BF367R	CY9BF366R
	MB9BF168M	MB9BF167M	MB9BF166M
	MB9BF168N	MB9BF167N	MB9BF166N
	MB9BF168R	MB9BF167R	MB9BF166R
	CY9BF168M	CY9BF167M	CY9BF166M
	CY9BF168N	CY9BF167N	CY9BF166N
	CY9BF168R	CY9BF167R	CY9BF166R



Table 2 TYPE2-M4 Product List

Description in		Flash memory size		
this manual	512 Kbytes	384 Kbytes	256 Kbytes	
TYPE2-M4	MB9BF566K	MB9BF565K	MB9BF564K	
	MB9BF566L	MB9BF565L	MB9BF564L	
	CY9BF566K	CY9BF565K	CY9BF564K	
	CY9BF566L	CY9BF565L	CY9BF564L	
	MB9BF466K	MB9BF465K	MB9BF464K	
	MB9BF466L	MB9BF465L	MB9BF464L	
	CY9BF466K	CY9BF465K	CY9BF464K	
	CY9BF466L	CY9BF465L	CY9BF464L	
	MB9BF366K	MB9BF365K	MB9BF364K	
	MB9BF366L	MB9BF365L	MB9BF364L	
	CY9BF366K	CY9BF365K	CY9BF364K	
	CY9BF366L	CY9BF365L	CY9BF364L	
	MB9BF166K	MB9BF165K	MB9BF164K	
	MB9BF166L	MB9BF165L	MB9BF164L	
	CY9BF166K	CY9BF165K	CY9BF164K	
	CY9BF166L	CY9BF165L	CY9BF164L	

Table 3 TYPE3-M4 Product List

Description		Flash memory size		No-Flash
in this	2 Mbytes	1.5 Mbytes	1 Mbytes	SRAM size
manual				256 Kbytes
TYPE3-M4	S6E2CCAL	S6E2CC9L	S6E2CC8L	-
	S6E2CCAJ	S6E2CC9J	S6E2CC8J	
	S6E2CCAH	S6E2CC9H	S6E2CC8H	
	S6E2C5AL	S6E2C59L	S6E2C58L	-
	S6E2C5AJ	S6E2C59J	S6E2C58J	
	S6E2C5AH	S6E2C59H	S6E2C58H	
	S6E2C4AL	S6E2C49L	S6E2C48L	-
	S6E2C4AJ	S6E2C49J	S6E2C48J	
	S6E2C4AH	S6E2C49H	S6E2C48H	
	S6E2C3AL	S6E2C39L	S6E2C38L	-
	S6E2C3AJ	S6E2C39J	S6E2C38J	
	S6E2C3AH	S6E2C39H	S6E2C38H	
	S6E2C2AL	S6E2C29L	S6E2C28L	-
	S6E2C2AJ	S6E2C29J	S6E2C28J	
	S6E2C2AJH	S6E2C29H	S6E2C28JH	
	S6E2C1AL	S6E2C19L	S6E2C18L	S6E2C10L
	S6E2C1AJ	S6E2C19J	S6E2C18J	S6E2C10J
	S6E2C1AH	S6E2C19H	S6E2C18H	S6E2C10H



Table 4 TYPE4-M4 Product List

	Flash memory s	size 384 Kbytes	
Description in this		VRAM 512 Kbytes	
manual	VRAM 512 Kbytes	+	
		VFLASH 2 Mbytes	
	S6E2D35G0	S6E2D35GJ	
	S6E2D35J0	30L2D33G3	
	S6E2D55G0	S6E2D55GJ	
TYPE4-M4	S6E2D55J0	36E2D33GJ	
1 1 F E 4-1V14	S6E2DF5G0	S6E2DF5GJ	
	S6E2DF5J0	30L2D1 303	
	S6E2DH5G0	S6E2DH5GJ	
	S6E2DH5J0	SULZDIOGJ	

Table 5 TYPE5-M4 Product List

Description in	Flash me	mory size
this manual	1 Mbytes	512 Kbytes
TYPE5-M4	S6E2GM8J	S6E2GM6J
	S6E2GM8H	S6E2GM6H
	S6E2GK8J	S6E2GK6J
	S6E2GK8H	S6E2GK6H
	S6E2GH8J	S6E2GH6J
	S6E2GH8H	S6E2GH6H
	S6E2G28J	S6E2G26J
	S6E2G28H	S6E2G26H
	S6E2G38J	S6E2G36J
	S6E2G38H	S6E2G36H

Table 6 TYPE6-M4 Product List

Description in	Flash memory size	
this manual	512 Kbytes	256 Kbytes
TYPE6-M4	S6E2HG6G	S6E2HG4G
	S6E2HG6F	S6E2HG4F
	S6E2HG6E	S6E2HG4E
	S6E2HE6G	S6E2HE4G
	S6E2HE6F S6E2	
	S6E2HE6E	S6E2HE4E
	S6E2H46G S6E2H44	
S6E2H46F S6E2H46		S6E2H44F
S6E2H46E S6		S6E2H44E
	S6E2H16G S6E2	
	S6E2H16F S6E2H	
	S6E2H16E	S6E2H14E

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CHAPTER 1-1: A/D Converter



This chapter explains the functions and operations of the A/D converter.

- 1. Configuration
- 2. Functions and Operations
- 3. Usage Precautions



1. Configuration

The A/D converter converts analog input voltage from an external pin to a digital value.

A/D Converter Configuration

- The maximum 3 units of A/D converters with 12-bit resolution have been installed.
- Any channel can be selected to any unit from the maximum 32 channels of analog input.
- The following triggers can be selected as an activation trigger for A/D conversion.
 - Priority conversion activation trigger
 - Trigger input from an external pin
 - Timer trigger input (base timer or multifunction timer)
 - Software activation
 - Scan conversion activation trigger
 - Timer trigger input (base timer or multifunction timer)
 - Software activation

Figure 1-1 shows a block diagram of the A/D converter with the related circuits.



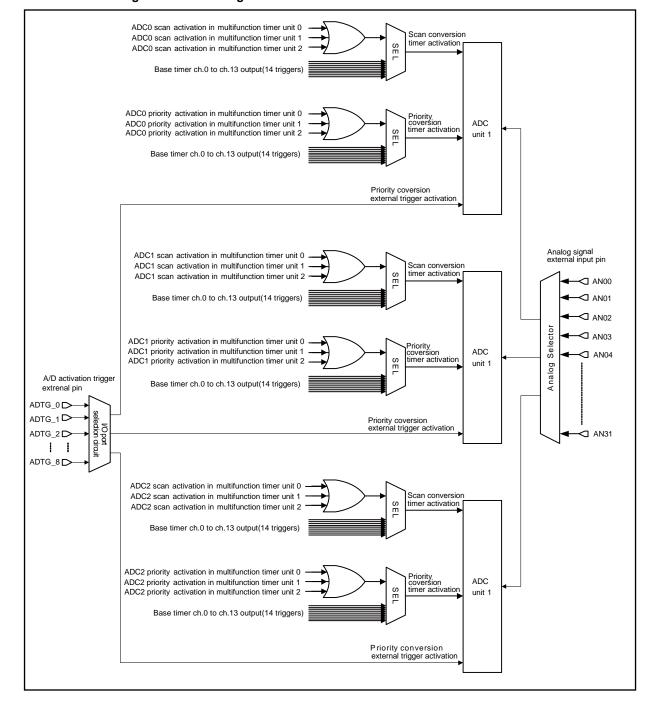


Figure 1-1 Block Diagram of the A/D Converter with the Related Circuits



2. Functions and Operations

See descriptions of the following related chapters for functions and operations of the A/D converter.

12-bit A/D Converter Operation

See the chapter about the 12-bit A/D Converter for conversion operations of the 12-bit A/D converter.

12-bit A/D Timer Trigger Select Operation

See the chapter about the A/D Timer Trigger Selection for operations of the 12-bit A/D converter timer trigger selection.



3. Usage Precautions

■ Simultaneous A/D conversion of multiple channels is possible on the products that have multiple A/D converters.

Do not select the same input channel with the multiple units.

- Some channels of an analog input cannot be used for certain products. Do not change the selection registers (SCIS0, SCIS1, SCIS2, and SCIS3) or the sampling time selection registers (ADSS0, ADSS1, ADSS2, and ADSS3) for the channels that cannot be used from their initial values.
- In this family, P1A[2:0] of the priority conversion input selection register (PCIS) should be selected for an analog input channel during priority conversion. Always write 0 to the ESCE bit of the priority conversion control register (PCCR) of the 12-bit A/D converter.
- DMA transfer using the A/D interrupt request generation of this family supports only DMA transfer using generation of a scan conversion interrupt request. DMA transfer using a priority conversion interrupt request is not supported.
- Product specifications and Number of channels mounted

 The number of analog inputs mounted and the number of base timer channels used for AD Startup trigger are different by products.

For details, see Product Configuration in Data Sheet of the product used.

CHAPTER 1-1: A/D Converter



CHAPTER 1-2: 12-bit A/D Converter



This chapter explains the functions and operations of the 12-bit A/D converter.

- 1. Overview
- 2. Configuration
- 3. Explanation of Operations
- 4. Setup procedure Examples
- 5. Registers



1. Overview

The 12-bit A/D converter is a function that converts analog input voltages into 12-bit digital values using a type of the RC Successive Approximation register.

Features of the 12-bit A/D Converter

- 12-bit resolution
- Converter using a type of RC Successive Approximation register with sample and hold circuits
- Two sampling times selectable for each input channel
- Scan conversion operation:
 - Multiple analog inputs can be selected from multiple channels.
 - Start factors are software and timers.
 - Repeat mode is available.
- Priority conversion operation:

Even during scan operation, if a start factor of priority conversion occurs, it is possible to interrupt the ongoing scan conversion and perform conversion with high priority (There are two priority levels: 1 and 2. Priority level 1 is higher than priority level 2.).

Start factors are software and timers (priority level 2), and external triggers (priority level 1).

- FIFO function:
 - Sixteen FIFO stages for scan conversion and four FIFO stages for priority conversion are incorporated.
 - An interrupt is generated when data is written in the specified count of FIFO stages.
- Changeable A/D conversion data placement (selectable between shift to the MSB side and shift to LSB side)
- The A/D conversion result comparison function is available.
- Range comparison function
 - Upper and lower limits can be specified
 - Either detection of within the range or without the range can be set.
 - With the continuous detection, the noise can be removed. The continuous detection time can be specified from 1 to 7.
 - For the detection of without the range, over the upper limit or below the lower limit can be specified.
- There are five interrupt factors as follows:
 - 1. Scan conversion FIFO stage count interrupt
 - 2. Priority conversion FIFO stage count interrupt
 - 3. FIFO overrun interrupt (for both scan and priority conversion processes)
 - 4. A/D conversion result comparison interrupt
 - 5. Range comparison interrupt
- DMA transfer triggered by an interrupt request.

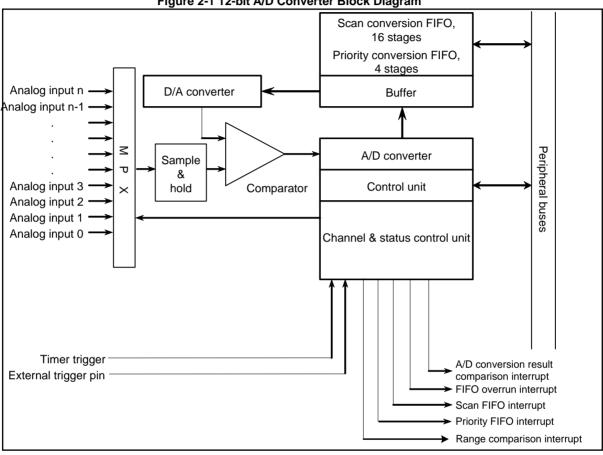


Configuration 2.

This section provides the configuration of the 12-bit A/D converter.

12-bit A/D Converter Block Diagram

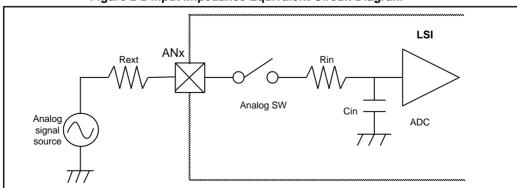
Figure 2-1 12-bit A/D Converter Block Diagram



Input Impedance

The sampling circuit of the A/D converter is shown as an equivalent circuit in Figure 2-2. See the "Electrical Characteristics" in "Data Sheet" to make sure that the external impedance, Rext should be selected not to exceed the sampling time.

Figure 2-2 Input Impedance Equivalent Circuit Diagram





3. Explanation of Operations

This section explains the operations of the 12-bit A/D converter.

- 3.1. Enabling Operations of the A/D Converter
- 3.2. A/D Conversion Operation
- 3.3. FIFO Operations
- 3.4. A/D Comparison Function
- 3.5. Range Comparison Function
- 3.6. Starting DMA



3.1 Enabling Operations of the A/D Converter

This section explains enabling operations of the A/D converter.

The A/D converter must be in the operation enable state prior to A/D conversion. Writing "1" to the ENBL bit of the A/D Operation Enable Setup Register (ADCEN) turns the A/D converter from the operation stop state to the operation enable state after the period of operation enable state transitions. On the other hand, writing "0" to the ENBL bit of the ADCEN register turns the A/D converter immediately to the operation stop state.

A/D conversion can be performed only in the operation enable state. An A/D conversion request in the operation stop state is ignored. If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

Reading the READY bit of the ADCEN register allows you to check whether the A/D converter is in the operation enable state or not.



3.2 A/D Conversion Operation

The A/D converter can perform two types of conversion processes: scan conversion and priority conversion.

- 3.2.1. Scan Conversion Operation
- 3.2.2. Priority Conversion Operation
- 3.2.3. Priority Levels and State Transitions



3.2.1 Scan Conversion Operation

This section explains the scan conversion operation.

The input channels are selected in the Scan Conversion Input Selection Register (SCIS). By setting the corresponding bit in the SCIS to 1, any necessary channel can be selected from among multiple analog input channels.

The A/D converter can be started by software or a timer. To start the converter by software, set the SSTR bit in the Scan Conversion Control Register (SCCR) to 1. Then conversion starts. To start the converter by timers, set the SHEN bit in the SCCR register to 1 to enable timer start. Conversion starts when the timer's rising edge is detected. When conversion starts, the SCS bit in the ADSR register is set to 1. When the conversion is completed, the SCS bit is reset to 0.

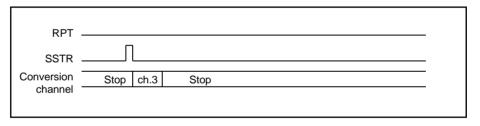
When the SSTR bit in the SCCR register is set to 1 again during A/D conversion or the timer's rising edge is detected again while timer start is enabled, the ongoing conversion operation is immediately stopped and initialized and the A/D conversion is performed again (the operation is restarted).

The available scan conversion modes are as follows:

1. One-shot mode for a single channel

This mode is selected when only one analog priority conversion is specified for scan conversion and RPT = 0 in the SCCR register. When the selected priority conversion is completed, the operation stops.

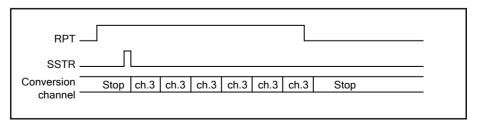
Figure 3-1 Stop of Operation in One-shot Mode for a Single Channel (SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, SCIS0 = 0x08)



2. Continuous mode for a single channel

This mode is selected when only one analog priority conversion process is specified for scan conversion and RPT = 1 in the SCCR register. When the selected priority conversion is completed, the same priority conversion is started again. To stop A/D conversion, set RPT bit to 0. The operation stops when the ongoing A/D conversion is completed.

Figure 3-2 Stop of Operation in Continuous Mode for a Single Channel (SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, SCIS0 = 0x08)

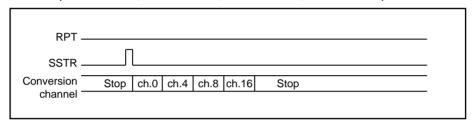




3. One-shot mode for multiple channels

This mode is selected when multiple analog channels are specified for scan conversion and RPT = 0 in the SCCR register. When the conversion starts, the existence of each channel is automatically checked. While the channels are switched from one to another, A/D conversion is started and the conversion result is written to the FIFO when the conversion is completed. The conversion channels are selected in descending order of channel number (starting from ch.0). Channels not selected in the SCIS register are skipped and the conversion operation targets the next selected channel. When the A/D conversion of the last one of the selected channels is completed, the A/D conversion is stopped.

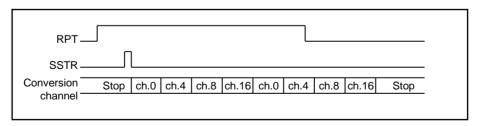
Figure 3-3 Stop of Operation in One-shot Mode for Multiple Channels (SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)



4. Continuous mode for multiple channels

This mode is selected when multiple analog channels are specified for scan conversion and RPT = 1 in the SCCR register. When the conversion starts, the existence of each channel is automatically checked. While the channels are switched from one to another, A/D conversion is started and the conversion result is written to FIFO when the conversion is completed. The conversion channels are selected in descending order of channel number (starting from ch.0). Channels not selected in the SCIS register are skipped and the conversion operation targets the next selected channel. When the A/D conversion of the last one of the selected channels is completed, the conversion operation starts again from ch.0. To end A/D conversion, clear the RPT bit to 0. The operation stops when the A/D conversion of the last one of the selected channels is completed.

Figure 3-4 Stop of Operation in Continuous Mode for Multiple Channels (SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)





3.2.2 Priority Conversion Operation

This section explains the priority conversion operation.

This mode is used to give priority to a specific conversion process. Even when scan conversion is in progress, if priority conversion is started, the scan conversion is interrupted immediately and the priority conversion is performed. When the priority conversion is completed, the scan operation restarts from the channel where it was interrupted. If conversion with higher priority (priority level 1) is started while the conversion with lower priority (priority level 2) is performed, the priority level 2 conversion is interrupted immediately and the priority level 1 conversion is performed. When the priority level 1 conversion is completed, the priority level 2 conversion is restarted.

Two levels of priority are given to priority conversion. Priority level 1 is the highest and priority level 2 is the second. Trigger start by an external pin is assigned as the start factor at priority level 1 and software/timer start is assigned as that at priority level 2.

- The input channels are selected in the Priority Conversion Input Selection register (PCIS).

The procedure for selecting channels at priority level 1 differs depending on the ESCE bit in the Priority Conversion Control register (PCCR).

When ESCE = 0: The P1A[2:0] bits in the PCIS register are used. Only one of the eight channels, ch.0 to ch.7, can be selected.

When ESCE = 1: The setting of the P1A[2:0] bits in the PCIS register is ignored. Only one of the eight channels, ch.0 to ch.7, can be selected with input from the external pin (ECS[2:0]).

Example: ECS[2:0] = 000 -> ch.0 = 010 -> ch.2 = 111 -> ch.7

The P2A[4:0] bits in the PCIS register are used for selecting the channel at priority level 2. Only one
of the multiple input channels can be selected.

The start factor of A/D conversion differs depending on the priority level.

- Priority level 1 (highest priority) conversion can be started by a falling edge of external trigger input.
 To enable external trigger start, set the PEEN bit in the PCCR register to 1.
- Priority level 2 conversion can be started by software or a timer.

To start conversion by software, set the PSTR bit in the PCCR register to 1. To start conversion by a timer, set the PHEN bit in the PCCR register to 1 to enable timer start. Conversion starts when the timer's rising edge is detected. When conversion starts, the PCS bit in the ADSR register is set to 1. When the conversion is completed, the PCS bit is reset to 0.

In priority conversion mode, the conversion cannot be restarted. In addition, start factors at the same priority level are ignored.

(A timer start factor is ignored during software-started operation.)

If a priority level 1 start factor (external trigger) occurs during conversion started by a priority level 2 start factor (software or timer), the PCNS bit in the A/D Status register (ADSR) is set to 1 and the priority level 2 conversion is interrupted immediately. When the priority level 1 conversion is completed, PCNS is reset to 0 and the interrupted priority level 2 conversion is restarted. If a priority level 2 start factor occurs during priority level 1 conversion, the priority level 2 start factor is reserved (retained) and PCNS bit is set to 1. When the priority level 1 conversion is completed, PCNS bit is reset to 0 and the priority level 2 conversion is started.

Priority conversion can only be performed in one-shot mode for a single channel.



3.2.3 Priority Levels and State Transitions

This section explains priority levels and state transitions.

Priority Levels

Table 3-1 Priority Levels for the A/D Converter

Priority level	Conversion type	Start factor
1	Priority level 1 conversion	- Input from external trigger pin (at falling edge)
		- Software (when the priority conversion start bit (PSTR) of priority
2	Priority level 2 conversion	conversion control register (PCCR) is set to 1)
		- Trigger input from timer (at rising edge)
		- Software (when the scan conversion start bit (SSTR) of scan
3	Scan conversion	conversion control register (SCCR)is set to 1)
		- Trigger input from timer (at rising edge)

■ When a startup by priority conversion occurs during scan conversion

The scan conversion operation is interrupted and priority conversion operation is performed. When the priority conversion operation is completed, the scan conversion is restarted from the channel where it was interrupted.

- When a startup at priority level 1 occurs during conversion at priority level 2

 The priority level 2 conversion is interrupted and the operation by the startup at priority level 1 is performed. When the priority level 1 operation is completed, the priority level 2 conversion is restarted automatically.
- When a startup at priority level 2 occurs during conversion at priority level 1

 The start factor at priority level 2 is retained. When the priority level 1 conversion is completed, the priority level 2 conversion is started automatically.
- When a startup of scan conversion occurs during priority level 1 conversion

 The start factor of the scan conversion is retained. When the priority level 1 conversion is completed, the scan conversion operation is started automatically.
- When a startup of scan conversion occurs during priority level 2 conversion

 The start factor of the scan conversion is retained. When the priority level 2 conversion is completed, the scan conversion operation is started automatically.
- While priority conversion is performed, start factor at the same priority level are masked (the operation is not restarted).



State Transitions

000 Standby for A/D conversion Priority conversion Scan conversion request request Scan conversion Priority conversion 001 010 completed completed Scan conversion Priority conversion is in progress. is in progress. Priority conversion Scan conversion request request Priority conversion 011 Priority conversion is in Priority level 1 Priority completed progress. conversion conversion Scan conversion is completed request pending. Priority level 1 Priority 110 Priority level 1 conversion is in conversion conversion progress. completed request Priority level 2 conversion is pending. Scan conversion Priority level 1 conversion is in request progress.

Priority level 2 conversion is pending Scan conversion is pending.

Figure 3-5 12-bit A/D Converter State Transitions

The operation states can be read from the PCNS, PCS, and SCS bits of the ADSR register.

Table 3-2 Correspondence between Bits and Operation States

PCNS	PCS	scs	Explanation of states
0	0	0	Standby for A/D conversion.
0	0	1	Scan A/D conversion is in progress.
0	1	0	Priority A/D conversion (priority level 1 or 2) is in progress.
0	1	1	Priority A/D conversion (priority level 1 or 2) is in progress. Scan conversion is
			pending.
1	1	0	Priority A/D conversion (priority level 1) is in progress. Priority conversion (priority
			level 2) is pending.
1	1	1	Priority A/D conversion (priority level 1) is in progress. Scan conversion and priority
			conversion (priority level 2) are pending.



3.3 FIFO Operations

The A/D converter has 16 FIFO stages for scan conversion and 4 FIFO stages for priority conversion. When conversion data is written in the specified count of FIFO stages, an interrupt is generated to the CPU.

- 3.3.1. FIFO Operations in Scan Conversion
- 3.3.2. Interrupts in Scan Conversion
- 3.3.3. FIFO Operations in Priority Conversion
- 3.3.4. Interrupts in Priority Conversion
- 3.3.5. Validity of FIFO Data
- 3.3.6. Bit placement Selection for FIFO Data Registers



3.3.1 FIFO Operations in Scan Conversion

This section explains FIFO operations in scan conversion.

Sixteen FIFO stages are incorporated for writing scan conversion data. After reset, they are in empty state and the SEMP bit in the Scan Conversion Control Register (SCCR) is set to 1. When A/D conversion of one channel is completed, the conversion result, start factor, and conversion channel are written in the first FIFO stage. This resets SEMP bit to 0. The conversion result, start factor, and conversion channel for the next channel are written sequentially in the second FIFO stage.

When such data is written in all of the 16 stages, the SFUL bit is set to 1 to indicate that FIFO is in full state. If conversion is performed and an attempt is made to write data in FIFO when FIFO is in full state, the SOVR bit is set to 1 and the data is discarded (cannot overwrite the existing data).

To clear the data in FIFO, set the SFCLR bit in the Scan Conversion Control register to 1. FIFO goes to the empty state and the SEMP bit is set to 1.

Data in FIFO can be read sequentially by reading the Scan Conversion FIFO Data Register (SCFD). To perform a byte (8 bits) access to this register, read the most significant byte (bit31:24) to shift FIFO (reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO). To perform a half word (16 bits) access to this register, read the most significant half word (bit31:16) to shift FIFO (reading the other byte (bit15:0) does not shift FIFO). Performing a word (32 bits) access to this register shifts FIFO.



3.3.2 Interrupts in Scan Conversion

This section explains interrupts in scan conversion.

Valid FIFO stage count N=5(6stages) FIFO stage count setting N=3(4stages) Flag clear Flag clear FIFO interrupt request FIFO readout A/D conversion Stop Stop Stop Stop

Figure 3-6 FIFO Interrupt Settings and FIFO Operations

When conversion data for the number of FIFO stages (N + 1) set in SFS[3:0] in the Scan Conversion FIFO Stage Count Setup Register (SFNS) is written in the FIFO, the interrupt request bit (SCIF) in the A/D Control Register (ADCR) is set to 1. If the interrupt enable bit (SCIE) is set to 1, an interrupt request is generated to the CPU.

The following explains FIFO stage count interrupt methods for each scan conversion mode.

1. One-shot mode for a single channel

To generate an interrupt after the completion of one conversion process for the specified channel, set SFS[3:0] = 0x0. When conversion data is written in the first FIFO stage, SCIF bit is set to 1.

Note:

 If SFS[3:0] bits are set to 0x1 or more (two stages or more), interrupts are not generated until conversion data is written into FIFO by the specified stage count.

2. Continuous mode for a single channel

To generate an interrupt after the completion of one conversion process for the specified channel, set SFS[3:0] = 0x0. When conversion data is written in the first FIFO stage, SCIF bit is set to 1. To generate an interrupt at the completion of a number of times of conversion of the specified channel, set SFS[3:0] bits to 0x1 or more (two stages or more). For example, set SFS[3:0] = 0x3 to generate an interrupt after four repeats.



3. One-shot mode for multiple channels

To generate an interrupt after the completion of conversion of the multiple specified channels, set the FIFO stage count according to the number of channels. If eight channels are selected, set the FIFO stage count by setting SFS[3:0] = 0x7. When the conversion of the last one of the selected channels is completed, SCIF bit is set to 1.

An interrupt can be generated at any timing before scan completion by setting SFS[3:0] bits to a value less than the number of selected channels.

4. Continuous mode for multiple channels

To generate an interrupt after the completion of the first scan of the multiple specified channels, set the FIFO stage count according to the number of channels. If eight channels are selected, set the FIFO stage count by setting SFS[3:0] = 0x7. When the conversion of the last one of the selected channels is completed, SCIF bit is set to 1.

To generate an interrupt after the completion of the second scan, set the FIFO stage count to twice the number of selected channels. For example, when four channels are selected, set the FIFO stage count to 8 (SFS[3:0] = 0x7). An interrupt is generated when the second scan is completed.

Because the FIFO stage count can be set to any value, an interrupt can be generated at any desired timing.



3.3.3 FIFO Operations in Priority Conversion

This section explains FIFO operations in priority conversion.

Four FIFO stages are incorporated for writing priority conversion data. After reset, they are in empty state and the PEMP bit in the Priority Conversion Control Register is set to 1. When one A/D conversion process is completed, the conversion result, start factor, and conversion channels are written in the first FIFO stage. This resets SEMP bit to 0. The conversion result and conversion channels for the subsequent conversion processes are written in the corresponding FIFO stages.

When such data is written in all of the 4 stages, the PFUL bit is set to 1 to indicate that FIFO is in full state. If conversion is performed and an attempt is made to write data in FIFO when FIFO is in full state, the POVR bit is set to 1 and the data is discarded (cannot overwrite the existing data).

To clear the data in FIFO, set the PFCLR bit in the Priority Conversion Control Register (PCCR) to "1". FIFO goes to the empty state and the PEMP bit is set to 1.

Data in FIFO can be read sequentially by reading the Priority Conversion FIFO Data Register (PCFD). To perform byte (8 bits) access to this register, read the most significant byte (bit31:24) to shift FIFO (reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO). To perform a half word (16 bits) access to this register, read the most significant half word (bit31:16) to shift FIFO (reading the other byte (bit15:0) does not shift FIFO). Performing a word (32 bits) access to this register shifts FIFO.



3.3.4 Interrupts in Priority Conversion

This section explains interrupts in priority conversion.

When conversion data for the number of FIFO stages (N + 1) set in PFS[1:0] in the Priority Conversion FIFO Stage Count Setup register (PFNS) is written in FIFO, the interrupt request bit (PCIF) in the A/D Control register (ADCR) is set to 1. If the interrupt enable bit (PCIE) is set to "1", an interrupt request is generated to the CPU.

The following explains FIFO stage count interrupt methods in priority conversion.

To generate an interrupt after the completion of one conversion process for the specified channel, set PFS[1:0] = 0x0. When conversion data is written in the first FIFO stage, PCIF bit is set to 1.

Note:

If PFS[1:0] bits are set to 0x1 or more (two stages or more), interrupts are not generated until
conversion data is written into FIFO by the specified stage count.



3.3.5 Validity of FIFO Data

This section explains a restriction on reading FIFO data registers.

The bit12 of the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) comes with the INVL (A/D conversion result disable) bit which indicates data validity. During reading FIFO data registers, the INVL bit is cleared to 0 if data is valid while the INVL bit is set to 1 if data is invalid.

For word (32 bits) reading, data validity can be checked by the INVL bit.

For half word (16 bits) reading which does not use interrupts or empty bits (SEMP, PEMP), always start reading from the least significant 16 bits including the INVL bit. If the INVL bit is 1 at this time, reading the most significant 16 bits is prohibited. The most significant 16 bits must be read only when the INVL bit is 0.

For byte (8 bits) reading which does not use interrupts or empty bits (SEMP, PEMP), always start reading from bit15:8 including the INVL bit. If the INVL bit is 1 at this time, reading bit31:24, bit23:16, or bit7:0 is prohibited. They must be read only when the INVL bit is 0.



3.3.6 Bit placement Selection for FIFO Data Registers

This section explains bit placement selection for FIFO data registers.

The A/D converter can change the bit placement for the conversion results in the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data register (PCFD) with the FDAS bit in the A/D Status Register (ADSR) (Figure 3-7).

Setting the FDAS bit to 1 places 12-bit A/D conversion results (SD11 to SD0, PD11 to PD0) on the LSB side (bit27:16) when a FIFO data register is read. Placement of the least significant 16 bits of a FIFO data register does not change.

FIFO is shifted, regardless of the set value of the FDAS bit, by reading bit31:24 (for a byte access), bit31:16 (for a half word access), or bit31:0 (for a word access) of a FIFO data register.

SCFD register When FDAS=0 29 28 27 26 25 23 22 20 19 17 31 30 24 21 18 16 SD8 SD7 SD4 SD2 SD1 SD0 SD10 SD9 SD6 SD5 SD3 SD11 Reserved When FDAS=1 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 0 0 SD11 SD9 SD8 SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0 0 0 SD10 PCFD register When FDAS=0 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 PD10 PD9 PD8 PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0 Reserved When FDAS=1 27 31 30 29 `28 26 25 24 23 22 21 20 19 18 17 16 PD11 PD10 PD9 PD8 PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0

Figure 3-7 FIFO Data Register Bit Placement



3.4 A/D Comparison Function

The A/D comparison function compares A/D conversion results and generates interrupts.

To use the comparison function, set the CMPEN bit in the A/D Comparison Control Register (bit7 in the CMPCR register) to 1.

The values set in the A/D Comparison Value Setup Register (CMPD) are compared with the most significant 10 bits (bit11:2) of the A/D conversion result. If the comparison result satisfies the conditions set in the A/D Comparison Control Register (CMPCR), the A/D comparison interrupt bit (CMPIF) in the ADCR register is set to 1. If the interrupt enable bit (CMPIE) is 1, an interrupt is generated to the CPU.

Note:

Two bits (bit1:0) on the LSB side are not compared.

Because the result of A/D conversion, regardless of scan or priority, is compared before it is written to FIFO, comparison is possible when FIFO is full.

If CMD1 bit is set to 1 (to generate an interrupt when the result is equal to or more than the CMPD set value), CMPIF is set to 1 when the conversion result is equal to the value in the A/D Comparison Value Setup Register (CMPD).



3.5 Range Comparison Function

The range comparison function is a function to determine whether the conversion result of the A/D converter is within or outside the specified range and generate an interrupt.

To start the range comparison function, write 1 to the range comparison enabling setting (RCOE) of Range Comparison Control register (WCMPCR).

The upper 10 bits (bit11:2) of the A/D conversion result is compared with the upper threshold setting register (WCMPDH) and the lower threshold setting register (WCMPDL).

Note:

The comparison with two bits (bit1, bit0) on the LSB side is not executed.

When the within-range /outside-range confirmation select (RCOIRS) of Range Comparison Control Register is 1, the A/D conversion result is confirmed to be outside of the specified range.

Table 3-3 shows the detection conditions of the range comparison and Figure 3-8 shows the operation of the range comparison.

Table 3-3 Range Comparison Conditions

Range Comparison Result	Outside-Range Confirmation (RCOIRS="0")	Within-Range Confirmation (RCOIRS="1")	Remarks
Outside range (beyond upper limit threshold)	Detected	Not detected	Figure 3-8 : 2.6
A/D data bit > upper limit threshold setting register			g 0 . =,0
Within Range			
A/D data bit ≥ lower limit threshold setting register	Not detected	Detected	Figure 3-8 : 1,4,5
And,	Not detected	Delected	1 iguic 5 6 : 1,4,5
A/D data bit ≤ upper limit threshold setting register			
Outside range (below lower limit threshold)	Detected	Not detected	Figure 2.9 . 2
A/D data bit < lower limit threshold setting register	Detected	Not detected	Figure 3-8 : 3



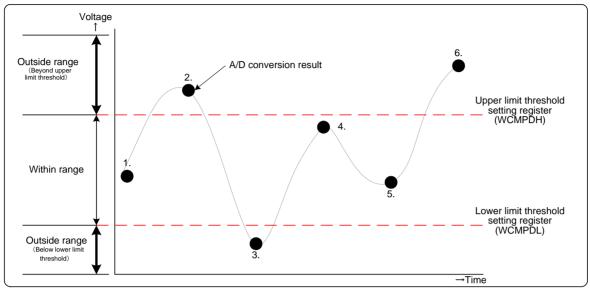


Figure 3-8 Range Comparison Operation

The Continuous detection function detects the range comparison continuously, and removes the noise etc. When the range comparison is continuously detected for the times specified in continuous detection count specification and state setting (RCOCD) of the range comparison control register (WCMPCR), the range comparison flag register (RCINT) is set to 1. When the range comparison interrupt enable bit (RCOIE) is set to "1", the interrupt is generated for CPU.

When the range comparison result is found to be undetected even one time in the continuous detection, the continuous detection measurement is cleared to 0 times, and restarts the measurement. For the continuous detection conditions, see Table 3-4.

Items **Descriptions** The detection is always operated whenever the continuous comparison execution Continuous detection measurement operation enable setting (RCOE) is set to "1". With the continuous detection count specification (RCOCD), the detection count can be selected from 1 to 7 times. Continuous detection count With the continuous detection count status display (RCOCD), the state of the detection count can be confirmed. When the range comparison execution enable setting (RCOE) is set to "0". Clear conditions When the result is undetected with the range comparison result. When the result is detected with the range comparison result. However, when the detection count reaches the continuous detection count Increment condition specification (RCOCD), the detection is stopped at the continuous detection count specification value

Table 3-4 Continuous Detection Conditions

Note:

 When the confirmation of outside-range (WCMPCR.RCOIRS) is 0, the continuous detection measurement is not cleared to 0 times, and continues the continuous detection even if the range comparison result is changed from the state of the upper limit threshold excess to the state of below lower limit threshold.

To initialize the state of the continuous detection count of the range comparison result, disable the range comparison while A/D conversion is not required, and then enable the range comparison again.



When the confirmation of outside-range of the range comparison (RCOIRS) is "0", the state of the upper limit threshold excess or the state of below lower limit threshold can be confirmed with the range comparison threshold excess flag bit (RCOOF).

For the judgment conditions of the Range Comparison Threshold Excess Flag, see Table 3-5.

Table 3-5 Range Comparison Threshold Excess Flag, Judgment Conditions

	Range Comparison Thresh	old Excess Flag Bit(RCOOF)	
Range Comparison Result	Outside-range confirmed	Within-range confirmed	
	(RCOIRS="0")	(RCOIRS="1")	
Outside range (beyond upper limit threshold)	"4"	Prior value held	
A/D data bit > upper limit threshold setting register	l	Prior value nelo	
Within Range			
A/D data bit ≥ lower limit threshold setting register	Prior value held	Prior value held	
And,	Prior value neid	Phor value neid	
A/D data bit ≤ upper limit threshold setting register			
Outside range (below lower limit threshold)	"0"	Drier value held	
A/D data bit < lower limit threshold setting register	U"	Prior value held	

Moreover, the range comparison threshold excess flag bit (RCOOF) holds the content set in itself while the comparison interrupt factor flag (RCINT) is set to 1.

For the operation example of the range comparison function, see Figure 3-9.

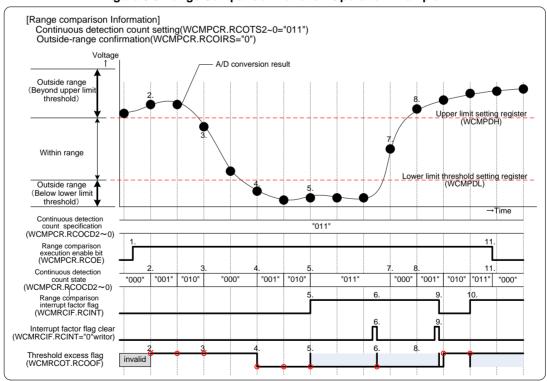


Figure 3-9 Range Comparison Function Operation Example



The explanation of range comparison function operation in Figure 3-9 is as follows:

- 1. When the range comparison execution disable setting (RCOE) is 0, the continuous detection count state (RCOCD) is initialized to 000.
 - When the range comparison execution disable setting (RCOE) is set to 1, the range comparison operation is started.
- 2. When the range comparison result exceeds the upper limit threshold, the continuous count detection state (RCOCD) begins to increment.
 - Moreover, the threshold excess flag notifies the upper limit threshold excess (RCOOF=1).
- 3. Before the continuous detection count specification value (RCOCD) becomes 011, the range comparison result is found to be within the range. So, the continuous detection count state (RCOCD) is initialized to be 000.
 - Furthermore, the threshold excess flag (RCOOF) holds the prior value.
- 4. Because the range comparison result is below the lower limit threshold, the continuous count detection state (RCOCD) executes the increment.
 - And, the threshold excess flag notifies that the result is below the lower limit threshold (RCOOF=0).
- 5. As the range comparison result reaches continuously the continuous detection count specification value (RCOCD =011), the range comparison interrupt factor flag (RCINT) is set to be 1. Moreover, the threshold excess flag (RCOOF) sets the threshold excess state where the range comparison interrupt factor flag is set (RCINT=1) and holds the state until the range comparison interrupt factor flag is cleared (RCINT=0).
- 6. The set operation by the state of the continuous detection is given priority when the state of the range comparison interrupt factor flag clear (RCINT=0) and the state of the continuous detection compete. The range comparison interrupt factor flag is set (RCINT=1) and the threshold excess flag (RCOOF) set to the threshold excess state again.
- When the range comparison result is within the range, even in the state of the range comparison interrupt factor flag set (RCINT=1), the state of the continuous detection frequency is initialized (RCOCD =000).
- 8. Even in the range comparison interrupt factor flag set state (RCINT=1), the range comparison result increments the continuous count detection (RCOCD2) by the upper limit threshold excess. However, in the range comparison interruption factor flag set state (RCINT=1), the threshold excess flag (RCOOF) holds the prior value.
- The range comparison interrupt factor flag is cleared (RCINT=0) because of the range comparison interrupt factor flag clear (RCINT=0).
 - Moreover, the hold state of the limit excess flag (RCOOF) is also released.
- 10. Because the range comparison result continuously reached the continuous detection count specification value (RCOCD =011), the range comparison interrupt factor flag (RCINT) is set to 1. Moreover, the threshold excess flag (RCOOF) is set to the threshold excess state when the range comparison interrupt factor flag is set (RCINT=1) and its state is held until the range comparison interrupt factor flag is cleared (RCINT=0).
- 11. When the range comparison operation is disabled (RCOE=0), the continuous detection count state (RCOCD) is initialized to 000.
 - Moreover, neither the range comparison interrupt factor flag (RCINT) nor the threshold excess flag (RCOOF) are cleared because the range comparison operation is disabled (RCOE=0).

However, because the range comparisons of the A/D conversion results are implemented before A/D conversion result is written to FIFO regardless of the scanning conversion and the priority conversion, the range comparison can be executed even when FIFO is in the FULL state.



3.6 Starting DMA

This section explains the DMA transfer processing for FIFO data of A/D converter.

Data stored in the FIFO of the A/D converter can be transferred with the hardware activated DMA transfer using interrupt signals. The required settings and operations are as follows.

This product is compatible with DMA transfers of scan convert FIFO data by DMAC, and scan convert FIFO data and prior convert FIFO data by DSTC.

- The interrupt signal from the A/D converter is connected to the interrupt controller in the initial state. According to the select register setting for DMA transfer requests of interrupt controller and the DREQENB register setting of DSTC, connect the scan convert interrupt signal and prior convert interrupt signal to DMAC/DSTC. Enables interrupts from the A/D converter. (ADCR:SCIE=1, ADCR:PCIE=1)
- Set 0 for the FIFO stage count when the interrupts from the A/D converter are generated (the interrupt request will be generated when the conversion result is stored in the first FIFO stage).
- For DMAC/DSTC side, specify the transfer source addresses for the scan convert FIFO data register (SCFD) and prior conversion FIFO data register (PCFD). In case of DMAC, select the hardware demand transfer for transfer mode. In case of DSTC, select DES0.MODE=1 for transfer mode. For number of transfer, specify the number of data stored in FIFO.

Figure 3-10 shows a timing chart of DMA transfer operations.

After A/D conversion is started, the converted data will be stored in FIFO. Interrupt requests from the A/D converter are generated. By DMAC/DSTC, reading the FIFO data register and writing to the destination are performed, and data transfer is performed. The generated interrupt signals are cleared from the DMAC/DSTC side. (▼mark in this figure) Clearing the interrupt flag (ADCR:SCIF, ADCR:PCIF) from CPU is not required. After transfer operation is completed for the times specified in DMAC/DSTC, the transfer completion notification from DMAC/DSTC can be received.

If DMAC/DSTC processes transfer requests other than those of the A/D converter, note that the start of DMA transfer may get delayed as shown from ∇ to \triangle in the figure.

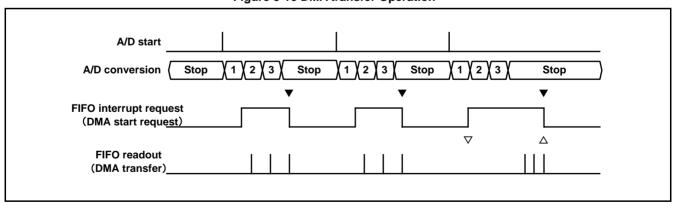


Figure 3-10 DMA transfer Operation



4. Setup procedure Examples

This section provides examples of setup procedures for the 12-bit A/D converter.

- 4.1. A/D Operation Enable Setup Procedure Example
- 4.2. Scan Conversion Setup Procedure Example
- 4.3. Priority Conversion Setup Procedure Example
- 4.4. Range Comparison Function Setting Example
- 4.5. Setting Conversion Time

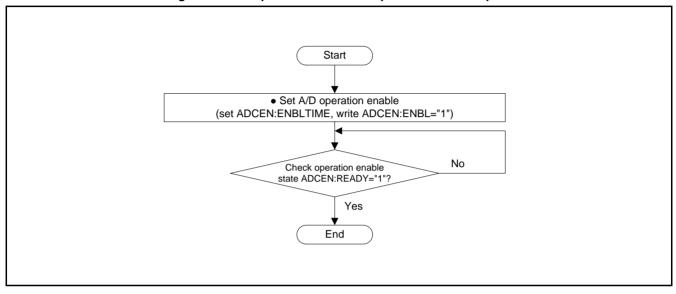


4.1 A/D Operation Enable Setup Procedure Example

This section provides an A/D operation enable setup procedure example.

- Set the period of operation enable state transitions
- Poll the operation enable state

Figure 4-1 A/D Operation Enable Setup Procedure Example



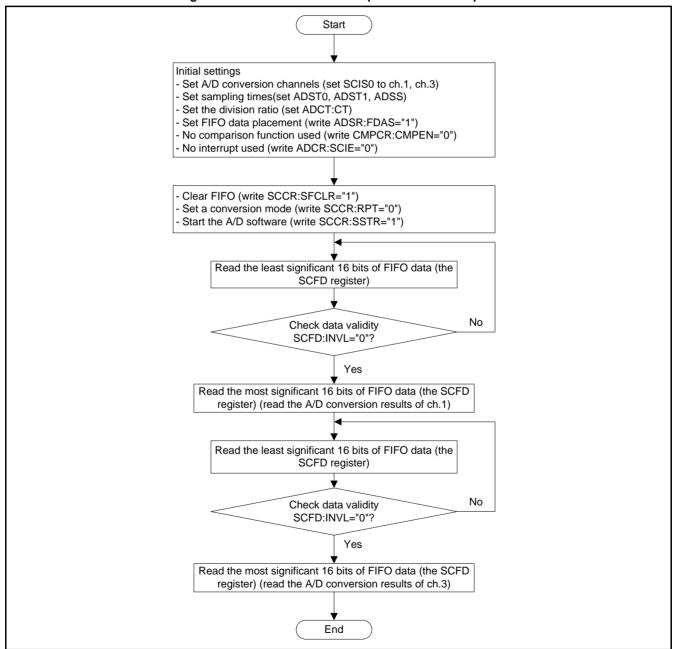


4.2 Scan Conversion Setup Procedure Example

This section provides a scan conversion setup procedure example.

- Scan conversion by software startup
- Set A/D conversion channels to ch.1 and ch.3
- Set different sampling times for ch.1 and ch.3
- Set the clock division ratio
- Read the least significant 16 bits of FIFO data and check data validity by the INVL bit
- After checking that data is valid, read the most significant 16 bits of FIFO data

Figure 4-2 Scan Conversion Setup Procedure Example



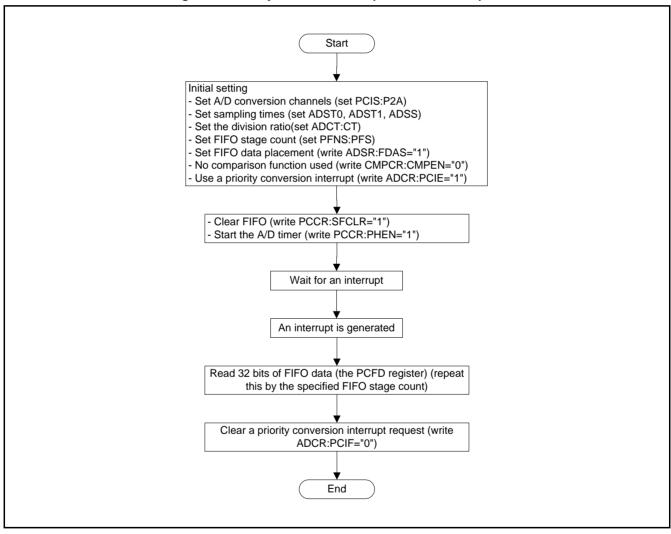


4.3 Priority Conversion Setup Procedure Example

This section provides a priority conversion setup procedure example.

- Priority conversion at priority level 2 by timer start
- Conversion channels are ch.1 and ch.3
- Set different sampling times for ch.1 and ch.3
- Set the clock division ratio
- Read 32 bits of FIFO data by using an interrupt
- Read FIFO by the specified stage count

Figure 4-3 Priority Conversion Setup Procedure Example

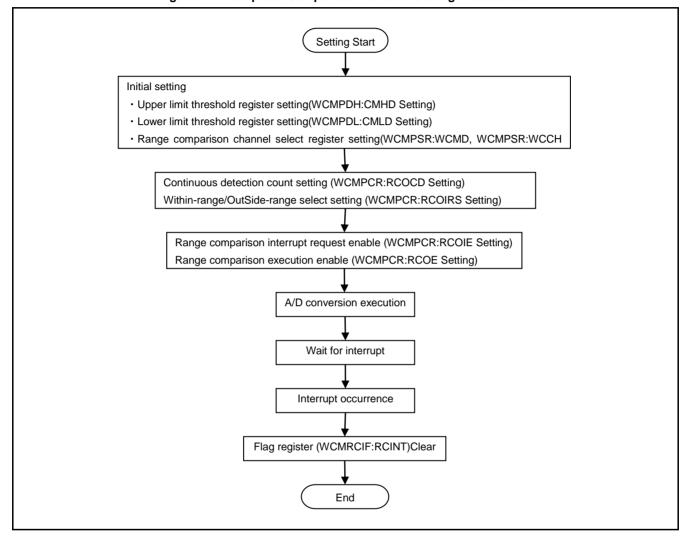




4.4 Range Comparison Function Setting Example

This section shows the example of range comparison function setting procedures.

Figure 4-4 Example of Comparison Function Setting Procedures





4.5 Setting Conversion Time

The conversion time of the A/D converter is "sampling time" + "comparison time". Two sampling time settings can be applied to each channel. This section explains how to set and calculate the conversion time.

Example of Setting the Sampling Time

A sampling time is set in each of Sampling Time Setup registers 0 and 1 (ADST0 and ADST1). Using Sampling Time Selection Registers (ADSS3 to ADSS0), whether Sampling Time Setup Registers 0 or 1 is used to provide the value can be selected for each channel. This allows you to set different sampling times for channels with different external impedances.

Sampling time = Base clock (HCLK) cyclex Clock division ratio \times {(ST set value + 1) \times STX setting multiplier + 3}

Notes:

- For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.
- When STXx2, STXx1, and STXx0 = 000 (STx4 to STx0 set values multiplied by 1) are set, set STx4 to STx0 to "2" or more ("1" or less must not be set).

Example of Setting the Comparison Time

The comparison time is set in the Comparison Time Setup register (ADCT).

Comparison time = Compare clock cycle x 14

Compare clock cycle = Base clock (HCLK) cycle x Clock division ratio

Notes:

- For setting the compare clock cycle, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.
- If the sampling time or compare clock cycle fails to meet the electrical characteristics of the A/D converter, the A/D conversion accuracy may be degraded.



Example of Conversion Time Calculation (when HCLK = 20 MHz (50 ns cycle))

(1) Sampling time

- When ST04 to ST00 = 2, STX02, STX01, and STX00 = 000 (multiplied by 1), and CT7 to CT0=0 (Compare clock division ratio: 2)
- Sampling time = $50 \text{ ns} \times 2 \times \{(2+1) \times 1 + 3\} = 600 \text{ ns}$ When ST14 to ST10 = 19, STX12, STX11, and STX10 = 001 (multiplied by 4), and CT7 to CT0=0 (Compare clock division ratio: 2) Sampling time = $50 \text{ ns} \times 2 \times \{(19 + 1) \times 4 + 3\} = 8300 \text{ ns}$

(2) Comparison time

When CT7 to CT0 = 0 (Clock division ratio: 2)
 Compare clock cycle = 50 ns x 2 = 100 ns
 Comparison time = 100 ns x 14 = 1400 ns

(3) Conversion time

- By adding (1) and (2) together:

Conversion time for channels specified with the ADST0 register = 2000 ns Conversion time for channels specified with the ADST1 register = 9700 ns

Example of setting register

Table 4-1 Example of Setting Register for Sampling Time and Compare Time

HCLK	CT7~	STXx2~	STx4~	Sampling	Comparis	Conversi	Compare
	СТ0	STXx0	STx0	Time	on Time	on Time	Clock Cycle
40 MHz	10000000	000	00010	0.15 μs	0.35 µs	0.50 µs	25 ns
40 MHz	00000000	000	00010	0.30 µs	0.70 µs	1.00 µs	50 ns
40 MHz	00000000	000	00011	0.35 µs	0.70 µs	1.05 µs	50 ns
40 MHz	00000000	001	00010	0.75 μs	0.70 µs	1.45 µs	50 ns
40 MHz	00000001	000	00010	0.45 µs	1.05 µs	1.50 µs	50 ns
72 MHz	00000000	000	00010	0.17 µs	0.39 µs	0.56 µs	27.8 ns
72 MHz	00000010	000	00010	0.33 µs	0.78 µs	1.11 µs	55.6 ns
80 MHz	00000000	000	00010	0.15 µs	0.35 µs	0.50 µs	25 ns
80 MHz	00000010	000	00010	0.30 µs	0.70 µs	1.00 µs	50 ns
160 MHz	00000010	000	00010	0.15 µs	0.35 µs	0.50 µs	25 ns
160 MHz	00000110	000	00010	0.30 µs	0.70 µs	1.00 µs	50 ns
180 MHz	00000011	000	00010	0.17 µs	0.39 µs	0.56 µs	27.8 ns
180 MHz	00000111	000	00010	0.30 µs	0.70 µs	1.00 µs	50 ns
200 MHz	00000011	000	00010	0.15 µs	0.35 µs	0.50 µs	25 ns
200 MHz	00001000	000	00010	0.30 µs	0.70 µs	1.00 µs	50 ns



5. Registers

This section explains the configuration and functions of the registers used for the 12-bit A/D converter.

Table 5-1 List of Registers for the 12-bit A/D Converter

Abbreviation	Register name	Reference
ADCR	A/D Control register	5.1
ADSR	A/D Status register	5.2
SCCR	Scan Conversion Control register	5.3
SFNS	Scan Conversion FIFO Stage Count Setup register	5.4
SCFD	Scan Conversion FIFO Data register	5.5
SCIS	Scan Conversion Input Selection register	5.6
PCCR	Priority Conversion Control register	5.7
PFNS	Priority Conversion FIFO Stage Count Setup register	5.8
PCFD	Priority Conversion FIFO Data register	5.9
PCIS	Priority Conversion Input Selection register	5.10
CMPD	A/D Comparison Value Setup register	5.11
CMPCR	A/D Comparison Control register	5.12
ADSS	Sampling Time Selection register	5.13
ADST	Sampling Time Setup register	5.14
ADCT	Comparison Time Setup register	5.15
ADCEN	A/D Operation Enable Setup register	5.16
WCMPDH	Upper Limit Threshold Setting register	5.17
WCMPCR	Range Comparison Control register	5.18
WCMPDL	Lower Limit Threshold Setting register	5.19
WCMPSR	Range Comparison Channel Select register	5.20
WCMRCOT	Range Comparison Threshold Excess Flag register	5.21
WCMRCIF	Range Comparison Flag register	5.22



5.1 A/D Control Register (ADCR)

The A/D Control register (ADCR) performs interrupt flag display and interrupt enable control.

bit	15	14	13	12	11	10	9	8
Field	SCIF	PCIF	CMPIF	Reserved	SCIE	PCIE	CMPIE	OVRIE
Attribute	R/W	R/W	R/W	=	R/W	R/W	R/W	R/W
Initial value	0	0	0	X	0	0	0	0

[bit15] SCIF: Scan conversion interrupt request bit

When conversion values are written up to the stage count specified in the Scan Conversion FIFO Stage Count Setup register (SFNS), this bit is set to 1. The read value of Read-Modify-Write operation is 1 regardless of the bit value.

bit	Descr	Description		
Dit	Read	Write		
0	Conversion result is not stored.	Clears this bit.		
1	Conversion result is stored.	No effect.		

[bit14] PCIF: Priority conversion interrupt request bit

When conversion values are written up to the stage specified in the Priority Conversion FIFO Stage Count Setup register (PFNS), this bit is set to 1. The read value of Read-Modify-Write operation is 1 regardless of the bit value.

hi4	bit		
Dit	Read	Write	
0	Conversion result is not stored.	Clears this bit.	
1	Conversion result is stored.	No effect.	

[bit13] CMPIF: Conversion result comparison interrupt request bit

When the condition set in the A/D Comparison Value Setup register (CMPD) or A/D Comparison Control register (CMPCR) is satisfied during the operation of the A/D conversion result comparison function, this bit is set to 1. The read value of Read-Modify-Write operation is 1 regardless of the bit value.

bit	Description			
Dit	Read	Write		
0	Specified condition is not satisfied.	Clears this bit.		
1	Specified condition is satisfied.	No effect.		

[bit12] Reserved: Reserved bit

Writing has no effect on operation.

The read value is undefined.



[bit11] SCIE: Scan conversion interrupt enable bit

This bit controls the interrupt request of SCIF. When the SCIE bit is enabled, and the SCIF bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

[bit10] PCIE: Priority conversion interrupt enable bit

This bit controls the interrupt request of PCIF. When the PCIE bit is enabled, and the PCIF bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

[bit9] CMPIE: Conversion result comparison interrupt enable bit

This bit controls the interrupt request of CMPIF. When the CMPIE bit is enabled and the CMPIF bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

[bit8] OVRIE: FIFO overrun interrupt enable bit

This bit controls the interrupt request of the SOVR bit in the SCCR register or the POVR bit in the PCCR register. When the OVRIE bit is enabled, and the SOVR or POVR bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable



5.2 A/D Status Register (ADSR)

The A/D Status register (ADSR) displays scan and priority conversion statuses.

bit	7	6	5	4	3	2	1	0
Field	ADSTP	FDAS		Reserved		PCNS	PCS	SCS
Attribute	R/W	R/W		-		R	R	R
Initial value	0	0		XXX		0	0	0

[bit7] ADSTP: A/D conversion forced stop bit

Setting the ADSTP bit to 1 stops the A/D conversion operation forcibly (both scan and priority conversion operations are stopped). Forced stop of A/D conversion initializes the PCNS, PCS, and SCS bits in the ADSR register to 0. However, other register bits are not reset.

bit	Description			
DIL	Read	Write		
0	The value is always "0".	No effect.		
1	The value is always U.	Stops the conversion operation forcibly.		

[bit6] FDAS: FIFO data placement selection bit

Setting the FDAS bit to 1 shifts the Scan Conversion FIFO Data register (SCFD) and Priority Conversion FIFO Data register (PCFD) conversion result values by 4 bits to the LSB side, placing them in bit27:16. The position of the lower 16-bit of the FIFO data register does not change.

bit	Description
0	Places conversion result on the MSB side.
1	Places conversion result on the LSB side.

[bit5:3] Reserved: Reserved bits

Writing has no effect on operation.

The read value is undefined.

[bit2] PCNS: Priority conversion pending flag

This flag indicates that conversion at priority level 2 (software/timer) is pending. This flag is set when priority conversion at priority level 2 (software/timer) is started while priority conversion at priority level 1 (external trigger start) is performed or when conversion at priority level 1 is started while priority conversion at priority level 2 is performed. Writing is ignored.

bit	Description
0	Priority level 2 conversion is not pending.
1	Priority level 2 conversion is pending.



[bit1] PCS: Priority conversion status flag

This flag indicates that priority A/D conversion is in progress. This flag is set while priority conversion at priority level 1 or 2 is performed. Writing is ignored.

bit	Description
0	Priority conversion is stopped.
1	Priority conversion is in progress.

[bit0] SCS: Scan conversion status flag

This flag indicates that scan A/D conversion is in progress. Writing is ignored.

bit	Description
0	Scan conversion is stopped.
1	Scan conversion is in progress.



5.3 Scan Conversion Control Register (SCCR)

The Scan Conversion Control register (SCCR) controls the scan conversion mode.

bit	15	14	13	12	11	10	9	8
Field	SEMP	SFUL	SOVR	SFCLR	Reserved	RPT	SHEN	SSTR
Attribute	R	R	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	Χ	0	0	0

[bit15] SEMP: Scan conversion FIFO empty bit

This bit is set when the FIFO goes to the empty state. When conversion data is written in the Scan Conversion FIFO Data register (SCFD), this bit is set to 0. Writing is ignored.

bit	Description
0	Data remains in FIFO.
1	FIFO is empty.

[bit14] SFUL: Scan conversion FIFO full bit

This bit is set when the FIFO goes to full state. When SFCLR is set to 1 or the Scan Conversion FIFO Data register (SCFD) is read, this bit is set to 0. Writing is ignored.

bit	Description
0	Data can be input to FIFO.
1	FIFO is full.

[bit13] SOVR: Scan conversion overrun flag

This bit is set when an attempt to write data to a full FIFO is made (conversion data in a full FIFO is not overwritten). The read value of Read-Modify-Write operation is 1 regardless of the bit value. When the OVRIE bit in the ADCR register is 1 and the SOVR bit is 1, an interrupt is generated to the CPU.

bit	Description			
Dit	Read	Write		
0	No overrun has occurred.	Clears this bit.		
1	Overrun has occurred.	No effect.		

[bit12] SFCLR: Scan conversion FIFO clear bit

Setting this bit to 1 clears the scan conversion FIFO. The FIFO becomes empty and the SEMP bit is set to 1.

bit	Description			
Dit	Read	Write		
0	The value is always "0"	No effect.		
1	The value is always "0".	Clears FIFO.		



[bit11] Reserved: Reserved bit

Writing has no effect on operation.

The read value is undefined.

[bit10] RPT: Scan conversion repeat bit

Setting this bit to 1 places the converter in the repeat mode. When the conversion of all analog input channels selected in the Scan Conversion Input Selection register (SCIS) is completed, the conversion is started again.

Setting the RPT bit to 0 ends the repeat conversion. The operation stops when the conversion of the analog input channels selected in the SCIS bit is completed.

Setting the RPT bit to 1 must be performed while scan conversion is stopped (ADSR: SCS= 0). (Setting the SSTR bit to 1 may be performed simultaneously with setting the RPT bit to 1.)

bit	Description
0	Single conversion mode
1	Repeat conversion mode

Note:

The repeat transfer cannot be stooped immediately even when PRT bit is set to 0.
 Writing data to FIFO will be continued until the transfer is stopped.
 Note that FIFO data and Status bits (FIFO full bit etc.) continue to change until the transfer is stopped.

[bit9] SHEN: Scan conversion timer start enable bit

Set this bit to 1 to start scan conversion using a rising edge from a timer. Software startup (SSTR = 1) is valid even when this bit is set to 1.

bit	Description
0	Timer start disable
1	Timer start enable

[bit8] SSTR: Scan conversion start bit

Setting this bit to 1 starts A/D conversion. Setting this bit to 1 again during conversion stops the ongoing conversion immediately and restarts the conversion.

bit	Description						
Dit	Read	Write					
0		No effect.					
1	The value is always "0".	Starts conversion or restarts the conversion (during conversion).					

Note:

 If a startup by a timer occurs simultaneously with the setting of the SSTR bit to 1, the setting of the SSTR bit to 1 takes preference and the startup by the timer is ignored.



5.4 Scan Conversion FIFO Stage Count Setup Register (SFNS)

The Scan Conversion FIFO Stage Count Setup register (SFNS) sets up the generation of interrupt requests in scan conversion. When the specified count of FIFO stages store A/D conversion data, the interrupt request bit (SCIF) is set.

bit	7	6	5	4	3	2	1	0			
Field		Rese	erved			SFS	[3:0]				
Attribute		-	=		R/W						
Initial value		XX	XX		0000						

[bit7:4] Reserved: Reserved bits

Writing has no effect on operation.

The read value is undefined.

[bit3:0] SFS[3:0]: Scan conversion FIFO stage count setting bits

When A/D conversion data for the FIFO stage count (N + 1) set in SFS[3:0] bits are written, the interrupt request flag (SCIF) is set to 1.

bit3:0	Description
0000	Generates an interrupt request when conversion result is stored in the first FIFO stage.
0001	Generates an interrupt request when conversion result is stored in the second FIFO stage.
0010	Generates an interrupt request when conversion result is stored in the third FIFO stage.
1101	Generates an interrupt request when conversion result is stored in the 14th FIFO stage.
1110	Generates an interrupt request when conversion result is stored in the 15th FIFO stage.
1111	Generates an interrupt request when conversion result is stored in the 16th FIFO stage.



5.5 Scan Conversion FIFO Data Register (SCFD)

The Scan Conversion FIFO Data register (SCFD) consists of 16 FIFO stages and stores analog conversion results. Data can be retrieved sequentially by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	SD	SD	SD	SD	SD	SD	SD	SD	SD	SD	SD	SD		Rese	erved	
	11	10	9	8	7	6	5	4	3	2	1	0				
Attribute						F	3							F	₹	
Initial value		0xXXX XXXX														
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	F	Reserve	d	INV	Rese	erved	RS	RS	F	Reserve	d	SC	SC	SC	SC	SC
				L			1	0				4	3	2	1	0
Attribute		R		R	F	3	F	₹	•	R	•		•	R		
Initial value		XXX 1 XX XX XXX			XXX			XXXXX								

[bit31:20] SD11 to SD0: Scan conversion result

The result of 12-bit scan A/D conversion is written.

[bit19:13] Reserved: Reserved bits

The read value is undefined.

[bit12] INVL: A/D conversion result disable bit

This bit is set when this register value is invalid.

bit	Description						
0	This register value is valid						
1	This register value is invalid						

[bit11:10] Reserved: Reserved bits

The read value is undefined.

[bit9:8] RS1, RS0: Scan conversion start factor

The start factor of the scan conversion corresponding to this register value is shown.

bit9:8	Description
01	Software start
10	Timer start

[bit7:5] Reserved: Reserved bits

The read value is undefined.



[bit4:0] SC4 to SC0: Conversion input channel bits

The analog input channels corresponding to the conversion result written in SD11 to SD0 are written. Settings for channels not defined in the product specifications are not written. See the specified number of the analog input channels in the Data Sheet of each product.

bit4:0	Description
00000	ch.0
00001	ch.1
00010	ch.2
11101	ch.29
11110	ch.30
11111	ch.31

Notes:

- This register has different bit configurations depending on the FDAS bit setting in the A/D Status register (ADSR). When the FDAS bit is 1, see 3.3.6 Bit placement Selection for FIFO Data Registers.
- To perform a byte access to this register, read the most significant byte (bit31:24) to shift the FIFO data. Reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO. To perform a half byte access to this register, read the most significant half byte (bit 31:16) to shift the FIFO data. Reading the other byte (bit15:0) does not shift FIFO. Performing a word access to this register shifts FIFO.
- If software and a timer are started simultaneously, 0b11 may be read from the RS[1:0] bits.



5.6 Scan Conversion Input Selection Register (SCIS)

The Scan Conversion Input Selection register (SCIS) is used to select analog input channels for which scan conversion is performed. Any channels can be selected from multiple analog inputs. The selected channels are converted in ascending order of channel number.

SCIS3 (most significant byte: AN31 to AN24) and SCIS2 (least significant byte: AN23 to AN16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Field	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Attribute		R/W															
Initial value		0x00															

[bit15:0] AN31 to AN16: Analog input selection bits

When these bits are set to 1, the corresponding channels are selected for analog conversion.

SCIS1 (most significant byte: AN15 to AN8) and SCIS0 (least significant byte: AN7 to AN0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Field	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	AN	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Attribute		R/W															
Initial value		0x00															

[bit15:0] AN15 to AN0: Analog input selection bits

When these bits are set to 1, the corresponding channels are selected for analog conversion.

Notes:

- It is not allowed to change the channels during A/D conversion. Be sure to set SCIS3 to SCIS0 while the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.
- It is not possible to set 1 in the bit corresponding to a channel that is not defined in the product specifications. See the specified number of the analog input channels in the Data Sheet of each product.

Example of Scan Conversion Order

The selected channels are converted in ascending order of channel number.

Example: When the AN1, AN3, AN5, and AN23 bits are set to 1, the analog conversion proceeds from ch.1, ch.3, ch.5, and to ch.23.



5.7 Priority Conversion Control Register (PCCR)

The Priority Conversion Control register (PCCR) controls the priority conversion mode.

Priority conversion can be performed even while scan conversion is being performed.

In addition, different priority levels (two levels) can be given to priority conversion processes.

bit	15	14	13	12	11	10	9	8
Field	PEMP	PFUL	POVR	PFCLR	ESCE	PEEN	PHEN	PSTR
Attribute	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

[bit15] PEMP: Priority conversion FIFO empty bit

This bit is set when the FIFO goes to the empty state. When conversion data is written in the Priority Conversion FIFO Data register (PCFD), this bit is set to "0". Writing is ignored.

bit	Description							
0	Data remains in the FIFO.							
1	The FIFO is empty.							

[bit14] PFUL: Priority conversion FIFO full bit

This bit is set when FIFO goes to full state. When PFCLR bit is set to "1" or the Priority Conversion FIFO Data register (PCFD) is read, this bit is set to 0. Writing is ignored.

bit	Description						
0	Data can be input to the FIFO.						
1	The FIFO is full.						

[bit13] POVR: Priority conversion overrun flag

This bit is set when an attempt to write data to a full FIFO is made (conversion data in a full FIFO is not overwritten). The read value of Read-Modify-Write operation is 1 regardless of the bit value. When the OVRIE bit in the ADCR register is 1, an interrupt is generated to the CPU if the POVR bit is 1.

bit	Description						
Dit	Read	Write					
0	No overrun has occurred.	Clears this bit.					
1	Overrun has occurred.	No effect on operation.					

[bit12] PFCLR: Priority conversion FIFO clear bit

Setting this bit to 1 clears the priority conversion FIFO. FIFO becomes empty and the PEMP bit is set to 1.

hi4	Description						
bit	Read	Write					
0	The value is always "0"	No effect on operation					
1	The value is always "0".	Clears FIFO.					



[bit11] ESCE: External trigger analog input selection bit

This bit selects whether the external trigger analog input is selected with the P1A[2:0] bits in the Priority Conversion Input Selection register (PCIS) or the external input pin ECS[2:0] bits.

bit	Description							
0	The external trigger analog inputs are selected with P1A[2:0].							
1	The external trigger analog inputs are selected with an external input.							

Notes:

- It is not allowed to change the setting of the ESCE bit during A/D conversion. To change the setting, make sure the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the setting of the ESCE bit during no start factors period.
- If channel selection with external pins ECS[2:0] cannot be used due to the product specifications, be sure to set the ESCE bit to 0.

[bit10] PEEN: Priority conversion external start enable bit

Set this bit to 1 to start priority conversion using a falling edge of an external trigger pin input. Conversion started with an external trigger has priority level 1 (highest priority).

bit	Description							
0	External trigger start disable							
1	External trigger start enable							

[bit9] PHEN: Priority conversion timer start enable bit

Set this bit to 1 to start priority conversion using a rising edge from a timer. Software startup (PSTR = 1) is valid even when this bit is set to 1. Conversion started with an external trigger has priority level 2 (lower priority than level 1).

bit	Description						
0	Timer start disable						
1	Timer start enable						

[bit8] PSTR: Priority conversion start bit

Setting this bit to 1 starts A/D conversion. Conversion started with this bit has priority level 2 (lower than priority level 1). It is not possible to restart the conversion started with this bit.

bit	Description						
Dit	Read	Write					
0	The value is always "0"	No effect on operation					
1	The value is always "0".	Starts priority conversion.					



5.8 Priority Conversion FIFO Stage Count Setup Register (PFNS)

The Priority Conversion FIFO Stage Count Setup register (PFNS) sets up the generation of interrupt requests in priority conversion. When the specified count of FIFO stages store A/D conversion data, the interrupt request bit (PCIF) is set.

bit	7	6	5	4	3	2	1	0	
Field	Reserved		TEST	Γ[1:0]	Rese	rved	PFS[1:0]		
Attribute	=		F	₹	-		R	k/W	
Initial value	ue XX		XX XX				00		

[bit7:6] Reserved: Reserved bits

Writing has no effect on operation.

The read value is undefined.

[bit5:4] TEST[1:0]: Test bits

Write	Has no effect on operation.				
Read	The value is undefined.				

[bit3:2] Reserved: Reserved bits

Writing has no effect on operation.

The read value is undefined.

[bit1:0] PFS[1:0]: Priority conversion FIFO stage count setting bits

When A/D conversion data for the FIFO stage count (N + 1) set in PFS[1:0] is written, the interrupt request flag (PCIF) is set to 1.

bit1:0	Description
00	Generates an interrupt request when conversion result is stored in the first FIFO stage.
01	Generates an interrupt request when conversion result is stored in the second FIFO stage.
10	Generates an interrupt request when conversion result is stored in the third FIFO stage.
11	Generates an interrupt request when conversion result is stored in the fourth FIFO stage.



5.9 Priority Conversion FIFO Data Register (PCFD)

The Priority Conversion FIFO Data register (PCFD) consists of four FIFO stages and stores analog conversion results. Data can be retrieved sequentially by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	PD	PD	PD	PD	PD	PD	PD	PD	PD	PD	PD	PD		Rese	erved	
	11	10	9	8	7	6	5	4	3	2	1	0				
Attribute						F	₹							F	₹	
Initial value						0xX	ΧX							XX	XX	
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Re	eserved		INV	Rese	RS	RS	RS	F	Reserve	d	PC	PC	PC	PC	PC
				L	rved	2	1	0				4	3	2	1	0
Attribute		R		R	R		R			R				R		_
Initial value		XXX		1	Χ		XXX		XXX XXXXX							

[bit31:20] PD11 to PD0: Priority conversion result

The result of 12-bit priority A/D conversion is written.

[bit19:13] Reserved: Reserved bits

The read value is undefined.

[bit12] INVL: A/D conversion result disable bit

This bit is set when this register value is invalid.

bit	Description						
0	This register value is valid						
1	This register value is invalid						

[bit11] Reserved: Reserved bit

The read value is undefined.

[bit10:8] RS2 to RS0: Scan conversion start factor

The start factor of the priority conversion corresponding to this register value is shown.

bit10:8	Description					
001	Software start (priority level 2)					
010	Timer start (priority level 2)					
100	External trigger (priority level 1)					



[bit7:5] Reserved: Reserved bits

The read value is undefined.

[bit4:0] PC4 to PC0: Conversion input channel bits

The analog input channels corresponding to the conversion result written in PD11 to PD0 are written. Settings for channels not defined in the product specifications are not written. See the specified number of the analog input channels in the "Data Sheet" of each product.

bit4:0	Description
00000	ch.0
00001	ch.1
00010	ch.2
11101	ch.29
11110	ch.30
11111	ch.31

Notes:

- This register has different bit configurations depending on the FDAS bit setting in the A/D Status register (ADSR). When the FDAS bit is 1, see 3.3.6 Bit placement Selection for FIFO Data Registers.
- To perform a byte access to this register, read the most significant byte (bit31:24) to shift the FIFO data. Reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO. To perform a half word access to this register, read the most significant half word (bit31:16) to shift FIFO. Reading the other byte (bit15:0) does not shift FIFO. Performing a word access to this register shifts FIFO.
- If software and a timer are started simultaneously, 0b011 may be read from the RS[2:0] bits.
- Conversion started with an external trigger can be performed only when the analog input channel is between ch.0 to ch.7.



5.10 Priority Conversion Input Selection Register (PCIS)

The Priority Conversion Input Selection register (PCIS) is used to select the analog input channels for which priority conversion is performed. For software or timer start at priority level 2, only one channel can be selected from multiple analog input channels. For external trigger start at priority level 1, one channel can be selected from eight channels (ch.0 to ch.7).

bit	7	6	5	4	3	2	1	0
Field			P2A[4:0]	P1A[2:0]				
Attribute			R/W		R/W			
Initial value			00000		000			

[bit7:3] P2A[4:0]: Priority level 2 analog input selection

This bit specifies the analog input channel for a start at priority level 2 (software/timer). It can be selected from all channels. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

bit7:3	Description
00000	ch.0
00001	ch.1
00010	ch.2
11101	ch.29
11110	ch.30
11111	ch.31

[bit2:0] P1A[2:0]: Priority level 1 analog input selection

This bit specifies the analog input channel for a start at priority level 1 (external trigger). It can be selected from eight channels (ch.0 to ch.7).

bit2:0	Description
000	ch.0
001	ch.1
010	ch.2
101	ch.5
110	ch.6
111	ch.7

Note:

 It is not allowed to change the channel during A/D conversion. Be sure to write a value to P1A or P2A when the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.



5.11 A/D Comparison Value Setup Register (CMPD)

The A/D Comparison Value Setup register (CMPD) sets the value to be compared with the A/D conversion result. When the conditions set in both this register and the A/D Comparison Control register (CMPCR) are satisfied, the conversion result comparison interrupt request bit (CMPIF) in the A/D Control register (ADCR) is set.

bit	31	30	29	28	27	26	25	24				
Field	CMAD11	CMAD10	CMAD9	CMAD8	CMAD7	CMAD6	CMAD5	CMAD4				
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Initial value	0	0	0	0	0	0	0	0				
bit	23	22	21	20	19	18	17	16				
Field	CMAD3	CMAD2	Reserved									
Attribute	R/W	R/W	-									
Initial value	0	0	XXXXXX									

[bit31:22] CMAD11 to CMAD2: A/D conversion compare value setting bits

These bits set the value to be compared with the A/D conversion result.

The most significant 10 bits (bit11:2) of the A/D conversion result are compared with the value in this register (CMAD11 to CMAD2). The least significant two bits (bit1:0) of the A/D conversion result are not compared.

[bit21:16] Reserved: Reserved bits

The read value is undefined.



5.12 A/D Comparison Control Register (CMPCR)

The A/D Comparison Control register (CMPCR) controls the A/D comparison function. When the converted value is compared with the value in the A/D Comparison Value Setup register (CMPD) and the comparison condition in this register is satisfied, the conversion result comparison interrupt request bit (CMPIF) in the A/D Control register (ADCR) is set.

bit	7	6	5	4	3	2	1	0
Field	CMPEN	CMD1	CMD0			CCH[4:0]		
Attribute	R/W	R/W	R/W			R/W		
Initial value	0	0	0			00000		

[bit7] CMPEN: Conversion result comparison function operation enable bit

This bit enables the operation of the A/D comparison function.

bit	Description						
0	Stops the comparison function operation.						
1	Enables the comparison function operation.						

[bit6] CMD1: Comparison mode 1

This bit sets the condition for generating a conversion interrupt request.

bit	Description
0	Generates an interrupt request when the most significant 10 bits (bit11:2) of the A/D
0	conversion result is smaller than the CMPD set value.
1	Generates an interrupt request when the most significant 10 bits (bit11:2) of the A/D
1	conversion result is equal to or greater than the CMPD set value.

[bit5] CMD0: Comparison mode 0

This bit selects the comparison target. When this bit is 1, the setting of CCH[4:0] is invalid.

bit	Description
0	Compares the conversion result of the channel set in CCH[4:0].
1	Compares the conversion results of all channels.

[bit4:0] CCH[4:0]: Comparison target analog input channel

This bit sets the analog channel to be compared. When the CMD0 bit is 1, setting of this bit is invalid. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

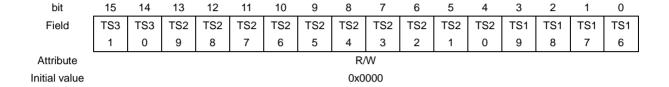
bit4:0	Description
00000	ch.0
00001	ch.1
00010	ch.2
11101	ch.29
11110	ch.30
11111	ch.31



5.13 Sampling Time Selection Register (ADSS)

The Sampling Time Selection register (ADSS3 to ADSS0) allows you to set the sampling time for each bit. Which of the sampling times set in Sampling Time Setup registers 0 and 1 (ADST0 and ADST1) is used is specified in this register.

ADSS3 (most significant byte: TS31 to TS24) and ADSS2 (least significant byte: TS23 to TS16)



[bit15:0] TS31 to TS16: Sampling time selection bits

Set the sampling time specified in the Sampling Time Setup register (ADST) for the corresponding channel. Setting 0 specifies the time set in ADST0 and setting 1 specifies the time set in ADST1. TS31 to TS16 correspond respectively to ch.31 to ch.16.

ADSS1 (most significant byte: TS15 to TS8) and ADSS0 (least significant byte: TS7 to TS0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Field	TS	TS	TS	TS	TS	TS	TS9	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	
	15	14	13	12	11	10											
Attribute	R/W																
Initial value	0x0000																

[bit15:0] TS15 to TS0: Sampling time selection bits

Set the sampling time specified in the Sampling Time Setup register (ADST) for the corresponding channel. Setting 0 specifies the time set in ADST0 and setting "1" specifies the time set in ADST1. TS15 to TS0 correspond respectively to ch.15 to ch.0.

Notes:

- It is not allowed to write to the ADSS register during A/D conversion. A/D conversion is not period
 of waiting start factors. It is allowed to write to the ADSS register during no start factors period.
- It is not possible to set 1 in the bit corresponding to a channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.



5.14 Sampling Time Setup Register (ADST)

Sampling Time Setup registers 0 and 1 (ADST0 and ADST1) set the sampling times for A/D conversion. ADST0 and ADST1 are provided for setting two sampling times, and which one is used is selected in the Sampling Time Selection register (ADSS3 to ADSS0).

ADST0 (most significant byte)

bit	15	14	13	12	11	10	9	8
Field	STX02	STX01	STX00	ST04	ST03	ST02	ST01	ST00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit15:13] STX02 to STX00: Sampling time N times setting bits

These bits multiply the sampling time set values in the ST04 to ST00 bits by N.

bit15	bit14	bit13	Description		
0	0	0	Set value x 1 (Initial value)		
0	0	1	Set value x 4		
0	1	0	Set value x 8		
0	1	1	Set value x 16		
1	0	0	Set value x 32		
1	0	1	Set value x 64		
1	1	0	Set value x 128		
1	1	1	Set value x 256		

[bit12:8] ST04 to ST00: Sampling time setting bits

These bit set the sampling time for A/D conversion.

Sampling time = HCLK cycle × Clock division ratio × {(ST set value + 1) × STX setting multiplier + 3}

Example: When ST04 to ST00 = 9, STX02, STX01, and STX00 = 001 (multiplied by 4), CT7 to CT0=0x00 (Clock frequency division ratio: 2), and HCLK = 20 MHz (50 ns), Sampling time = 50 ns \times 2 \times {(9 + 1) \times 4 + 3} = 4300ns

Notes:

- It is not allowed to write to the ADST0 register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST0 register during no start factors period.
- For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.
- When STX02, STX01, and STX00 = 000 (ST04 to ST00 set values multiplied by 1) are set, set ST04 to ST00 to 2 or more (1 or less must not be set).



ADST1 (least significant byte)

bit	7	6	5	4	3	2	1	0
Field	STX12	STX11	STX10	ST14	ST13	ST12	ST11	ST10
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit7:5] STX12 to STX10: Sampling time N times setting bits

These bits multiply the sampling time set values in the ST14 to ST10 bits by N.

bit7	bit6	bit5	Description
0	0	0	Set value x 1(initial value)
0	0	1	Set value x 4
0	1	0	Set value x 8
0	1	1	Set value x 16
1	0	0	Set value x 32
1	0	1	Set value x 64
1	1	0	Set value x 128
1	1	1	Set value × 256

[bit4:0] ST14 to ST10: Sampling time setting bits

These bit set the sampling time for A/D conversion.

Sampling time = HCLK cycle \times Clock division ratio \times {(ST set value + 1) \times STX setting multiplier + 3}

Example: When ST14 to ST10 = 9, STX12, STX11, and STX10 = 001 (multiplied by 4), CT7 to CT0=0x00 (Clock frequency division ratio: 2), and HCLK = 20 MHz (50 ns), Sampling time = 50 ns \times 2 \times {(9 + 1) \times 4 + 3} = 4300ns

Notes:

- It is not allowed to write to the ADST1 register during A/D conversion. A/D conversion is not
 period of waiting start factors. It is allowed to write to the ADST1 register during no start factors
 period.
- For setting the sampling time, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.
- When STX12, STX11, and STX10 = 000 (ST14 to ST10 set values multiplied by 1) are set, set ST14 to ST10 to 2 or more (1 or less must not be set).



5.15 Frequency Division Ratio Setup Register (ADCT)

The Frequency Division Ratio Setup register (ADCT) sets the clock frequency division ratio, which is part of the A/D conversion time.

bit	7	6	5	4	3	2	1	0
Field	CT7	CT6	CT5	CT4	CT3	CT2	CT1	СТ0
Attribute	R/W							
Initial value	0	0	0	0	0	1	1	1

[bit7:0] CT7 to CT0: Frequency division ratio setting bits

These bits set the division ratio of the HCLK frequency for generating the clock of A/D conversion.

The frequency division ratio setting is common in Sampling Setup registers 0 and 1 (ADST0/1).

bit7:0	Description
0x80	Frequency division ratio 1
0x00	Frequency division ratio 2
0x01	Frequency division ratio 3
0x02	Frequency division ratio 4
0X07	Frequency division ratio 9 (Initial value)
0x3C	Frequency division ratio 62
0x3D	Frequency division ratio 63
0x3E	Frequency division ratio 64
0x3F	Frequency division ratio 65

Compare clock cycle = Base clock (HCLK) cycle × Frequency division ratio Comparison time = Compare clock cycle × 14

Example: When the CT[7:0] set value = 0 (Compare frequency division ratio: 2) and HCLK = 20 MHz (50 ns),

Compare clock cycle = $50 \text{ ns} \times 2 = 100 \text{ ns}$ Comparison time = $100 \text{ ns} \times 14 = 1400 \text{ ns}$

Notes:

- Setting 0x40 to 0x7F to bit7:0 is not allowed.
- It is not allowed to write to the clock division setting register (ADCT) during A/D conversion. A/D
 conversion is not period of waiting start factors. It is allowed to write to the clock division setting
 register (ADCT) during no start factors period.
 - Only when the base clock prescaler register (BSC_PSR) of clock generator is set to 0x0, A/D conversion can be performed in frequency division ratio at 1.
- For setting the compare clock cycle, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.



5.16 A/D Operation Enable Setup Register (ADCEN)

The A/D Operation Enable Setup register (ADCEN) is used to turn the 12-bit A/D converter to the operation enable state.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Field			EN	IBLTI	ИЕ[15	:8]					Res	erved			READY	ENBL	
Attribute		R/W						R			R	R/W	_				
Initial value	0xFF					000	0000			0	0						

[bit15:8] ENBLTIME[15:8]: Operation enable state transition cycle selection bits

These bits select the cycle count of operation enable state transition period.

Operation enable state transition period= Base clock (HCLK) cycle × (ENBLTIME setting value × 4 + 1)

Example: When ENBLTIME[15:8] = 0xFF, and HCLK = 20MHz (50ns),

Operation enable state transition period = $50 \text{ ns} \times (255 \times 4 + 1) = 51050 \text{ ns}$

[bit7:2] Reserved: Reserved bits

The read value is undefined.

[bit1] READY: A/D operation enable state bit

This bit indicates whether the A/D converter is in the operation enable state or in the operation stop state. A/D conversion can be performed only in the operation enable state.

An A/D conversion request in the operation stop state is ignored.

If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

bit	Description					
0	Operation stop state					
1	Operation enable state					

[bit0] ENBL: A/D operation enable bit

This bit enables the operation of the A/D converter.

Writing 1 to the ENBL bit turns the A/D converter to the operation enable state after the period of operation enable state transitions. On the other hand, writing 0 to this bit turns the A/D converter to the operation stop state.

bit	Description
0	Stops operation
1	Enables operation

Note:

 For setting the period of operation enable state transition, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.

It is not allowed to rewrite ENBLTIME[15:8] during the period between writing 1 to ENBL bit and setting READY bit to 1.

When setting the CPU to the timer mode, the stop mode, RTC mode, deep standby STOP mode, and deep standby RTC mode, set the ENBL bit to 0 and turn the A/D converter to the operation stop state.



5.17 Upper Limit Setup Register (WCMPDH)

The Upper Limit Setup register (WCMPDH) is used to set the upper limit used for the range comparison.

bit	31	30	29	28	27	26	25	24		
Field	CMHD11	CMHD10	CMHD9	CMHD8	CMHD7	CMHD6	CMHD5	CMHD4		
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	0	0	0	0	0	0	0	0		
bit	23	22	21	20	19	18	17	16		
Field	CMHD3	CMHD2		Reserved						
Attribute	R/W	R/W		R						
Initial value	0	0		000000						

[bit31:22] CMHD11 to CMHD2: Upper limit bits

These bits specify the upper limit threshold used for range comparison.

bit31:22	Description				
	Upper limit				

[bit21:16] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

Note:

When the range comparison function enabled, the most significant 10 bits (bit11:2) of the A/D conversion result is compared with this register (CMHD). The comparison with the least significant 2 bits (bit1:0) of the A/D conversion result is not executed.



5.18 Range Comparison Control Register (WCMPCR)

The range comparison control register (WCMPCR) is used for the confirmation of continuous detection specification count and its state, the selection of within-range or out-of-range confirmation, the confirmation of upper limit excess or lower limit excess in the out-of-range area, and enabling and disabling of range comparison interrupt.

bit	7	6	5	4	3	2	1 0	
Field	RCOCD2	RCOCD1	RCOCD0	RCOIRS	RCOIE	RCOE	Reserved	
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R	
Initial value	0	0	1	0	0	0	00	

[bit7:5] RCOCD2 to RCOCD0: Continuous detection specification count/state indication bits

These bits indicate continuous detection specification count and continuous detection time state of range comparison result.

	Description							
bit7:5	At reading except in RMW accessing	At reading or at writing in RMW accessing						
000	Continuous detection state: 0 times	Setting prohibited						
001	Continuous detection state: 1 time	Specified continuous detection time: 1						
010	Continuous detection state: 2 times	Specified continuous detection time: 2						
011	Continuous detection state: 3 times	Specified continuous detection time: 3						
100	Continuous detection state: 4 times	Specified continuous detection time: 4						
101	Continuous detection state: 5 times	Specified continuous detection time: 5						
110	Continuous detection state: 6 times	Specified continuous detection time: 6						
111	Continuous detection state: 7 times	Specified continuous detection time: 7						

- When the range comparison result count reaches the continuous detection specification count, the range comparison interrupt factor flag bit (RCINT) of the corresponding start channel is set to 1. And the continuous detection state is stopped at the continuous detection specification count.
- At reading other the read-modify-write (RMW) access, the continuous detection state is read out.
- At reading other the read-modify-write (RMW) access, the written value (the continuous detection specification count) is read out.

Notes:

- Do not change the continuous detection specification count bit and state indication bit (RCOCD)
 while the range comparison operation is enabled (RCOE=1).
- Do not set 000 to the continuous detection specification count bit and state indication bit (RCOCD).



[bit4] RCOIRS: Selection bit of within-range and out-of- range confirmation

bit	Description						
0	Confirmation of out-of-range						
1	Confirmation of within-range						

- The A/D conversion result (scan conversion or priority conversion) selects the range comparison conditions of out-of- range or within-range for upper limit threshold bit (CMHD) and lower limit threshold bit (CMLD) selected by the upper/lower limit threshold selection bit (RCOTS).
- The range comparison condition at the out-of-range confirmation (RCOIRS=0) is as follows:

 A/D conversion result (scan conversion or priority conversion) > upper limit threshold bit (CMHD)

 Or, A/D conversion result (scan conversion or priority conversion) < lower limit threshold bit (CMLD)
- The range comparison condition at the within-range confirmation (RCOIRS=1) is as follows:
 A/D conversion result (scan conversion or priority conversion) ≤ upper limit threshold bit (CMHD)
 And, A/D conversion result (scan conversion or priority conversion) ≥ lower limit threshold bit
 (CMLD)
- At the range comparison detection for the out-of-range range confirmations (RCOIRS="0"), the upper limit threshold excess or below the lower limit threshold can be confirmed by threshold excess flag bit (RCOOF).

[bit3] RCOIE: Range comparison interrupt request enable bit

bit	Description				
0	Range comparison interrupt disabled				
1 Range comparison interrupt enabled					

■ When the range comparison interrupt factor flag bit (RCINT) of the corresponding startup channel is set to 1 and when the range comparison interrupt request is enabled (RCOIE=1), the interrupt request is generated.

[bit2] RCOE: Range comparison execution enable bit

Selects A/D comparison function and range comparison function.

bit	Description				
0	0 Range comparison execution disabled				
1	1 Range comparison execution enabled				

■ When the range comparison execution enable bit (RCOE) is 0, the range comparison execution is disabled. Moreover, the continuous detection count sate is initialized to 000.

When the range comparison execution enable bit (RCOE) is 1, the range comparison execution is enabled.

[bit1:0] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.



5.19 Lower Limit Threshold Setup Register (WCMPDL)

The lower limit threshold setup register (WCMPDL) is used to set the lower limit threshold for the range comparison.

bit	15	14	13	12	11	10	9	8
Field	CMLD11	CMLD10	CMLD9	CMLD8	CMLD7	CMLD6	CMLD5	CMLD4
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
Field	CMLD3	CMLD2			Rese	rved		
Attribute	R/W	R/W	R					
Initial value	0	0	000000					

[bit15:6] CMLD11 to CMLD2: Lower limit threshold bits

Set the lower limit threshold used for the range comparison.

bit15:6	Description		
Lower limit threshold			

[bit5:0] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

Note:

When the range comparison execution is enabled, the most significant 10 bits (bit11:2) of the A/D conversion result is compared with this register (CMLD). The comparison with the least significant 2 bits (bit1:0) of the A/D conversion result is not executed.



5.20 Range Comparison Channel Select Register (WCMPSR)

The range comparison channel select register (WCMPSR) is used to set the channel for the range comparison.

bit	15	14	13	12	11	10	9	8
Field	Reserved		WCMD	WCCH[4:0]				
Attribute	R		R/W	R/W				
Initial value	00		0			00000		

[bit15:14] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

[bit13] WCMD: Comparison mode select bit

bit	Description						
0	Compares the conversion result of the channel set with WCCH[4:0] bits.						
1	Compares the conversion results of all channels.						

Selects the target for the range comparison. When this bit is 1, the setting of WCCH[4:0] bits becomes invalid.

[bit12:8] WCCH[4:0]: Comparison target analog input channel

[in and the end in the parties in the ger annual group are entained.					
bit12:8		Description				
00000	Ch.0					
00001	Ch.1					
00010	Ch.2					
11101	Ch.29					
11110	Ch.30					
11111	Ch.31					

Selects the target analog input channel for comparison. When WCMD bit is 1, the setting of these bits is invalid. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the Data Sheet of the product used.



5.21 Range Comparison Threshold Excess Flag Register (WCMRCOT)

The range comparison threshold excess flag register (WCMCOT) is used to indicate that the comparison result is beyond the upper limit threshold or below the lower limit threshold in the out-of-range confirmation setting.

bit	31	30	29	28	27	26	25	24
Field		Reserved						
Attribute				F	₹			
Initial value				0x	00			
bit	23	22	21	20	19	18	17	16
Field				Rese	erved			
Attribute				F	₹			
Initial value				0x	00			
bit	15	14	13	12	11	10	9	8
Field				Rese	erved			
Attribute				F	₹			_
Initial value				0x	00			
bit	7	6	5	4	3	2	1	0
Field				Reserved				RCOOF
Attribute				R				R/W
Initial value				0000000				0

[bit31:1] Reserved: Reserved bits

When writing, always write 0. When reading, 0 is always read.

[bit0] RCOOF: Threshold excess flag bit

and process and control character may an							
bit Description							
0	Below the lower limit threshold (A/D data < Lower limit threshold bit)						
1	Beyond the upper limit threshold (A/D data > Upper limit threshold bit)						

- For the confirmation of outside-range (RCOIRS=0), this bit indicates that the range comparison result is greater than the upper limit threshold setting register (RCOOF=1), or the result is smaller than the lower limit threshold (RCOOF=0).
- For the confirmation of outside-range (RCOIRS=0), when the range comparison result is confirmed to be within the range, the threshold excess flag bit holds the prior value.
- When the range comparison interrupt factor flag bit (RCINT) of the corresponding startup channel is set to be 1, the threshold excess flag bit (RCOOF) is not updated and holds the prior value, even if the range comparison result is confirmed to be outside the range for the confirmation of outside-range (RCOIRS=0)
- For the confirmation of within-range (RCOIRS=1), the threshold excess flag bit has no meaning (the bit holds the prior value.)



5.22 Range Comparison Flag Register (WCMRCIF)

The range comparison flag register (WCMRCIF) indicates the interrupt factor due to the continuous detection of the range comparison result.

bit	31	30	29	28	27	26	25	24
Field				Rese	erved			
Attribute		R						
Initial value				0x	:00			
bit	23	22	21	20	19	18	17	16
Field		Reserved						
Attribute				F	3			
Initial value		0x00						
bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute				F	₹			_
Initial value		0x00						
Bit	7	6	5	4	3	2	1	0
Field				Reserved				RCINT
Attribute				R				R/W
Initial value	0000000 0					0		

[bit31:1] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

[bit0] RCINT: Range comparison interrupt factor flag bit

	moj reality realige companion mentapt ractor mag are						
bit	Description						
Dit	Read	Write					
0	Range comparison interrupt factor clear state	Bit clear					
1	State where the interrupt factor is generated due to the continuous detection of range comparison results	No change and no influence to others.					

- The RCINT bit is set to 1 by the continuous detection of the range comparison results of the corresponding startup channel.
- When RCINT bit and range comparison interrupt request permission (RCOIE) of the corresponding startup channel are 1, the range comparison interrupt request is generated.
- At writing, the RCINT bit is cleared by 0, the bit is not changed by 1 and has no influence to others.

Notes:

- At read-modify-write access (RMW), 1 is read.
- When the software clear (writing RCINT=0) and hardware set occurs simultaneously, the hardware set has a priority.

CHAPTER 1-2: 12-bit A/D Converter



CHAPTER 1-3: A/D Timer Trigger Selection



This chapter explains the functions and operations to select a timer trigger of the A/D converter.

- 1. Overview
- 2. Registers



1. Overview

This section explains the operations to select a timer trigger of the A/D converter.

Selecting a Timer Trigger of the A/D Converter

The A/D converter can be started by the factors shown in Table 1-1.

Table 1-1 A/D Converter Start Factor

Conversion Type		Start Factor
Priority level 1 conversion	-	Input from an external trigger pin (at falling edge)
	-	Software (when the Priority Conversion Start Bit(PSTR) of Priority Conversion
Priority level 2 conversion		Control Register (PCCR) is set to 1)
	-	Trigger input from timer (at rising edge)
	-	Software (when the Scan Conversion Start Bit (SSTR) of SCAN Conversion
Scan conversion		Control Register (SCCR) is set to 1)
	-	Trigger input from timer (at rising edge)

The A/D converter can be started with two types of timers: base timer and multifunction timer.

A timer start factor can be selected using the Scan Conversion Timer Trigger Selection Register (SCTSL) or Priority Conversion Timer Trigger Selection Register (PRTSL). The A/D converter starts A/D conversion if a rising edge of the selected timer is detected while timer starting is enabled.

The multiple A/D converters can use same start factor.

For details on the operations of the 12-bit A/D converter, see 3. Explanation of operations in the 12-bit A/D Converter.



2. Registers

This section explains the configuration and functions of the registers used to select an A/D timer trigger.

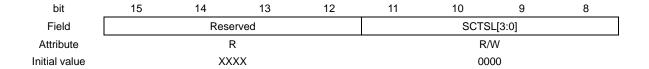
List of Timer Trigger Selection Registers for A/D Converter

Abbreviation	Register Name	Reference
SCTSL	Scan Conversion Timer Trigger Selection Register	2.1
PRTSL	Priority Conversion Timer Trigger Selection Register	2.2



2.1 Scan Conversion Timer Trigger Selection Register (SCTSL)

The Scan Conversion Timer Trigger Selection Register (SCTSL) is used to select a timer trigger when performing scan conversion.



[bit15:12] Reserved: Reserved bits

The read values are undefined.

Writing has no effect in operation.

[bit11:8] SCTSL[3:0]: Scan conversion timer trigger selection bits

bit11:8	Description
0000	No selected trigger (Input is fixed to 0.)
0001	Starts scan conversion with the multifunction timer.
0010	Base timer ch.0
0011	Base timer ch.1
0100	Base timer ch.2
0101	Base timer ch.3
0110	Base timer ch.4
0111	Base timer ch.5
1000	Base timer ch.6
1001	Base timer ch.7
1010	Base timer ch.8
1011	Base timer ch.9
1100	Base timer ch.10
1101	Base timer ch.11
1110	Base timer ch.12
1111	Base timer ch.13



2.2 Priority Conversion Timer Trigger Selection Register (PRTSL)

The Priority Conversion Timer Trigger Selection Register (PRTSL) is used to select a timer trigger when performing priority conversion.

bit	7	6	5	4	3	2	1	0
Field	Reserved			PRTSL[3:0]				
Attribute	R				R/	W		
Initial value	XXXX			00	00			

[bit7:4] Reserved: Reserved bits

The read values are undefined.

Writing has no effect in operation.

[bit3:0] PRTSL[3:0]: Priority conversion timer trigger selection bits

bit3:0	Description
0000	No selected trigger (Input is fixed to 0.)
0001	Starts priority conversion with the multifunction timer.
0010	Base timer ch.0
0011	Base timer ch.1
0100	Base timer ch.2
0101	Base timer ch.3
0110	Base timer ch.4
0111	Base timer ch.5
1000	Base timer ch.6
1001	Base timer ch.7
1010	Base timer ch.8
1011	Base timer ch.9
1100	Base timer ch.10
1101	Base timer ch.11
1110	Base timer ch.12
1111	Base timer ch.13

CHAPTER 1-3: A/D Timer Trigger Selection



CHAPTER 1-4: A/D Converter Offset Calibration



This chapter describes the offset calibration for the A/D converter.

- 1. Overview
- 2. Configuration Block Diagram
- 3. Operation
- 4. Setting Procedure Example
- 5. Register List
- 6. Usage Precautions



1. Overview

The A/D converter in this device has an offset error due to process variation.

Offset correction of the A/D converter is performed for correcting the zero-transition voltage and full scale transition voltage. This enables the elimination of intermediate code error for minimizing the overall error.

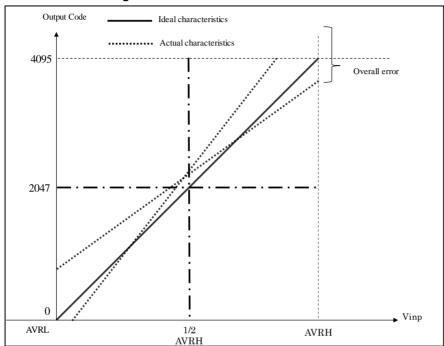
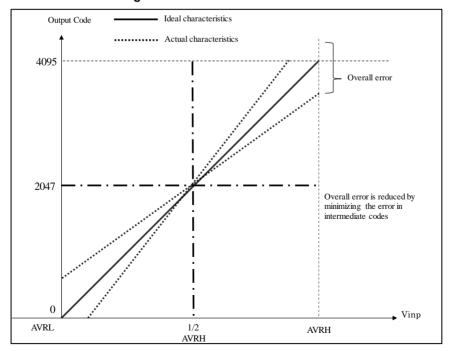


Figure 1-1 Overall Error before Correction







2. Configuration Block Diagram

The block diagram of the A/D converter offset calibration is shown in Figure 2-1.

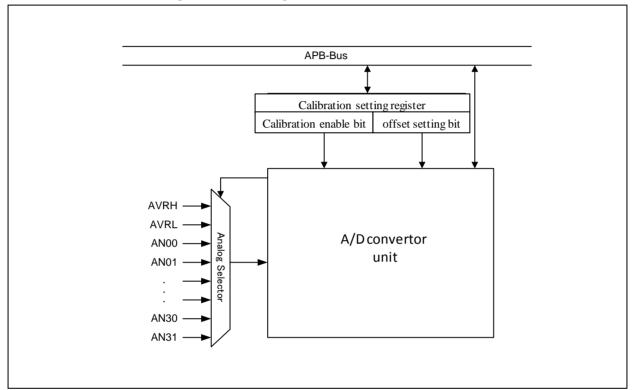


Figure 2-1 Block Diagram of A/D Converter Offset Calibration

Setting the calibration setting register connects AVRH and AVRL to the A/D converter, enabling A/D conversion.



3. Operation

This section describes the operation of the offset calibration for the A/D converter.

3.1 Operation of A/D Converter Offset Calibration

3.1.1 Setting the Value for Offset Calibration

An offset calibration value can be written to the offset calibration value setting bit (OFST) in the calibration setting register (CALSR) to correct the offset error of the A/D converter due to process variation.

Figure 3-1 shows the change in characteristics when offset calibration is performed.

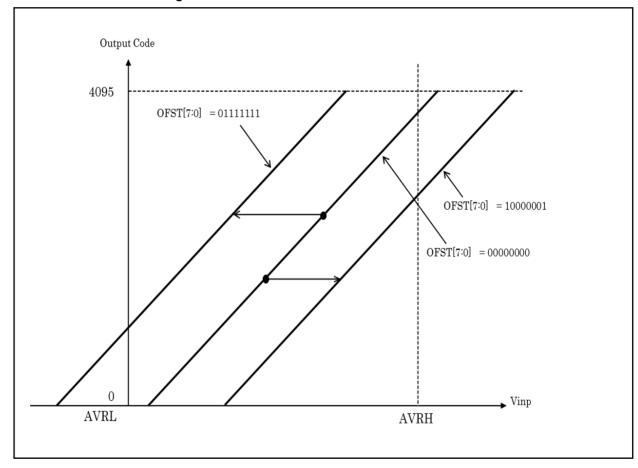


Figure 3-1 Offset Characteristics



3.1.2 A/D Converter Offset Calibration

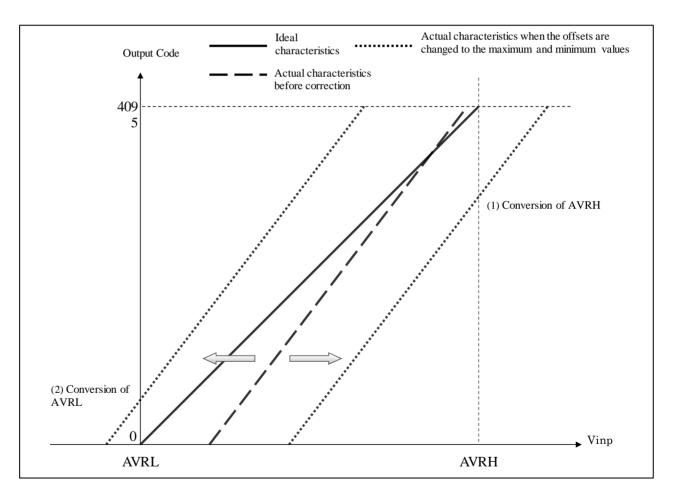
Following three steps must be completed to perform offset calibration for the A/D converter.

- A/D conversion of the analog reference voltage value AVRH
- A/D conversion of the analog reference voltage value AVRL
- Calculation of offset calibration value

The detailed setting steps are provided starting from section 3.1.3.

An A/D conversion must be performed for the analog reference voltage value before performing offset calibration for the A/D converter. For this purpose, an A/D conversion of the analog reference voltage value (AVRH/AVRL) is provided.

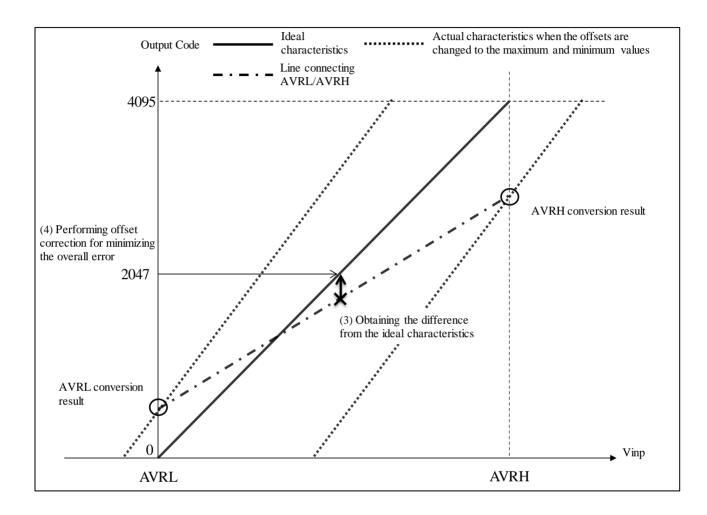
In A/D conversion of AVRH/AVRL, maximum offset correction is performed to obtain the code for AVRH/AVRL.



- (1) For details on the AVRH conversion method, see 3.1.3.1 AVRH Conversion Method.
- (2) For details on the AVRL conversion method, see 3.1.3.2 AVRL Conversion Method.



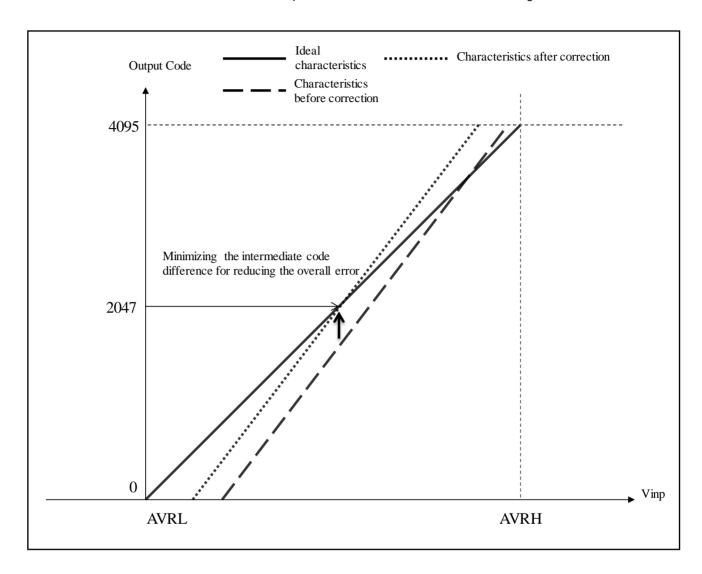
Next, connect the AVRH conversion result and AVRL conversion result with a line, and find the difference between the ideal line and the intermediate code. The difference from the ideal line indicates the code amount for which calibration is required.



For details on (3) and (4), see 3.1.4 Calculation of Offset Calibration Value.



The intermediate code difference required for calibration is minimized for reducing the overall error.





3.1.3 A/D Converter Offset Calibration Setting Example

3.1.3.1 AVRH Conversion Method

- 1. Only the bit that corresponds to AN0 of the scan conversion input selection register (SCIS) is set to 1. and all other bits are set to 0.
- 2. The CALEN bit in the calibration setting register (CALSR) is set to 1, and the OFST bit is set to 0x81.
- 3. Scan conversion of the A/D converter is performed, and the conversion results are fetched from the scan conversion FIFO data register (SCFD) after the conversion is completed.

3.1.3.2 AVRL Conversion Method

- 1. The bit that corresponds to AN1 of the scan conversion input selection register (SCIS) only is set to 1, and all other bits are all set to 0.
- 2. The CALEN bit of the calibration setting register (CALSR) is set to 1, and the OFST bit is set to 0x7F.
- 3. Scan conversion of the A/D converter is performed, and the conversion results are fetched from the scan conversion FIFO data register (SCFD) after the conversion is completed.

3.1.4 Calculation of Offset Calibration Value

The calculation method for data that is written to the offset calibration value setting bit (OFST) in the calibration setting register (CALSR) is shown below.

The formula below is used to calculate the difference of intermediate code between the actual characteristics and ideal characteristics based on the AVRH/AVRL voltage conversion values.

OFT_VRH: A/D conversion value of AVRH OFT_VRL: A/D conversion value of AVRL

The offset calibration value (OFST) is calculated from the OFT_CAL calculation value, and it is written to the offset calibration value setting bit (OFST).

OFST	OFT_CAL
0x7F	+127
	:
0x01	+1
0x00	0
0xFF	-1
÷	:
0x81	-127
0x80	Setting prohibited



4. Setting Procedure Example

This section provides an example of the setting procedure for the offset calibration function for the A/D converter.

Start Initial setting ·Sampling time setting (ADST0, ADST1, and ADSS are set) ·Clock frequency division ratio setting (ADCT is set) ·FIFO data layout setting (ADSR:FDAS="1" Write) · A/D conversion function is not used (CMPCR:CMPEN="'0" Write) ·Interrupt is not used (ADCR:SCIE="0" Write) Analog reference voltage (AVRH) is set to the analog input channel ·Scan conversion input selection register setting (SCIS3=SCIS2=SCIS1="0x00" Write, SCIS0="0x01" Write) · Setting of calibration setting register (CALSR) (CALEN="1" Write, OFST="0x81" Write) ·FIFO clear (SCCR:SFCLR="1" Write) ·Conversion mode setting (SCCR:RPT="0" Write) · A/D software start (SCCR:SSTR="1" Write) Read the lower 16 bits of SCFD register Data enable/disable No determination SCFD:INVL="0"? Read the upper 16 bits of SCFD register (AVRH A/D conversion result reading) **END**

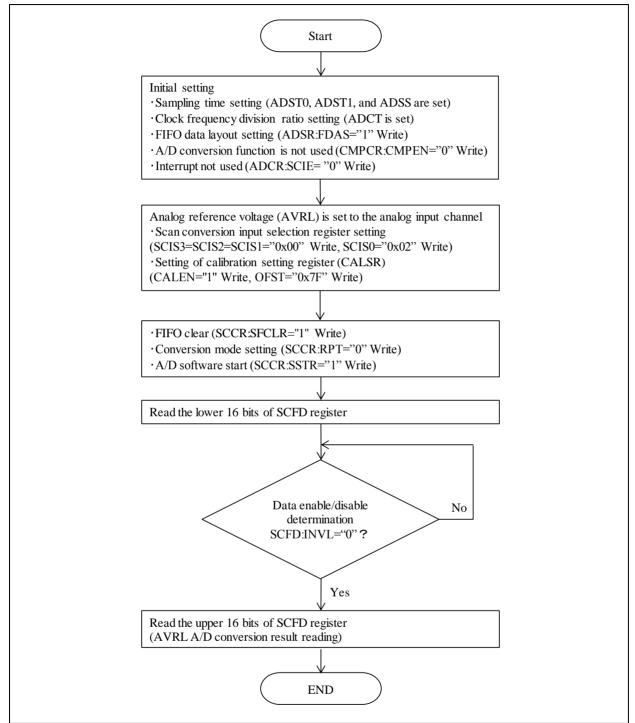
Figure 4-1 Example of AVRH A/D Conversion Setting Procedure

Note:

 The A/D conversion of AVRH/AVRL can be performed at the fastest speed setting provided in "Electrical Characteristics" of the Data Sheet for your product.



Figure 4-2 Example of AVRL A/D Conversion Setting Procedure



Note:

 The A/D conversion of AVRH/AVRL can be performed at the fastest speed setting provided in Electrical Characteristics of the Data Sheet for your product.



5. Register List

This section describes the registers for the offset calibration function of the A/D converter.

Register Abbreviation	Register Name	Reference
CALSR	Calibration setting register	5.1



5.1 Calibration Setting Register (CALSR)

The calibration setting register (CALSR) is used to set whether calibration (offset calibration) is allowed and to set the offset calibration value.

Bit	31	9	8	7		0
Field	Reserved		CLBEN		OFST	
Attribute	-		R/W		R/W	
Default value	-		0		0x00	

[bit31:9] Reserved: Reservation bit

A value read out always be 0.

Write a value of 0.

[bit8] CLBEN: Calibration permission bit

This bit determines whether the calibration operation of the A/D converter is permitted.

Bit	Description	
0	Calibration operation stop (default value)	
1	Calibration operation permitted	

[bit7:0] OFST: Offset calibration value setting bit

This bit sets the offset calibration value of the A/D converter.

Bit	Description	
Writing	This bit sets the offset calibration value of the A/D converter.	
Reading	The value that was set is read out.	
	The default value is 0x00.	

The OFST bit can be changed to set the calibration values shown below.

For details OFT_CAL, see 3.1.4 Calculation of Offset Calibration Value.

OFST	OFT_CAL
0x7F	+127
:	:
0x01	+1
0x00	0
0xFF	-1
:	:
0x81	-127
0x80	Setting prohibited

Notes

- Overwriting of this register is prohibited during A/D conversion.
- When set to calibration operation permitted (CLBEN=1), conversion operations other than scan conversion are prohibited.



6. Usage Precautions

This section provides the usage precautions of the offset calibration for the A/D converter.

- Overwriting of the calibration setting register (CALSR) is prohibited during A/D conversion.
- When the calibration operation is permitted (CALEN=1 for the calibration setting register (CALSR)), all conversion operations other than scan conversion are prohibited.
- Before performing the calibration operation, stop the conversion operations for units other than the unit performing calibration. Simultaneous calibration of multiple units is prohibited.
- During A/D conversion of AVRH and AVRL, do not restart scan conversion by setting SSTR of the scan conversion control register (SCCR) to 1.
- If A/D conversion is performed for a channel other than AVRH and AVRL, be sure to always set the offset calibration value setting bit (CLBEN) of the calibration setting register (CALSR) to 0.
- If measurement error occurred due to the measurement environment, perform conversion of AVRH/AVRL multiple times, and then use the average value to perform offset calibration.

CHAPTER 1-4: A/D Converter Offset Calibration



CHAPTER 2: 12-bit D/A Converter



This chapter explains the functions and operations of the 12-bit D/A converter.

- 1. Overview
- 2. Configuration
- 3. Operations
- 4. Example of Setting Procedure
- 5. Registers



1. Overview

The 12-bit D/A converter converts a 12-bit digital value into an analog value.

Features of the 12-bit D/A Converter

- 12-bit resolution (Maximum: 2 units)
 - 12-bit mode / 10-bit mode can be selected.
- R-2R method
- The 12-bit D/A converter stops operating in the following low power consumption modes.
 - RTC mode
 - Stop mode
 - Deep standby RTC mode
 - Deep standby Stop mode



2. Configuration

This section shows the configuration of the 12-bit D/A converter.

Peripheral bus

D/A converter operation enable bit

Digital input

Stop

Analog output

Analog output

D/A converter

Avcc

STOP mode
Deep standby RTC mode
Deep standby STOP mode
Deep standby STOP mode

Figure 2-1 12-bit D/A Converter Block Diagram



3. Operations

This section explains the operations of the 12-bit D/A converter.

Set the 12-bit D/A converter to operation enable state before performing D/A conversion. When 1 is written to the DAE bit in the D/A Control register (DACR), the 12-bit D/A converter transits from operation stop state to operation enable state. When 0 is written to the DAE bit in the D/A Control register (DACR), the 12-bit D/A converter immediately changes to operation stop state.

D/A conversion can be executed only in the operation enable state. D/A conversion is prohibited in the operation stop state.

It can be checked whether the 12-bit D/A converter is in the operation enable state by reading the DRDY bit in the D/A Control register (DACR).

If a value is written to the D/A Data Register (DADR) in the operation enable state, the 12-bit D/A converter converts the digital value written into an analog value and outputs the analog value from the DAx pin. In this situation, the direction of the I/O port is input, input to the I/O port is blocked, and the I/O port is disconnected from the pull-up register.

In certain low power consumption modes, regardless of the setting of the DAE bit, the operation of the 12-bit D/A converter stops.

If the DAE bit in the D/A Control register (DACR) is 1 when the 12-bit D/A converter returns from a low power consumption mode, the 12-bit D/A converter transits from the operation stop state to the operation enable state after the operation enable state transition period has elapsed.

Table 3-1 shows the operation state of the 12-bit D/A converter.

Table 3-1 Operation State of the 12-bit D/A Converter

Operation mode	DRDY	12-bit D/A Converter Operation
RTC mode STOP mode Deep standby RTC mode Deep standby STOP mode	-	Stopped
Modes other than the above	0	Stopped
Wodes other than the above	1	Enabled

In 12-bit mode, the voltage that can be output when the operation of the 12-bit D/A converter is enabled ranges from 0.0 V to 4095/4096×AVCC (AVCC: voltage of the AVCC pin). Table 3-2 shows the relation between the D/A Data Register (DADR) and the ideal output voltage.

Table 3-2 Relation between DA[11:0] and Analog Output Value in 12-bit Mode

DA[11:0]	Ideal Output Voltage
00000000000	0 / 4096 × AVCC
00000000001	1 / 4096 × AVCC
00000000010	2 / 4096 × AVCC
111111111101	4093 / 4096 × AVCC
111111111110	4094 / 4096 × AVCC
111111111111	4095 / 4096 × AVCC



In 10-bit mode, the voltage that can be output when the operation of the 12-bit D/A converter is enabled ranges from 0.0 V to 1023/1024×AVCC (AVCC: voltage of the AVCC pin). Table 3-3 shows the ideal output voltages with the 10-bit mode data allocation selection bit (DDAS) in the D/A Data Register (DADR) set to 0, and Table 3-4 shows the ideal output voltages with the 10-bit mode data allocation selection bit (DDAS) in the D/A Data Register (DADR) set to 1.

Table 3-3 Relation between DA[11:0] of DDAS=0 and Analog Output Value

DA[11:0]	Ideal Output Voltage
00000000000	0 / 1024 × AVCC
00000000100	1 / 1024 × AVCC
00000001000	2 / 1024 × AVCC
111111110100	1021 / 1024 × AVCC
111111111000	1022 / 1024 × AVCC
111111111100	1023 / 1024 × AVCC

Table 3-4 Relation between DA[11:0] of DDAS=1 and Analog Output Value

DA[11:0]	Ideal Output Voltage
00000000000	0 / 1024 × AVCC
00000000001	1 / 1024 × AVCC
00000000010	2 / 1024 × AVCC
001111111101	1021 / 1024 × AVCC
001111111110	1022 / 1024 × AVCC
001111111111	1023 / 1024 × AVCC

When the 12-bit D/A converter stops operating, its output is Hi-Z.



4. Example of Setting Procedure

This section provides an example of the procedure for setting the 12-bit D/A converter.

Below is the setting procedure for making the 12-bit D/A converter operate and output a conversion result to the DAx pin.

- 1. Set the operation mode using DAC10 and DDAS in the D/A Control register (DACR), and set the DAE bit to 1.
- 2. Wait until the DRDY bit in the D/A Control register (DACR) becomes 1.
- 3. Write to the D/A Data register (DADR) the digital value to be converted into an analog value.

After the above settings have been completed, an analog value is output from the DAx pin.

Notes:

 After DAE in the D/A Control register (DACR) has been set to 1, the output of the DAx pin is indeterminate until a digital value is written to the D/A Data register (DADR).



5. Registers

This section explains the configuration and functions of registers used in the 12-bit D/A converter.

List of 12-bit D/A Converter Registers

Abbreviation	Register Name	Reference
DACR	D/A Control register	5.1
DADR	D/A Data register	5.2



5.1 D/A Control Register (DACR)

The D/A Control register (DACR) controls the operation of the 12-bit D/A converter.

bit	23	22	21	20	19	18	17	16
Field	Rese	rved	DDAS	DAC10	Rese	erved	DRDY	DAE
Attribute	-		R/W	R/W	-	:	R	R/W
Initial value	XX	<	0	0	X	Χ	0	0

[bit23:22] Reserved: Reserved bits

The read value is indeterminate.

Writing a value to a reserved bit has no effect on operation.

[bit21] DDAS: 10-bit mode data allocation selection bit

In 10-bit mode, DDAS selects the conversion target bits in the D/A Data register (DADR).

In 12-bit mode, regardless of the setting of this bit, DA[11:0] in the D/A Data register (DADR) are selected as the conversion target bits.

bit	Description				
0	DA[11:2] in the D/A Data register (DADR)				
1	DA[9:0] in the D/A Data register (DADR)				

[bit20] DAC10: 10-bit mode

DAC switches the operation mode of the 12-bit D/A converter between 10-bit mode and 12-bit mode.

bit	Description			
0	12-bit mode			
1	10-bit mode			

[bit19:18] Reserved: Reserved bits

The read value is indeterminate.

Writing a value to a reserved bit has no effect on operation.

[bit17] DRDY: D/A converter operation enable state bit

bit	Description			
0	Operation stop state			
1	Operation enable state			

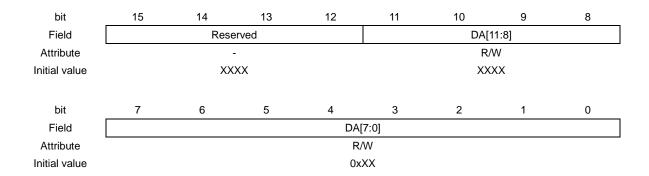
[bit16] DAE: D/A converter operating enable bit

bit	Description				
0	Stops the operation of the D/A converter.				
1	Enables the operation of the D/A converter.				



5.2 D/A Data Register (DADR)

The D/A Data Register sets the digital value to be converted into analog signal.



[bit15:12] Reserved: Reserved bits

The read value is indeterminate.

Writing a value to a reserved bit has no effect on operation.

[bit11:0] DA[11:0]: D/A Data Register

The 12-bit D/A converter executes D/A conversion immediately after a value has been written to DA[11:0]. In 10-bit mode, write 0 to an unused bit.

See Table 3-2 for the relation between the setting of this register and the output voltage.

CHAPTER 2: 12-bit D/A Converter



Appendixes



This chapter shows the register map, list of notes, limitations and product type list.

- A. Register Map
- B. List of Notes

A. Register Map



This chapter shows the register map.

1. Register Map

- 1.1 FLASH_IF
- 1.2 Unique ID
- 1.3 ECC Capture Address
- 1.4 Clock/Reset
- 1.5 HW WDT
- 1.6 SW WDT
- 1.7 Dual_Timer
- 1.8 MFT
- 1.9 PPG
- 1.10 Base Timer
- 1.11 IO Selector for Base Timer
- 1.12 QPRC
- 1.13 QPRC NF
- 1.14 A/DC
- 1.15 CR Trim
- 1.16 EXTI
- 1.17 INT-Req. READ
- 1.18 D/AC
- 1.19 HDMI-CEC
- 1.20 GPIO
- 1.21 LVD
- 1.22 DS_Mode
- 1.23 USB Clock
- 1.24 CAN_Prescaler
- 1.25 MFS
- 1.26 CRC
- 1.27 Watch Counter
- 1.28 RTC
- 1.29 Low-speed CR Prescaler
- 1.30 Peripheral Clock Gating
- 1.31 Smart Card Interface
- 1.32 MFSI2S
- 1.33 I2S Prescaler
- 1.34 GDC_Prescaler
- 1.35 EXT-Bus I/F



- 1.36 USB
- 1.37 DMAC
- 1.38 DSTC
- 1.39 CAN
- 1.40 Ethernet-MAC
- 1.41 Ethernet-Control
- 1.42 I2S
- 1.43 SD-Card
- 1.44 CAN FD
- 1.45 Programmable-CRC
- 1.46 WorkFlash_IF
- 1.47 High-Speed Quad SPI Controller
- 1.48 HyperBus Interface
- 1.49 GDC Sub System Controller
- 1.50 GDC Sub System SDRAM Controller



1. Register Map

Register map is shown on the table every module/function.

[How to read the each table]

Module/function name and its base address

Clock/Reset Base_Address : 0x4001_0000

Base_A	ddress			Regi	ster	
+ Address +3		+2 +1		+0		
0x000 -					SCM_CTL[B,H,W	
			-	-	00000-0-	
0.004					SCM_STR[B,H,V	
UXU	0x004 -			-	-	00000-0-
0x0	00			STB_CT	_[B,H,W]	
UXU	06			00000000 000000	0000	
0.00	00	-		T _	R	RST_STR[B,H,W]
0.00	0x00C ↑				-	 0 00000- 0 1
		ı	Initial va	lue after reset		
	-:	Reserved area	"1":	Initial value is 1		
	*:	Test register area	"0":	Initial value is (1	
			"X":	Initial value is u	ndefined	
			" - ":	Reserved bit		
			Register	name		J
			Access u	nit		
			(B: byte,	, H : half word, W :	word)	
			_	=	For word-length acces	ss, the "+0" column of the registe
			the LSB	of the data.)		

Notes:

- The register table is represented in the little-endian.
- When performing a data access, the addresses should be as below according to the access size.
- Word access: Address should be multiples of 4 (least significant 2 bits should be 0x00)
- Half word access: Address should be multiples of 2 (least significant bit should be 0x0)
- Byte access:
- Do not access the test register area.
- Do not access the area that is not written in the register table.
- When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.



1.1 FLASH_IF

1.1.1 TYPE1-M4, TYPE2-M4 Products

FLASH_IF Base_Address: 0x4000_0000

Base_Address		Register						
+ Address	+3	+3 +2 +1 +0						
0x000		FASZR[B,H,W]					
0x004		FRWTR	[B,H,W]					
0x008		FSTR[E	3,H,W]					
0x00C		*						
0x010		FSYNDN[B,H,W]						
0x014		FBFCR[B,H,W]						
0x018 - 0x01C	-							
0x020		FICR[E	3,H,W]					
0x024		FISR[B,H,W]						
0x028		FICLR[B,H,W]						
0x02C - 0x0FC	-							
0x100		CRTRMM[B,H,W]						
0x104 - 0x1FC	-	-	-	-				

Note:

- For details of Flash I/F registers, see Flash Programming Manual of the product used.



1.1.2 TYPE3-M4 Product

FLASH_IF Base_Address: 0x4000_0000

Base_Address		Register						
+ Address	+3	+3 +2 +1 +0						
0x000		FASZ	R[B,H,W]					
0x004		FRWT	R[B,H,W]					
0x008		FSTF	R[B,H,W]					
0x00C			*					
0x010		FSYND	DN[B,H,W]					
0x014		FBFC	R[B,H,W]					
0x018 - 0x01C	-	-	-	-				
0x020		FICR[B,H,W]						
0x024		FISR[B,H,W]						
0x028		FICLR[B,H,W]						
0x02C	-	-	-	-				
0x030		DFC	TRLR[W]					
0x034 - 0x0FC	-	-	-	-				
0x100		CRTRN	MM[B,H,W]					
0x104 - 0x10C	-	-	-	-				
0x110		FGPDM1[B,H,W]						
0x114		FGPDI	M2[B,H,W]					
0x118		FGPDM3[B,H,W]						
0x11C		FGPDI	И4[B,H,W]					
0x120 - 0x1FC	-	-	-	-				

Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x400	DFASZR[B,H,W]						
0x404	DFRWTR[B,H,W]						
0x408	DFSTR[B,H,W]						
0x40C - 0x4FC	-						

Note:

- For details of Flash I/F registers, see Flash Programming Manual of the product used.



1.1.3 TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

FLASH_IF Base_Address: 0x4000_0000

Base_Address	Register						
+ Address	+3	+2	+1	+0			
0x000		FASZ	R[B,H,W]	<u>.</u>			
0x004		FRW	ΓR[B,H,W]				
0x008		FSTI	R[B,H,W]				
0x00C			*				
0x010		FSYNI	DN[B,H,W]				
0x014		FBFC	R[B,H,W]				
0x018 - 0x01C	-	-	-	-			
0x020		FICE	R[B,H,W]				
0x024	FISR[B,H,W]						
0x028		FICL	R[B,H,W]				
0x02C - 0x0FC	=	-	-	-			
0x100		CRTRI	MM[B,H,W]				
0x104 - 0x10C	=	-	-	-			
0x110		FGPD	M1[B,H,W]				
0x114	FGPDM2[B,H,W]						
0x118	FGPDM3[B,H,W]						
0x11C		FGPD	M4[B,H,W]				
0x120 - 0x1FC			-				

Note:

- For details of Flash I/F registers, see Flash Programming Manual of the product used.



1.2 Unique ID

Unique ID Base_Address : 0x4000_0200

Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x000		UIDR0[W]					
		XXXXXXX XXXXXXX XXXXXXX XXXXXXX XXXX					
0x004		UIDR1[W]					
		XXXXX XXXXXXXX					
0x008 - 0xDFC	=	-	-	-			

1.3 ECC Capture Address

ECC Capture Address Base_Address : 0x4000_0300

Base_Address		Register				
+ Address	+3	+3 +2 +1 +0				
0x000		FERRAD[W]				
0x004 - 0xFFC	=	-	-	-		



1.4 Clock/Reset

1.4.1 TYPE1-M4, TYPE2-M4 Products

Clock/Reset Base_Address : 0x4001_0000

Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x000	_	_	_	SCM_CTL[W]		
0.000				00000-0-		
0x004	<u>-</u>	-	-	SCM_STR[W]		
0,0004				00000-0-		
0x008	STB_CTL[W]					
	00000000 000000000-000					
0x00C	_	-	RST_S			
			0 0	00001		
0x010	=	-	-	BSC_PSR[W]		
0.010				000		
0x014	_	_	_	APBC0_PSR[W]		
0.014				00		
0x018	_			APBC1_PSR[W]		
0.016	-	-	-	1000		
0,010		-		APBC2_PSR[W]		
0x01C	-		-	1000		
0.000				SWC_PSR[W]		
0x020	-	-	-	00		
0x024 - 0x027	-	-	-	-		
0000				TTC_PSR[W]		
0x028	-	-	-	00		
0x02C - 0x02F	-	-	-	-		
				CSW_TMR[W]		
0x030	-	-	-	00000000		
				PSW_TMR[W]		
0x034	-	-	-	0-000		
				PLL_CTL1[W]		
0x038	-	-	-	00000000		
				PLL_CTL2[W]		
0x03C	-	-	-	000000		
			CSV_C			
0x040	-	-	-11100			
			3	CSV_STR[W]		
0x044	-	-	-	00		
			FCSWH.			
0x048	-	-	11111111			
			FCSWL_			
0x04C	-	-	00000000			
			00000000	0000000		





Base_Address	Register			
+ Address	+3	+2	+1	+0
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W]
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] 0000
0x064	-	-	-	INT_STR[W] 0-000
0x068	-	-	-	INT_CLR[W] 0000
0x06C – 0xFFC	-	-	-	-



1.4.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

Clock/Reset Base_Address : 0x4001_0000

Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x000	-	-	-	SCM_CTL[W] 00000-0-	
0x004	-	-	-	SCM_STR[W] 00000-0-	
0x008		STB_CTL[W] 00000000 000000000-000			
0x00C	-	-	_	STR[W] 000001	
0x010	-	-	-	BSC_PSR[W] 000	
0x014	-	-	-	APBC0_PSR[W]00	
0x018	-	-	-	APBC1_PSR[W] 1000	
0x01C	-	-	-	APBC2_PSR[W] 1000	
0x020	-	-	-	SWC_PSR[W]	
0x024 - 0x027	-	-	-	-	
0x028	-	-	-	TTC_PSR[W] 00	
0x02C - 0x02F	-	-	-	-	
0x030	-	-	-	CSW_TMR[W] 00000000	
0x034	-	-	-	PSW_TMR[W]0-000	
0x038	-	-	-	PLL_CTL1[W] 00000000	
0x03C	-	-	-	PLL_CTL2[W] 000000	
0x040	-	-		CTL[W])11	
0x044	-	-	-	CSV_STR[W] 00	
0x048	-	-	FCSWH 11111111	_CTL[W] 11111111	
0x04C	-	-		_CTL[W] 00000000	





Base_Address		R	Register			
+ Address	+3	+2	+1	+0		
0x050	-	-		_CTL[W] 00000000		
0x054	-	-	-	DBWDT_CTL[W]		
0x058	-	-	-	*		
0x05C - 0x05F	-	-	-	-		
0x060	-	-	-	INT_ENR[W] 0000		
0x064	-	-	-	INT_STR[W] 0-000		
0x068	-	-	-	INT_CLR[W] 0000		
0x06C - 0x070	-	-	-	-		
0x074		PLLCG_CTL[W] 11111111 00000000 0000				
0x078 – 0xFFC	-	-	-	-		



1.5 HW WDT

HW WDT Base_Address: 0x4001_1000

Base_Address		Register			
+ Address	+3	+2	+1	+0	
0x000			LDR[W] 0 11111111 11111111		
0x004		WDG_VLR[W] XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	-	-	-	WDG_CTL[W] 11	
0x00C	-	-	-	WDG_ICL[W] XXXXXXXX	
0x010	-	-	-	WDG_RIS[W] 0	
0x014			*		
0x018 – 0xBFC	=	-	-	=	
0xC00		WDG_LCK[W] 00000000 00000000 000000001			
0xC04 - 0xFFC	-	-	-	-	

1.6 SW WDT

SW WDT Base_Address: 0x4001_2000

Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x000		Wdog	Load[W]		
0.000		11111111 11111111	1 11111111 11111111		
0x004			Value[W]		
0,004		11111111 11111111	1 11111111 11111111		
0000				WdogControl[W]	
0x008	-	-	-	00000	
_		Wdog	IntClr[W]		
0x00C			X XXXXXXXX XXXXXXX		
	x010 -			WdogRIS[W]	
0x010		-	-	0	
0x014			*		
0::040				WdogSPMC[W]	
0x018	-	-	-	0	
0x01C - 0xBFC	-	-	-	-	
		Wdog	Lock[W]		
0xC00		-	00000000 00000000		
0xC04 - 0xDFC	-	-	-	-	
0xF00 - 0xF04			*		
0xF08 - 0xFDF	-	-	-	-	
0xFE0 - 0xFFC			*		



1.7 Dual_Timer

Dual_Timer Base_Address: 0x4001_5000

Base_Address		Register				
+ Address	+3	+2	+1	+0		
0x000	Timer1Load[W]					
0x000		00000000 00000000 00000000 00000000				
0x004		Time	er1Value[W]			
0,004		11111111 11111	111 11111111 11111111			
0x008		Time	r1Control[W]			
0,000			00100000			
0x00C		Time	er1IntClr[W]			
00000		XXXXXXXX XXXXXX	XXX XXXXXXXX XXXXXXXX			
0x010		Tim	ner1RIS[W]			
0,010			0			
0x014		Timer1MIS[W]				
0x014			0			
0x018		Time	1BGLoad[W]			
0.018		00000000 00000000 00000000 00000000				
0x020		Tim	er2Load[W]			
0,020		00000000 00000	000 00000000 00000000			
0x024		Timer2Value[W]				
0,024		11111111 11111	111 11111111 11111111			
0x028		Time	r2Control[W]			
0,020			00100000			
0x02C		Time	er2IntClr[W]			
0,020		XXXXXXXX XXXXXX	XXX XXXXXXXX XXXXXXXX			
0x030		Tim	ner2RIS[W]			
0,000		0				
0x034			ner2MIS[W]			
0,004			0			
0x038			² BGLoad[W]			
0,000		00000000 00000	000 00000000 00000000			
0x040 - 0xFFC	-	-	-	=		



1.8 MFT

1.8.1 TYPE1-M4, TYPE2-M4 Products

MFT unit0 Base_Address : 0x4002_0000

MFT unit1 Base_Address : 0x4002_1000

MFT unit2 Base_Address: 0x4002_2000

Base_Address		Register			
+ Address	+3	+2	+1	+0	
0.400	OCCP	0[H,W]			
0x100	00000000	00000000	-	-	
0x104	OCCP	1[H,W]			
0.104	00000000	0000000	-	<u> </u>	
0x108	OCCP	• • •	-	_	
OX100	00000000				
0x10C	OCCP		-	-	
	00000000				
0x110	OCCP		-	-	
	00000000				
0x114	OCCP		=	-	
	00000000		000040004444	0000440004444	
0x118	-	OCSD10[B,H,W]	OCSB10[B,H,W]	OCSA10[B,H,W]	
		00000000	00000000	00000000	
0x11C	-	OCSD32[B,H,W]	OCSB32[B,H,W]	OCSA32[B,H,W]	
		00000000	00000000	00000000	
0x120	-	OCSD54[B,H,W]	OCSB54[B,H,W]	OCSA54[B,H,W] 00000000	
	-	00000000	00000000 OCSC[B,H,W]	0000000	
0x124		-	000000	-	
			OCSE0	IR H W1	
0x128	=	=	00000000		
		OCSE1			
0x12C		00000000 00000000			
			OCSE2	[B.H.W]	
0x130	-	-	00000000		
		OCSE3			
0x134		00000000 00000000	00000000 00000000		
0.400			OCSE4[B,H,W]		
0x138	-	-	00000000	00000000	
0x13C		OCSE5	[B,H,W]		
UXISC		00000000 00000000	00000000 00000000		
0x140	TCCP	D[H,W]	_	_	
0.8140	11111111	11111111	-	<u>-</u>	
0x144	TCDT	D[H,W]	_		
UX 144	00000000	00000000	- 	-	
0.440	TCSC	D[H,W]	TCSA0[B,H,W]	
0x148	00000000	00000000	00000000	01000000	



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x14C	TCCP		-	-	
	11111111				
0x150	TCDT1[H,W] 00000000 00000000		-	-	
	TCSC		TCSA1[B.H.WI	
0x154	00000000		00000000		
0x158	TCCP2	2[H,W]			
0.136	11111111	11111111	-	<u>-</u>	
0x15C	TCDT2		-	-	
	00000000		TORAGE	DILIMA	
0x160	TCSC2 00000000		TCSA2[00000000		
	0000000		L[W]	0100000	
	00000000 00000000 11111111 11111111 *1				
0x164	-	-	-	- *2	
			T unit0		
			ınit1,unit2		
0x168	-	OCFS54[B,H,W]	OCFS32[B,H,W]	OCFS10[B,H,W]	
		00000000	00000000	00000000	
0x16C	-	-	ICFS32[B,H,W]	ICFS10[B,H,W]	
		A OF OF 41D 11 147	00000000	00000000	
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000	
	ICCPO		0000000	0000000	
0x174	00000000		-	-	
0v470	ICCP1[H,W]				
0x178	00000000	00000000	-	-	
0x17C	ICCP2	2[H,W]	_	<u>-</u>	
	00000000	00000000			
0x180	ICCP3		-	-	
	00000000	0000000	ICCD40ID LLWI	ICCA40ID LLWI	
0x184	-	-	ICSB10[B,H,W]	ICSA10[B,H,W] 00000000	
			ICSB32[B,H,W]	ICSA32[B,H,W]	
0x188			00	00000000	
0v18C	WFTF1	0[H,W]			
0x18C	00000000	00000000	-	-	
0x190	WFTB1		WFTA1		
	00000000		00000000	00000000	
0x194	WFTF3		-	-	
	00000000		NA/ETA O	OU L MA	
0x198	WFTB3 00000000		WFTA32[H,W] 00000000 00000000		
	00000000	0000000	0000000	0000000	



Base_Address	s Register				
+ Address	+3	+2	+1	+0	
0x19C	WFTF5 00000000		-	-	
	WFTB5	54[H,W]	WFTA54[H,W]		
0x1A0	00000000		00000000 00000000		
0x1A4		-	-	WFSA10[B,H,W] 000000 000000	
0x1A8		-	-	WFSA32[B,H,W] 000000 000000	
0x1AC		-	-	WFSA54[B,H,W] 000000 000000	
0x1B0		-	-	WFIR[H,W] 00000000 00000000	
0x1B4		-	-	NZCL[H,W] 00000000 00000000	
0x1B8	ACMP 00000000	0[H,W] 00000000	-	-	
0x1BC	ACMP1[H,W] 00000000 00000000		-	-	
0x1C0	ACMP2[H,W] 00000000 00000000		-	-	
0x1C4	ACMP 00000000	3[H,W] 00000000	-	-	
0x1C8	ACMP 00000000	4[H,W] 00000000	-	-	
0x1CC	ACMP 00000000	5[H,W] 00000000	-	-	
0x1D0	-	-		[B,H,W] 00000000	
0x1D4	-	-	ACSD0[B,H,W] 00000000	ACSC0[B,H,W]	
0x1D8	-	-	ACSD1[B,H,W] 00000000	ACSC1[B,H,W] 00000000	
0x1DC	-	-	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000	
0x1E0	-	-	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000	
0x1E4	-	-	ACSD4[B,H,W] 00000000	ACSC4[B,H,W] 00000000	
0x1E8	-	-	ACSD5[B,H,W]	ACSC5[B,H,W]	
0x1EC-0xFFC	-	-	-	-	



1.8.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

MFT unit0 Base_Address : 0x4002_0000

MFT unit1 Base_Address : 0x4002_1000

MFT unit2 Base_Address : 0x4002_2000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x100	OCCP 00000000		-	-
0x104	OCCP1[H,W] 00000000 00000000		-	-
0x108	OCCP 00000000	2[H,W]	-	-
0x10C		3[H,W]	-	-
0x110	OCCP 00000000	4[H,W]	-	-
0x114	OCCP 00000000	5[H,W] 00000000	-	-
0x118	OCSD10 000000	D[B,H,W] 00000000	OCSB10[B,H,W] 00000000	OCSA10[B,H,W] 00000000
0x11C	OCSD32[B,H,W] 000000 00000000		OCSB32[B,H,W] 00000000	OCSA32[B,H,W] 00000000
0x120	OCSD54[B,H,W] 000000 00000000		OCSB54[B,H,W] 00000000	OCSA54[B,H,W] 00000000
0x124	-	-	OCSC[B,H,W] 000000	-
0x128	-	-	OCSE0[B,H,W] 00000000 00000000	
0x12C			[B,H,W] 00000000 00000000	
0x130	-	-	OCSE2 00000000	[B,H,W] 00000000
0x134			B[B,H,W] 00000000 00000000	
0x138	-	-		[B,H,W] 00000000
0x13C			5[B,H,W] 00000000 00000000	
0x140	TCCP 11111111		-	-
0x144	TCDT(000000000	D[H,W] 00000000	-	-
0x148		0[H,W] 00000000	TCSA0 00000000	
0x14C	TCCP 11111111		-	-



Base_Address		Reg	ister		
+ Address	+3	+2	+1	+0	
0x150	TCDT ² 00000000		-	-	
0x154	TCSC ²	1[H,W]		TCSA1[B,H,W] 00000000 01000000	
0x158	TCCP2	2[H,W]	-	-	
0x15C	TCDT2	2[H,W]	-	-	
0x160	TCSC2	2[H,W]	TCSA2		
		TCA	L[W] 11111111 11111111 *1		
0x164	-	-	-	- *2	
			T unit0 unit1,unit2		
0x168	-	OCFS54[B,H,W]	OCFS32[B,H,W] 00000000	OCFS10[B,H,W]	
0x16C	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000	
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000	
0x174	ICCP0 00000000		-	-	
0x178	ICCP1 00000000		-	-	
0x17C	ICCP2 00000000		-	-	
0x180	ICCP3 00000000		-	-	
0x184	-	-	ICSB10[B,H,W] 00	ICSA10[B,H,W] 00000000	
0x188			ICSB32[B,H,W] 00	ICSA32[B,H,W] 00000000	
0x18C	WFTF1 00000000		-	-	
0x190	WFTB1 00000000		WFTA1 00000000		
0x194	WFTF3 00000000		-	-	
0x198	WFTB3 00000000		WFTA3 00000000		
0x19C	WFTF5 00000000		-	-	





Base_Address		Reg	ister	
+ Address	+3	+2	+1	+0
0x1A0	WFTB5	54[H,W]	WFTA5	54[H,W]
UXTAU	00000000	00000000	00000000 00000000	
0x1A4	_		WFSA10[B,H,W]	
OX 17 (4			000000	000000
0x1A8	-	-	WFSA32	
			000000	
0x1AC	-	-	WFSA54	
			000000	
0x1B0	-	-	WFIR	
			00000000	
0x1B4	-	-	NZCL 00000000	
	A CMD	l 0[H,W]	0000000	0000000
0x1B8	00000000		-	-
	ACMP			
0x1BC	00000000		-	-
	ACMP2[H,W]			
0x1C0	00000000		-	-
	ACMP3[H,W]			
0x1C4	00000000 00000000		-	-
0.400	ACMP	4[H,W]		
0x1C8	00000000 00000000		-	·
0x1CC	ACMP	5[H,W]	_	_
0.100	00000000	00000000		
0x1D0	_	<u>-</u>	ACSA[B,H,W]	
0.1.2.0			00000000 00000000	
0x1D4	-	ACMC0[B,H,W]	ACSD0[B,H,W]	ACSC0[B,H,W]
		000000	00000000	00000000
0x1D8	-	ACMC1[B,H,W]	ACSD1[B,H,W]	ACSC1[B,H,W]
		00000	00000000	00000000
0x1DC	-	ACMC2[B,H,W] 000000	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000
0x1E0	-	ACMC3[B,H,W] 000000	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000
		ACMC4[B,H,W]	ACSD4[B,H,W]	ACSC4[B,H,W]
0x1E4	-	000000	00000000	00000000
		ACMC5[B,H,W]	ACSD5[B,H,W]	ACSC5[B,H,W]
0x1E8	-	000000	00000000	00000000
				TCSD[B,H,W]
0x1EC	-	-	-	00
0x1E0.0xEE0				
0x1F0-0xFFC	-	-	-	-



1.9 PPG

PPG Base_Address: 0x4002_4000

Base_Address		R	Register	
+ Address	+3	+2	+1	+0
0x000	-	-	TTCR0 [B,H,W] 11110000	-
0x004	-	-	-	*
0x008	-	-	COMP0 [B,H,W] 00000000	-
0x00C	-	-	-	COMP2 [B,H,W] 00000000
0x010	-	-	COMP4 [B,H,W] 00000000	-
0x014	-	-	-	COMP6 [B,H,W] 00000000
0x018 - 0x01C	-	-	-	-
0x020	-	-	TTCR1 [B,H,W] 11110000	-
0x024	-	-	-	*
0x028	-	-	COMP1 [B,H,W] 00000000	-
0x02C	-	-	-	COMP3 [B,H,W] 00000000
0x030	-	-	COMP5 [B,H,W] 00000000	-
0x034	-	-	-	COMP7 [B,H,W] 00000000
0x038 - 0x03C	-	-	-	-
0x040	-	-	TTCR2 [B,H,W] 11110000	-
0x044	-	-	-	*
0x048	-	-	COMP8 [B,H,W] 00000000	-
0x04C	-	-	-	COMP10 [B,H,W] 00000000
0x050	-	-	COMP12 [B,H,W] 00000000	-
0x054	-	-	-	COMP14 [B,H,W] 00000000
0x058 - 0x0FC	-	-	-	-
0x100	-	-	00000000	[B,H,W] 00000000
0x104	-	-		[B,H,W] 00000000
0x108 - 0x13C	-	-	- TD04	-
0x140	-	-	0	[B,H,W] 0000000
0x144	-	-		[B,H,W] 0000000
0x148 - 0x1FC	-	-	-	-





Base_Address	Register				
+ Address	+3	+2	+1	+0	
			PPGC0 [B,H,W]	PPGC1 [B,H,W]	
0x200	-	-	00000000	00000000	
			PPGC2 [B,H,W]	PPGC3 [B,H,W]	
0x204	-	=	00000000	00000000	
			PRLH0 [B,H,W]	PRLL0 [B,H,W]	
0x208	-	-	XXXXXXXX	xxxxxxxx	
			PRLH1 [B,H,W]	PRLL1 [B,H,W]	
0x20C	-	-	XXXXXXXX	xxxxxxxx	
			PRLH2 [B,H,W]	PRLL2 [B,H,W]	
0x210	-	-	XXXXXXXX	xxxxxxxx	
			PRLH3 [B,H,W]	PRLL3 [B,H,W]	
0x214	-	-	XXXXXXXX	xxxxxxxx	
				GATEC0 [B,H,W]	
0x218	-	=	-	0000	
0x21C - 0x23C	-	-	-	_	
			PPGC4 [B,H,W]	PPGC5 [B,H,W]	
0x240	-	-	00000000	0000000	
			PPGC6 [B,H,W]	PPGC7 [B,H,W]	
0x244	-	-	00000000	00000000	
			PRLH4 [B,H,W]	PRLL4 [B.H.W]	
0x248	=	-	XXXXXXXX	XXXXXXXX	
			PRLH5 [B,H,W]	PRLL5 [B,H,W]	
0x24C	=	=	XXXXXXXX	XXXXXXXX	
			PRLH6 [B,H,W]	PRLL6 [B,H,W]	
0x250	=	=	XXXXXXXX	XXXXXXXX	
			PRLH7 [B,H,W]	PRLL7 [B,H,W]	
0x254	-	-	XXXXXXXX	XXXXXXXX	
			7000000	GATEC4 [B,H,W]	
0x258	-	-	-	00	
0x25C - 0x27C	-	-	_	-	
ONLOG ONLIG			PPGC8 [B,H,W]	PPGC9 [B,H,W]	
0x280	-	-	00000000	00000000	
			PPGC10 [B,H,W]	PPGC11 [B,H,W]	
0x284	-	-	00000000	00000000	
			PRLH8 [B,H,W]	PRLL8 [B,H,W]	
0x288	-	-	XXXXXXXX	XXXXXXXX	
			PRLH9 [B,H,W]	PRLL9 [B,H,W]	
0x28C	-	-	XXXXXXXX	XXXXXXXX	
			PRLH10 [B,H,W]	PRLL10 [B,H,W]	
0x290	-	-	XXXXXXXX	XXXXXXXX	
			PRLH11 [B,H,W]	PRLL11 [B,H,W]	
0x294	-	-	XXXXXXXX	XXXXXXXX	
			^^^^^		
0x298	-	-	-	GATEC8 [B,H,W]	
0x29C - 0x2BC				0000	
OYTAC - OXTOC	-	-	-	-	
0x2C0	-	-	PPGC12 [B,H,W]	PPGC13 [B,H,W]	
			00000000	0000000	



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0004			PPGC14 [B,H,W]	PPGC15 [B,H,W]	
0x2C4	-	-	00000000	00000000	
0.000			PRLH12 [B,H,W]	PRLL12 [B,H,W]	
0x2C8	-	-	XXXXXXXX	XXXXXXXX	
0.000			PRLH13 [B,H,W]	PRLL13 [B,H,W]	
0x2CC	-	-	XXXXXXXX	XXXXXXXX	
0.000			PRLH14 [B,H,W]	PRLL14 [B,H,W]	
0x2D0	-	-	XXXXXXXX	XXXXXXXX	
0.004			PRLH15 [B,H,W]	PRLL15 [B,H,W]	
0x2D4	-	-	XXXXXXXX	XXXXXXXX	
0.000				GATEC12 [B,H,W]	
0x2D8	-	-	-	00	
0x2DC - 0x2FC	-	-	-	-	
0202			PPGC16 [B,H,W]	PPGC17 [B,H,W]	
0x300	<u>-</u> _	-	0000000	00000000	
0.204			PPGC18 [B,H,W]	PPGC19 [B,H,W]	
0x304	-	-	00000000	00000000	
0.000			PRLH16 [B,H,W]	PRLL16 [B,H,W]	
0x308	-	-	XXXXXXXX	XXXXXXXX	
0.000			PRLH17 [B,H,W]	PRLL17 [B,H,W]	
0x30C	-	-	XXXXXXXX	XXXXXXXX	
0.040			PRLH18 [B,H,W]	PRLL18 [B,H,W]	
0x310	-	-	XXXXXXXX	XXXXXXXX	
0.044			PRLH19 [B,H,W]	PRLL19 [B,H,W]	
0x314	-	-	XXXXXXXX	XXXXXXXX	
0.040				GATEC16 [B,H,W]	
0x318	-	-	-	0000	
0x31C - 0x33C	-	-	-	-	
0.040			PPGC20 [B,H,W]	PPGC21 [B,H,W]	
0x340	-	-	00000000	00000000	
0.044			PPGC22 [B,H,W]	PPGC23 [B,H,W]	
0x344	-	-	00000000	00000000	
0240			PRLH20 [B,H,W]	PRLL20 [B.H.W]	
0x348	-	-	XXXXXXXX	XXXXXXXX	
0.040			PRLH21 [B,H,W]	PRLL21 [B,H,W]	
0x34C	<u>-</u> _	-	XXXXXXXX	XXXXXXXX	
0250			PRLH22 [B,H,W]	PRLL22 [B,H,W]	
0x350	<u>-</u> _	-	XXXXXXXX	XXXXXXXX	
0,425.4			PRLH23 [B,H,W]	PRLL23 [B,H,W]	
0x354	<u>-</u> _	-	XXXXXXXX	XXXXXXXX	
0.050				GATEC20 [B,H,W]	
0x358	-	-	-	00	
0x35C - 0x37C	-	-	-	-	
0x380	-	-	-	-	
0x384 - 0xFFC	-		-	_	



1.10 Base Timer

Base Timer ch.0 Base Address: 0x4002 5000 Base Timer ch.1 Base Address: 0x4002 5040 Base Timer ch.2 Base Address : 0x4002_5080 Base Timer ch.3 Base Address: 0x4002_50C0 Base Timer ch.4 Base Address: 0x4002 5200 Base Timer ch.5 Base Address: 0x4002_5240 Base Timer ch.6 Base Address: 0x4002_5280 Base Address: 0x4002_52C0 Base Timer ch.7 Base Timer ch.8 Base Address: 0x4002 5400 Base Timer ch.9 Base Address: 0x4002_5440 Base Timer ch.10 Base Address: 0x4002_5480 Base Timer ch.11 Base Address: 0x4002 54C0 Base Timer ch.12 Base Address: 0x4002 5600 Base Timer ch.13 Base Address: 0x4002 5640 Base Timer ch.14 Base Address: 0x4002_5680 Base Timer ch.15 Base Address: 0x4002 56C0

Base_Address	dress Register			
+ Address	ess +3 +2 +1		+0	
0x000			PCSR/PRLL [H,W]	
0x000	•	-	XXXXXXXX	XXXXXXX
0x004			PDUT/PRLH	/DTBF [H,W]
0x004	•	-	XXXXXXXX XXXXXXXX	
0x008			TMR [H,W]	
0x006	-	-	00000000 00000000	
0x00C			TMCR	[B,H,W]
00000	•	-	-0000000	00000000
0x010			TMCR2 [B,H,W]	STC [B,H,W]
0.010	-	-	00	0000-000
0x014 - 0x03C	-	-	-	-



1.11 IO Selector for Base Timer

IO Selector for ch.0-ch.3 (Base Timer) Base Address: 0x4002_5100

Base_Address		Reg	ister	
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL0123 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7(Base Timer)Base Address: 0x4002_5300

Base_Address		Reg	ister	
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL4567 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.8-ch.11(Base Timer) Base Address : 0x4002_5500

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL89AB [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.12-ch.15(Base Timer) Base Address : 0x4002_5700

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSELCDEF [B,H,W] 00000000	-
0x004 - 0x0FC	=	-	-	-

Software-based Simultaneous Startup(Base Timer) Base Address: 0x4002_5F00

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR [B,H,W] XXXXXXXX XXXXXXX	



1.12 QPRC

1.12.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products

 QPRC ch.0
 Base Address : 0x4002_6000

 QPRC ch.1
 Base Address : 0x4002_6040

 QPRC ch.2
 Base Address : 0x4002_6080

 QPRC ch.3
 Base Address : 0x4002_60C0

Base_Address		R	Register			
+ Address	+3	+2	+1	+0		
0x0000			QPCR	[H,W]		
0.0000	-	-	00000000	0000000		
0x0004	_	_	QRCR	? [H,W]		
0,0004			00000000	0000000		
0x0008	_	_	QPCCI	R [H,W]		
0,0000			00000000	00000000		
0x000C	_		QPRCI	R [H,W]		
0.0000			00000000	00000000		
0x0010	_	_	QMPR	R [H,W]		
0,0010			11111111	11111111		
0x0014	_	_	QICRH [B,H,W]	QICRL [B,H,W]		
0,0014			000000	00000000		
0x0018	_	_	QCRH [B,H,W]	QCRL [B,H,W]		
0,0010			00000000	00000000		
0x001C	_	_	QECR	[B,H,W]		
0,0010				000		
0x0020 -	_	_	_	_		
0x003B						
0x003C	QPCRR	[B,H,W]	QRCRR	2[B,H,W]		
0,0000	00000000	00000000	00000000	00000000		



1.12.2 TYPE3-M4, TYPE4-M4, TYPE5-M4 Products

 QPRC ch.0
 Base Address : 0x4002_6000

 QPRC ch.1
 Base Address : 0x4002_6040

 QPRC ch.2
 Base Address : 0x4002_6080

 QPRC ch.3
 Base Address : 0x4002_60C0

Base_Address	Register			
+ Address	+3	+2	+1	+0
0000	-	-	QPCR [H,W]	
0x0000			00000000 00000000	
0x0004			QRCR [H,W]	
		-	00000000 00000000	
0x0008		QPCCR [H,W]		
	-	-	00000000	00000000 00000000
0000			QPRCR [H,W]	
0x000C		-	00000000 00000000	
0x0010	-	-	QMPR [H,W]	
000010			11111111 11111111	
0x0014	-	-	QICRH [B,H,W]	QICRL [B,H,W]
0x0014			000000	00000000
0x0018	-	-	QCRH [B,H,W]	QCRL [B,H,W]
000018			00000000	00000000
0x001C			QECR [B,H,W]	
000010	-	-	0000	
0x0020 -				
0x003B	-	<u>-</u>		-
0x003C	QPCRR[B,H,W]		QRCRR[B,H,W]	
0,0000	00000000 00000000		00000000 00000000	



1.13 QPRC NF

 QPRC ch.0 NF
 Base Address: 0x4002_6100

 QPRC ch.1 NF
 Base Address: 0x4002_6110

 QPRC ch.2 NF
 Base Address: 0x4002_6120

 QPRC ch.3 NF
 Base Address: 0x4002_6130

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000	-	-	-	NFCTLA[B,H,W] 00-000
0x0004	-	-	-	NFCTLB[B,H,W] 00-000
0x0008	-	-	-	NFCTLZ[B,H,W] 00-000
0x000C	-	-	-	-



1.14 A/DC

 12bit A/DC unit0
 Base_Address : 0x4002_7000

 12bit A/DC unit1
 Base_Address : 0x4002_7100

 12bit A/DC unit2
 Base_Address : 0x4002_7200

Base_Address	Register						
+ Address	+3	+2	+1	+0			
0.000			ADCR[B,H,W]	ADSR[B,H,W]			
0x000	-	-	000-0000	00000			
0x004	-	-	-	*			
			SCCR[B,H,W]	SFNS[B,H,W]			
800x0	-	-	1000-000	0000			
0.000	SCFD[B,H,W]						
0x00C		XXXXXXXX XXXX1XXXXXXX					
0040			SCIS3[B,H,W]	SCIS2[B,H,W]			
0x010	-	-	00000000	00000000			
0::04.4			SCIS1[B,H,W]	SCIS0[B,H,W]			
0x014	-	-	00000000	00000000			
0040			PCCR[B,H,W]	PFNS[B,H,W]			
0x018	-	-	10000000	XX00			
0040		PCFD	[B,H,W]				
0x01C		XXXXXXXX XXXX	1-XXXXXXXX				
0,000		_		PCIS[B,H,W]			
0x020	•	-	-	00000000			
0004	CMPD[B,H,W]			CMPCR[B,H,W]			
0x024	0000000	0000000 00		00000000			
0,000			ADSS3[B,H,W]	ADSS2[B,H,W]			
0x028	<u>-</u>	-	00000000	00000000			
0x02C	-	-	ADSS1[B,H,W]	ADSS0[B,H,W]			
UXU2C			00000000	00000000			
0000			ADST0[B,H,W]	ADST1[B,H,W]			
0x030	-	-	00010000	00010000			
0:-004				ADCT[B,H,W]			
0x034	-	-	-	00000111			
0020			SCTSL[B,H,W]	PRTSL[B,H,W]			
0x038	-	-	0000	0000			
0.000			ADCEN	[B,H,W]			
0x03C	-	-	11111111	100			
0x040	CALSR[B,H,W]						
0,040	0 00000000						
0x044	_	_	_	WCMRCIF[B,H,W]			
UAU44	_	-		00000000			
0x048	_	_	_	WCMRCOT [B,H,W]			
07070			_	00000000			
0x04C	_	_	WCMPSR[B,H,W]	WCMPCR[B,H,W]			
0,040	-		00000000 00100000				
0x050	WCMPDH[B,H,W]		WCMPDL[B,H,W]				
	00000000	00000000	00000000	00000000			
0x040 - 0x0FC	=	-	-	-			



1.15 CR Trim

CR Trim Base_Address : 0x4002_E000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0000	-	-	-	MCR_PSR[B,H,W]
0x000				001
0x004	-	-	MCR_FTRM[B,H,W]	
0x004			01 11101111	
0,4008	-	-		MCR_TTRM[B,H,W]
0x008			-	10000
0000	MCR_RLR[W] 00000000 00000000 000000001			
0x00C				
0x010 - 0x0FC	-	-	-	-



1.16 EXTI

1.16.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE4-M4 Products

EXTI Base_Address: 0x4003_0000

Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x000	ENIR[B,H,W]					
	00000000 00000000 00000000 00000000					
0,004		EIRR[B,H,W]				
0x004						
0,,000		EICL[B,H,W]				
0x008		11111111 11111111 11111111				
ELVR[B,H,W]						
0x00C		00000000 00000000 00000000 00000000				
0,010	ELVR1[B,H,W]					
00010	0x010 00000000 00000000 00000000 00000000					
0x014	-	-	-	NMIRR[B,H,W]		
0X014				0		
0x018				NMICL[B,H,W]		
03018	-	-	-	1		
0x01C	-					
0x020 - 0x0FC	-	-	-	-		

1.16.2 TYPE5-M4, TYPE6-M4 Products

EXTI Base_Address: 0x4003_0000

Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x000	ENIR[B,H,W]					
		0000000 00000000 00000000				
0.004		EIRR[B,H,W]				
0x004		XXXXXXX XXXXXXXX XXXXXXX XXXXXXX				
0x008 EICL[B,H,W]						
0.000		11111111 11111111 111111111				
0x00C ELVR[B,H,W] 00000000 00000000 000000000						
0x010	ELVR1[B,H,W]					
0.010		00000000 000000000 000000000				
0x014				NMIRR[B,H,W]		
	-		-	0		
0x018	_	_	_	NMICL[B,H,W]		
0x016				1		
0x01C	ELVR2[B,H,W]					
0.010	00000000 00000000 000000000					
0x020 - 0x0FC	-					



1.17 INT-Req. READ

1.17.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products

INT-Req. READ Base_Address : 0x4003_1000

Base_Address		Reg	gister	
+ Address	+3	+2	+1	+0
0,000		DRQSE	EL[B,H,W]	
0x000	00000000 00000000 00000000 00000000			
0x004 - 0x00C			-	
0x010	_			ODDPKS[B]
0.010	<u>-</u>	_	_	00000
0x014	-	-	-	-
0x018	-	*	-	*
0x01C - 0x10C	-	-	-	-
0x110			SEL[B,H,W]	
JA		00000000	00000000	
0x114			SEL[B,H,W]	
		00000000	00000000	
0x118			SEL[B,H,W]	
-			00000000	
0x11C			SEL[B,H,W]	
			00000000	
0x120			SEL[B,H,W]	
			00000000	
0x124	IRQ008SEL[B,H,W]			
			00000000	
0x128	IRQ009SEL[B,H,W]			
			00000000	
0x12C			SEL[B,H,W]	
		00000000	00000000	T
0x130 – 0x1FC	-		-	-
0x200			MON[B,H,W]	
			00	
0x204			//ON[B,H,W] 0	
			0 MON[B,H,W]	
0x208			0	
			MON[B,H,W]	
0x20C			0	
	IRQ003MON[B,H,W]			
0x210	00000000			
	IRQ004MON[B,H,W]			
0x214			00000000	
0v219		IRQ005N	MON[B,H,W]	
0x218			00000000	



Address 43 42 41 40	Base_Address		Register			
0x21C		+3		+0		
0x220 IRQ007MON[B.H.W]	0v21C		IRQ006MON[B,H,W]			
0x224	UXZIC		00000000			
IRQ008MON[B,HW]	0v220					
0x224	0,220		00000000			
IRQ009MON(B,H,W]	0×224					
0x22E IRQ010MON[B,H,W] 0x230 IRQ011MON[B,H,W] 0x234 IRQ012MON[B,H,W] 0x238 IRQ013MON[B,H,W] 0x23C IRQ014MON[B,H,W] 0x240 IRQ015MON[B,H,W] 0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x249 IRQ018MON[B,H,W] 0x240 IRQ019MON[B,H,W] 0x241 IRQ019MON[B,H,W] 0x242 IRQ019MON[B,H,W] 0x243 IRQ019MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x251 IRQ020MON[B,H,W] 0x252 IRQ021MON[B,H,W] 0x254 IRQ021MON[B,H,W] 0x255 IRQ022MON[B,H,W] 0x260 IRQ022MON[B,H,W] 0x261 IRQ022MON[B,H,W] 0x262 IRQ025MON[B,H,W] 0x263 IRQ025MON[B,H,W] 0x264 IRQ025MON[B,H,W] 0x265 IRQ025MON[B,H,W] 0x266 IRQ025MON[B,H,W] 0x270 IRQ025MON[B,H,W] 0x274 IRQ025MON[B,H,W]	0,224		00000000			
Dx22C IRQ010MON[B,H,W]	0v228					
0x22C	UNZZU					
	0x22C					
0x234 IRQ012MON[B,H,W] 0x238 IRQ013MON[B,H,W] 0x23C IRQ014MON[B,H,W] 0x240 IRQ015MON[B,H,W] 0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x24C IRQ013MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ022MON[B,H,W] 0x264 IRQ023MON[B,H,W] 0x265 IRQ024MON[B,H,W] 0x266 IRQ025MON[B,H,W] 0x267 IRQ025MON[B,H,W] 0x268 IRQ027MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ029MON[B,H,W] 0x278 IRQ029MON[B,H,W]	0,		00000000			
0x234 IRQ012MON[B,H,W]	0x230		- · · · · -			
0x238	0,200		0			
0x238	0,224		IRQ012MON[B,H,W]			
0x23C IRQ014MON[B,H,W] 0x240 IRQ015MON[B,H,W] 0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x26C IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]	UX234		0			
			IRQ013MON[B,H,W]			
0x240 0x240 IRQ015MON[B,H,W] 0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x270 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W]	0x238		0			
0x240 0x240 IRQ015MON[B,H,W] 0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x270 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W]			IRQ014MON[B.H.W]			
IRQ015MON[B,H,W]	0x23C		• • • •			
0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ022MON[B,H,W] 0x264 IRQ023MON[B,H,W] 0x268 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x260 IRQ025MON[B,H,W] 0x261 IRQ026MON[B,H,W] 0x262 IRQ026MON[B,H,W] 0x263 IRQ027MON[B,H,W] 0x264 IRQ027MON[B,H,W] 0x265 IRQ028MON[B,H,W] 0x266 IRQ028MON[B,H,W] 0x270 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]						
0x244 IRQ016MON[B,H,W] 0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x254 IRQ021MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]	0x240		• • •			
0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x258 IRQ022MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x260 IRQ026MON[B,H,W] 0x261 IRQ026MON[B,H,W] 0x262 IRQ026MON[B,H,W] 0x263 IRQ026MON[B,H,W] 0x264 IRQ026MON[B,H,W] 0x270 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]						
0x248 IRQ017MON[B,H,W] 0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x254 IRQ021MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]	0x244		- · · · · · · -			
0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254			•			
0x24C IRQ018MON[B,H,W] 0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]	0x248		• • • •			
0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x260 IRQ026MON[B,H,W] 0x261 IRQ025MON[B,H,W] 0x262 IRQ026MON[B,H,W] 0x263 IRQ026MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]						
0x250 IRQ019MON[B,H,W] 0x254 IRQ020MON[B,H,W] 0x258 IRQ022MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x265 IRQ023MON[B,H,W] 0x266 IRQ025MON[B,H,W] 0x267 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x260 IRQ026MON[B,H,W]	0x24C		IRQ018MON[B,H,W]			
0x254 IRQ020MON[B,H,W] 0x254 IRQ021MON[B,H,W] 0x258 IRQ021MON[B,H,W] 0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]	UNZ-10		0			
0x254 IRQ020MON[B,H,W]	0×250		IRQ019MON[B,H,W]			
0x254	0,250		000000			
0x258	0.054		IRQ020MON[B,H,W]			
0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]	0x254		000000			
0x25C IRQ022MON[B,H,W] 0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278 IRQ029MON[B,H,W]			IRQ021MON[B,H,W]			
0x260 0x260 IRQ023MON[B,H,W]	0x258		0000			
0x260 0x260 IRQ023MON[B,H,W]			IRQ022MON[B.H.W]			
0x260 IRQ023MON[B,H,W] 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278	0x25C					
0x264 0x264 IRQ024MON[B,H,W] 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278						
0x264	0x260					
0x264 0x268 IRQ025MON[B,H,W] 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278						
0x268	0x264					
0x268 0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W] 000000 IRQ028MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x278						
0x26C IRQ026MON[B,H,W] 0x270 IRQ027MON[B,H,W]	0x268					
0x26C 0x270 IRQ027MON[B,H,W] 0x274 IRQ028MON[B,H,W] 0x274 IRQ029MON[B,H,W]						
0x270	0x26C					
0x270	5.250		0000			
0x274 IRQ029MON[B,H,W] 0x278	0x270	IRQ027MON[B,H,W]				
0x274000 0x278 IRQ029MON[B,H,W]	0,210	• • • •				
0x278	0.274		IRQ028MON[B,H,W]			
UX278	UX2/4		000			
UX278			IRQ029MONIB.H.W1			
	0x278		000			



Base_Address	Register Register						
+ Address	+3	+2 +1	+0				
0x27C		IRQ030MON[B,H,W]					
	0000						
0x280		IRQ031MON[B,H,W]					
0x284		IRQ032MON[B,H,W]					
		000					
0x288		IRQ033MON[B,H,W]					
		000 IRQ034MON[B,H,W]					
0x28C		0000					
		IRQ035MON[B,H,W]					
0x290		00000					
		IRQ036MON[B,H,W]					
0x294		000					
		IRQ037MON[B,H,W]					
0x298		000					
0000		IRQ038MON[B,H,W]					
0x29C		000					
0×240		IRQ039MON[B,H,W]					
0x2A0		00					
0x2A4		IRQ040MON[B,H,W]					
UNE/ (4		00					
0x2A8		IRQ041MON[B,H,W]					
		00					
0x2AC		IRQ042MON[B,H,W]					
		00					
0x2B0		IRQ043MON[B,H,W] 00					
		IRQ044MON[B,H,W]					
0x2B4		00					
		IRQ045MON[B,H,W]					
0x2B8		00					
		IRQ046MON[B,H,W]					
0x2BC		00					
0.000		IRQ047MON[B,H,W]					
0x2C0		00					
0v2C4		IRQ048MON[B,H,W]					
0x2C4		0					
0x2C8		IRQ049MON[B,H,W]					
0,200		0					
0x2CC		IRQ050MON[B,H,W]					
5200	0						
0x2D0	IRQ051MON[B,H,W]						
	0						
0x2D4		IRQ052MON[B,H,W] 0					
		 IRQ053MON[B,H,W]					
0x2D8		0					



Base_Address Register						
+ Address	+3 +2 +1 +0					
0x2DC	IRQ054MON[B,H,W] 0					
0x2E0	IRQ055MON[B,H,W]					
UXZEU			0			
0x2E4			ON[B,H,W] 0			
0x2E8			ON[B,H,W] 0			
0x2EC		IRQ058Me	ON[B,H,W] 0			
0x2F0		IRQ059M	ON[B,H,W] 0000			
0x2F4		IRQ060Me	ON[B,H,W] 0			
0x2F8		IRQ061M	ON[B,H,W]			
0/12.0						
0x2FC			ON[B,H,W] 0			
0x300			ON[B,H,W]			
			00			
0x304			ON[B,H,W] 0			
0x308		IRQ065MON[B,H,W] 00				
0x30C			ON[B,H,W] 0			
0x310			ON[B,H,W] 00			
0x314		IRQ068Me	ON[B,H,W] 0			
0x318		IRQ069Me	ON[B,H,W] 00			
0x31C		IRQ070M	ON[B,H,W] 0			
0x320		IRQ071M	ON[B,H,W] 00			
0x324		IRQ072M	ON[B,H,W] 0			
0x328		IRQ073M	ON[B,H,W]			
0x32C	00 IRQ074MON[B,H,W] 0					
0x330	IRQ075MON[B,H,W] 00					
0x334		IRQ076M	ON[B,H,W] 			
0x338		IRQ077M	ON[B,H,W] 			



Base_Address	Register						
+ Address	+3	+2 +1	+0				
0x33C		IRQ078MON[B,H,W]					
0x340		IRQ079MON[B,H,W]					
		000000					
0x344		IRQ080MON[B,H,W] 0					
		IRQ081MON[B,H,W]					
0x348		0					
0x34C		IRQ082MON[B,H,W]					
0x34C		000					
0x350		IRQ083MON[B,H,W]					
		0					
0x354		IRQ084MON[B,H,W] 0					
		IRQ085MON[B,H,W]					
0x358		0					
		IRQ086MON[B,H,W]					
0x35C		0					
0,260		IRQ087MON[B,H,W]					
0x360		0					
0x364		IRQ088MON[B,H,W]					
		0					
0x368		IRQ089MON[B,H,W]					
		0 IRQ090MON[B,H,W]					
0x36C		0					
		IRQ091MON[B,H,W]					
0x370		00					
0x374		IRQ092MON[B,H,W]					
0,074		0000					
0x378		IRQ093MON[B,H,W]					
0x37C		IRQ094MON[B,H,W] 0000					
		IRQ095MON[B,H,W]					
0x380		0000					
0.204		IRQ096MON[B,H,W]					
0x384		000000					
0x388		IRQ097MON[B,H,W]					
0x38C	IRQ098MON[B,H,W]						
		00 IRQ099MON[B,H,W]					
0x390		00					
0v204		IRQ100MON[B,H,W]					
0x394		00					
0x398		IRQ101MON[B,H,W]					
		00					



Base_Address	Register			
+ Address	+3	+2	+1	+0
0x39C			ON[B,H,W]	
0,000	00			
0x3A0			ON[B,H,W]	
			0 ON[B,H,W]	
0x3A4			00	
0.040		IRQ105M0	ON[B,H,W]	
0x3A8			0	
0x3AC			ON[B,H,W]	
oxor to			00	
0x3B0		IRQ107M0	ON[B,H,W] 0	
			ON[B,H,W]	
0x3B4			00	
0.000			ON[B,H,W]	
0x3B8			0	
0x3BC			ON[B,H,W]	
0.020			00	
0x3C0			ON[B,H,W]	
0x3C4	<u>-</u>		00000	-
0.504	<u> </u>		 ON[B,H,W]	-
0x3C8			00000	
0x3CC		IRQ114M0	ON[B,H,W]	
UXSCC			000000	
0x3D0 – 0x3D8	-	-	-	-
0x3DC			ON[B,H,W]	
			00 N[B,H,W]	
0x3E0			0	
0.054		IRQ120M0	ON[B,H,W]	
0x3E4			0	
0x3E8		IRQ121M		
			00	
0x3EC			ON[B,H,W] 0	
0x3F0		IRQ123MON[B,H,W] 00		
0x3F4		IRQ124MON[B,H,W]		
UASE4		0		
0x3F8	IRQ125MON[B,H,W]			
	00			
0x3FC	IRQ126MON[B,H,W] 0			
			ON[B,H,W]	
0x400			00	
0x404 – 0xFFC	-	-	-	-



1.17.2 TYPE3-M4, TYPE5-M4 Product

INT-Req. READ Base_Address : 0x4003_1000

Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x000		DRQSE	L[B,H,W]		
0,000	00000000 00000000 000000000				
0x004 - 0x00C			<u>-</u>		
0x010	_	_	_	ODDPKS[B]	
0.010		_	_	00000	
0x014	_	_	_	ODDPKS1[B]	
0.014	-		_	00000	
0x018	-	*	-	*	
0x01C - 0x10C	-	-	-	-	
0x110		IRQ003S	EL[B,H,W]		
0.7110		00000000	00000000		
0x114		IRQ004S	EL[B,H,W]		
0.7114		00000000	00000000		
0x118		IRQ005S	EL[B,H,W]		
0.110		00000000	00000000		
0x11C		IRQ006S	EL[B,H,W]		
OXTIC		00000000	00000000		
0x120		IRQ007S	EL[B,H,W]		
0.120		00000000	00000000		
0x124		IRQ008S	EL[B,H,W]		
OXIZT		00000000	00000000		
0x128		IRQ009S	EL[B,H,W]		
0.120	00000000 00000000				
0v42C		IRQ010S	EL[B,H,W]		
0x12C		00000000	00000000		
0x130 - 0x1FC	-	-	-	-	
0.000	EXC02MON[B,H,W]				
0x200			00		
		IRQ000M	ON[B,H,W]		
0x204			0		
		IRQ001M	ON[B,H,W]		
0x208			0		
		IRQ002M	ON[B,H,W]		
0x20C			0		
	IRQ003MON[B,H,W]				
0x210	00000000				
	IRQ004MON[B,H,W]				
0x214			0000000		
0x218			ON[B,H,W]		
	00000000				



Base_Address	Register						
+ Address	+3	+2	+1	+0			
0x21C		IRQ006MON[B,H,W]					
0,210		00000000					
0x220			ION[B,H,W]				
			00000000				
0x224			ION[B,H,W]				
			00000000				
0x228			1ON[B,H,W]				
			00000000				
0x22C			10N[B,H,W] 0000000				
			ION[B,H,W]				
0x230			·0				
			1ON[B,H,W]				
0x234			·0				
		IRQ013M	ION[B,H,W]				
0x238			0				
2 222		IRQ014M	ION[B,H,W]				
0x23C			0				
0v240		IRQ015MON[B,H,W]					
0x240		0					
0x244		IRQ016MON[B,H,W]					
UNE TH			0				
0x248			ION[B,H,W]				
			0				
0x24C			ION[B,H,W]				
			0				
0x250		IRQ019MON[B,H,W] 000000					
0x254			10N[B,H,W] 00000				
			ION[B,H,W]				
0x258			0000				
		IRQ022M	ION[B,H,W]				
0x25C			0000				
		IRQ023MON[B,H,W]					
0x260			0000				
IRQ024MON[B,H,W]							
UXZ64	0x264000						
0x268		IRQ025M	ION[B,H,W]				
0,200			000				
0x26C			ION[B,H,W]				
0,1200			0000				



Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0,270		IRQ027MON[B,H,W]					
0x270	000000						
0x274		IRQ028N	MON[B,H,W]				
0,274			000				
0x278		IRQ029N	MON[B,H,W]				
0,270			000				
0x27C		IRQ030N	MON[B,H,W]				
UAZ I O			0000				
0x280			MON[B,H,W]				
			000000				
0x284			MON[B,H,W]				
			000				
0x288		IRQ033N	MON[B,H,W]				
			000				
0x28C			MON[B,H,W]				
0x290			MON[B,H,W]				
			000000				
0x294			MON[B,H,W]				
			000				
0x298		IRQ037MON[B,H,W]					
			000				
0x29C			MON[B,H,W] 				
0x2A0			//ON[B,H,W] 00				
0x2A4		IRQ040MON[B,H,W] 00					
			ION[B,H,W]				
0x2A8			·00				
		IRQ042M	ION[B,H,W]				
0x2AC			00				
		IRQ043M	ION[B.H.W]				
0x2B0		IRQ043MON[B,H,W] 00					
		IRQ044MON[B,H,W]					
0x2B4	00						
0.000	IRQ045MON[B,H,W]						
0x2B8	B800						
0050		IRQ046N	ION[B,H,W]				
0x2BC			00				
0000		IRQ047M	ION[B,H,W]				
0x2C0			00				



Base_Address	Register						
+ Address	+3 +2 +1 +0						
0x2C4		IRQ048MON[B,H,W]					
	0						
0x2C8	IRQ049MON[B,H,W]						
			0				
0x2CC			ON[B,H,W]				
			ONITE 1 1 14/1				
0x2D0			ON[B,H,W] 0				
			ON[B,H,W]				
0x2D4			·0				
			ON[B,H,W]				
0x2D8			·0				
		IRQ054M	ON[B,H,W]				
0x2DC			0				
0.050		IRQ055M	ON[B,H,W]				
0x2E0			0				
0v2E4		IRQ056M	ON[B,H,W]				
0x2E4		0					
0x2E8		IRQ057M	ON[B,H,W]				
UXZLU	0						
0x2EC	IRQ058MON[B,H,W]						
5/125			0				
0x2F0			ON[B,H,W]				
0x2F4			ON[B,H,W] 0				
			ON[B,H,W]				
0x2F8			00				
0x2FC	IRQ062MON[B,H,W] 0						
		IRQ063M	ON[B,H,W]				
0x300			00				
0.001		IRQ064M	ON[B,H,W]				
0x304			0				
0×208		IRQ065M	ON[B,H,W]				
0x308			00				
0x30C IRQ066MON[B,H,W]							
0,000			0				
0x310		IRQ067M	ON[B,H,W]				
5,70.10			00				
0x314			ON[B,H,W]				
			0				





Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x318		IRQ069MON[B,H,W]					
0.516	00						
0x31C			ON[B,H,W]				
			0				
0x320			ON[B,H,W]				
			00				
0x324			ON[B,H,W] 0				
0x328			ON[B,H,W] 00				
			ON[B,H,W]				
0x32C			·0				
		IRQ075M	ON[B,H,W]				
0x330			00				
		IRQ076M	ON[B,H,W]				
0x334							
0x338		IRQ077M	ON[B,H,W]				
0x336							
0x33C		IRQ078M	ON[B,H,W]				
0.000							
0x340		IRQ079MON[B,H,W]					
			000000				
0x344			ON[B,H,W]				
			ONED 1174				
0x348			ON[B,H,W] 				
			ON[B,H,W]				
0x34C			000				
		IRQ083M	ONIB.H.W1				
0x350		IRQ083MON[B,H,W] 0					
0054		IRQ084M	ON[B,H,W]				
0x354			0				
0x358		IRQ085M	ON[B,H,W]				
0,000			0				
0x35C			ON[B,H,W]				
			0				
0x360	IRQ087MON[B,H,W]						
		0					
0x364			ON[B,H,W] 0				
0x368			ON[B,H,W] 0				
		0					



Base_Address	Register						
+ Address	+3	+2	+1	+0			
0x36C		IRQ090MON[B,H,W]					
UXSOC		0					
0x370		IRQ091MON[B,H,W]					
0.0.0			00				
0x374			ON[B,H,W]				
0x378			ON[B,H,W]				
			0000				
0x37C			ON[B,H,W] 				
			ON[B,H,W]				
0x380			0000				
			ON[B,H,W]				
0x384			000000				
			ON[B,H,W]				
0x388			000000				
0.200		IRQ098M	ON[B,H,W]				
0x38C			00				
0x390		IRQ099M	ON[B,H,W]				
0,0390			00				
0x394		IRQ100MON[B,H,W]					
chec :			00				
0x398			ON[B,H,W]				
			00				
0x39C			ON[B,H,W]				
			00				
0x3A0			ON[B,H,W] 0				
			ON[B,H,W]				
0x3A4			00				
		IRQ105M	ON[B,H,W]				
0x3A8			·0				
2 24 2		IRQ106M	ON[B,H,W]				
0x3AC			00				
Ovabo		IRQ107M	ON[B,H,W]				
0x3B0			0				
0x3B4	IRQ108MON[B,H,W]						
0,004			00				
0x3B8			ON[B,H,W]				
			0				
0x3BC			ON[B,H,W]				
00							





Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x3C0	IRQ111MON[B,H,W]					
0.300	00000					
0x3C4		IRQ112M	MON[B,H,W]			
0,001						
0x3C8			MON[B,H,W]			
0,000						
0x3CC		IRQ114M	ION[B,H,W]			
UXSCC			0000000			
0x3D0		IRQ115M	MON[B,H,W]			
OXSDO			000			
0x3D4		IRQ116M	MON[B,H,W]			
0,021						
0x3D8			ION[B,H,W]			
			00			
0x3DC	IRQ118MON[B,H,W]					
	00					
0x3E0	IRQ119MON[B,H,W]					
	0					
0x3E4		IRQ120MON[B,H,W]				
		0				
0x3E8			MON[B,H,W]			
			00			
0x3EC			MON[B,H,W]			
		0				
0x3F0			MON[B,H,W]			
			00			
0x3F4			10N[B,H,W] 0			
0x3F8	IRQ125MON[B,H,W]					
		00				
0x3FC			10N[B,H,W] 0			
0x400			10N[B,H,W] 00			
0x404 – 0xFFC	T		1			
UA+U4 - UXFFC						



1.17.3 TYPE4-M4 Product

INT-Req. READ Base_Address : 0x4003_1000

s Register				
+3	+2	+1	+0	
	DRQSE	L[B,H,W]		
00000000 000000000 000000000 000000000				
		-		
			ODDPKS[B]	
-	-	-	00000	
			ODDPKS1[B]	
-	-	-	00000	
-	*	-	*	
-	-	-	-	
	IRQ0038	SEL[B,H,W]		
	0000000 0000000	00 00000000		
	IRQ0045	SEL[B,H,W]		
	00000000 0000000	00 00000000		
	IRQ0055	SEL[B,H,W]		
	0000000 0000000	00 00000000		
	IRQ0065	SEL[B,H,W]		
	0000000 0000000	00 00000000		
IRQ007SEL[B,H,W]				
00000000 00000000 00000000				
IRQ008SEL[B,H,W]				
00000000 00000000 00000000				
IRQ009SEL[B,H,W]				
	0000000 0000000	00 00000000		
	IRQ0105	SEL[B,H,W]		
	0000000 0000000	00 00000000		
-	-	-	-	
EXC02MONIB.H.WI				
	IRQ000M	ION[B,H,W]		
	IRQ001M	ION[B,H,W]		
	IRQ002M	MON[B.H.W]		
		0000000		
		#3 #2 DRQSE	+3	





Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x21C	IRQ006MON[B,H,W]					
0,210	00000000					
0x220		IRQ007N	MON[B,H,W]			
OALLO			00000000			
0x224			ION[B,H,W]			
			00000000			
0x228			MON[B,H,W]			
			00000000			
0x22C			10N[B,H,W] 0000000			
			1ON[B,H,W]			
0x230			·0			
		IRQ012N	MON[B,H,W]			
0x234			·0			
0::000		IRQ013N	ION[B,H,W]			
0x238			0			
0x23C		IRQ014MON[B,H,W]				
0,230		0				
0x240	IRQ015MON[B,H,W]					
		0				
0x244	IRQ016MON[B,H,W]					
		0				
0x248		IRQ017MON[B,H,W] 0				
0x24C			10N[B,H,W] 0			
			MON[B,H,W]			
0x250			000000			
		IRQ020N	MON[B,H,W]			
0x254			000000			
0x258		IRQ021N	MON[B,H,W]			
0x256			0000			
0x25C		IRQ022N	MON[B,H,W]			
UNZUU						
0x260			ION[B,H,W]			
		0000				
0x264	IRQ024MON[B,H,W]					
	000					
0x268			10N[B,H,W] 000			
			 MON[B,H,W]			
0x26C			0000			
	<u> </u>					



Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x270		IRQ027MON[B,H,W]				
	000000					
0x274			ON[B,H,W]			
			000			
0x278			ON[B,H,W]			
			000			
0x27C			ON[B,H,W] 			
0x280			ON[B,H,W] 			
			ON[B,H,W]			
0x284			000			
			ON[B,H,W]			
0x288			000			
			ON[B,H,W]			
0x28C			00000			
		IRQ035M	ON[B,H,W]			
0x290			000000			
0.004		IRQ036MON[B,H,W]				
0x294	000					
0v209	IRQ037MON[B,H,W]					
0x298		000				
0x29C		IRQ038MON[B,H,W]				
0,250			000			
0x2A0		IRQ039M	ON[B,H,W]			
			00			
0x2A4		IRQ040MON[B,H,W]				
		00				
0x2A8		IRQ041MON[B,H,W]				
			00			
0x2AC			ON[B,H,W] 			
0x2B0		IRQ043MON[B,H,W]				
		00				
0x2B4	IRQ044MON[B,H,W] 00					
	 IRQ045MON[B,H,W]					
0x2B8	IRQU45MON[B,H,W]					
			ON[B,H,W]			
0x2BC			00			
			ON[B,H,W]			
0x2C0						
	00					





Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x2C4		IRQ048MON[B,H,W]					
	0						
0x2C8			ION[B,H,W]				
			00				
0x2CC			ION[B,H,W]				
			0				
0x2D0			ION[B,H,W]				
			0				
0x2D4			ION[B,H,W]				
			0				
0x2D8			ION[B,H,W] 0				
0x2DC			ION[B,H,W] 0				
0x2E0			ION[B,H,W] 0				
0x2E4		IRQ056MON[B,H,W] 0					
		*					
0x2E8		IRQ057MON[B,H,W] 0					
		IRQ058MON[B,H,W]					
0x2EC		0					
		IRQ059MON[B,H,W]					
0x2F0		00000					
0054		IRQ060M	ION[B,H,W]				
0x2F4			0				
0.250		IRQ061M	ION[B,H,W]				
0x2F8			00				
0x2FC		IRQ062M	ION[B,H,W]				
UAZI O			0				
0x300		IRQ063M	ION[B,H,W]				
			00				
0x304			ION[B,H,W]				
		0					
0x308		IRQ065MON[B,H,W]					
		00					
0x30C		IRQ066MON[B,H,W]					
			0				
0x310			ION[B,H,W]				
			·00				
0x314			ION[B,H,W] 0				
			U				



Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x318	IRQ069MON[B,H,W]						
0,010	00						
0x31C		IRQ070MON[B,H,W]					
0,010			0				
0x320		IRQ071M	ON[B,H,W]				
0.020			00				
0x324			ON[B,H,W]				
			0				
0x328			ON[B,H,W]				
			00				
0x32C			ON[B,H,W]				
			0				
0x330			ON[B,H,W]				
			00				
0x334			ON[B,H,W]				
0x338			ON[B,H,W]				
0x33C	IRQ078MON[B,H,W]						
0x340	IRQ079MON[B,H,W]						
			000000				
0x344		IRQ080MON[B,H,W]					
			0				
0x348			ON[B,H,W]				
0x34C			ON[B,H,W]				
			000				
0x350			ON[B,H,W] 0				
0x354			ON[B,H,W] 0				
			-				
0x358			ON[B,H,W] 0				
			ON[B,H,W]				
0x35C							
		0 IRQ087MON[B,H,W]					
0x360			ON[B,H,VV] 0				
			ON[B,H,W]				
0x364			он[в,п,vv] 0				
0x368			ON[B,H,W] 0				
	0						



Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
		IRQ090MON[B,H,W]					
0x36C		0					
		IRQ091MON[B,H,W]					
0x370		00					
		IRQ092M	ION[B,H,W]				
0x374			00000				
			ION[B,H,W]				
0x378			00000				
			ION[B,H,W]				
0x37C			00000				
			ION[B,H,W]				
0x380			00000				
0x384			ION[B,H,W] 0000000				
0x388			ION[B,H,W] 0000000				
0x38C		IRQ098MON[B,H,W]					
		0					
0x390		IRQ099MON[B,H,W]					
		0					
0x394		IRQ100MON[B,H,W]					
		0					
0x398		IRQ101MON[B,H,W]					
			000				
0x39C			ION[B,H,W]				
0.000			000				
0x3A0		IRQ103M	ION[B,H,W]				
0.0710			0				
0x3A4		IRQ104M	ION[B,H,W]				
UX3A4			000				
0.42 4.0		IRQ105M	ION[B,H,W]				
0x3A8			00				
0040		IRQ106M	ION[B,H,W]				
0x3AC			000				
		IRQ107M	ION[B,H,W]				
0x3B0			00				
		IRQ108M	ION[B,H,W]				
0x3B40							
			ION[B,H,W]				
0x3B8			·00				
			ION[B,H,W]				
0x3BC			00				



Base_Address	Register						
+ Address	+3 +2 +1 +0						
0x3C0		IRQ111MON[B,H,W]					
0.500							
0x3C4		IRQ112MON[B,H,W]					
0,001			00 00000000				
0x3C8		IRQ113M	ION[B,H,W]				
0.000			000000				
0x3CC		IRQ114M	ION[B,H,W]				
0,000			0000000				
0x3D0		IRQ115M	ION[B,H,W]				
			000				
0x3D4			ION[B,H,W]				
0x3D8			1ON[B,H,W]				
		000 IRQ118MON[B,H,W]					
0x3DC							
	00 IRQ119MON[B,H,W]						
0x3E0		0					
		IRQ120MON[B,H,W]					
0x3E4		0					
0.050		IRQ121M	ION[B,H,W]				
0x3E8			0				
0x3EC		IRQ122MON[B,H,W]					
UXSEC			0				
0x3F0		IRQ123M	ION[B,H,W]				
0,01 0			0				
0x3F4			ION[B,H,W]				
0,101 1		0					
0x3F8			ION[B,H,W]				
		00					
0x3FC			ION[B,H,W]				
			0				
0x400			ION[B,H,W]				
0.404 0.550	Т		00 				
0x404 – 0xFFC	-	-	=	=			



1.18 D/AC

12bit D/AC unit0 Base_Address : 0x4003_3000 12bit D/AC unit1 Base_Address : 0x4003_3008

Base_Address		Register			
+ Address	+3	+2	+1	+0	
0000				DACR[B,H,W]	
0x000	-	-	-	0000	
0004			DADI	R[H,W]	
0x004	-	-	XXXX X	XXXXXXX	
0x010 – 0xFFC	-	-	-	-	



1.19 HDMI-CEC

HDMI-CEC/Remote Control Receiver ch.0 Base_Address: 0x4003_4000 HDMI-CEC/Remote Control Receiver ch.1 Base_Address: 0x4003_4100

Base_Address		Register				
+ Address	+3	+2	+1	+0		
0x000				TXCTRL[B,H,W]		
00000	•	-	-	0000-0		
0x004				TXDATA[B,H,W]		
0,004	-	_		00000000		
0x008	_	_	_	TXSTS[B,H,W]		
0.000				000		
0x00C	-	_	-	SFREE[B,H,W]		
				0000		
0x010 - 0x03C	-	-	-	-		
0x040	-	_	RCCR[B,H,W]	RCST[B,H,W]		
			00000	00000000		
0x044	_	_	RCSHW[B,H,W]	RCDAHW[B,H,W]		
0,044			00000000	00000000		
0x048	_	_	RCDBHW[B,H,W]	_		
0.040			00000000			
0x04C	_	_	RCADR1[B,H,W]	RCADR2[B,H,W]		
0,040			00000	00000		
0x050	_	_	RCDTHH[B,H,W]	RCDTHL[B,H,W]		
0.000	-	_	00000000	00000000		
0x054			RCDTLH[B,H,W]	RCDTLL[B,H,W]		
0.0034	-	-	00000000	00000000		
0x058	_	_	RCCKI	D[B,H,W]		
0.000	-	-	00000	0000000		
0x05C	_	_	RCRC[B,H,W]	RCRHW[B,H,W]		
0.000	<u>-</u>	-	00	00000000		
0x060	_		RCLE[B,H,W]	_		
0,000	<u>-</u>	_	00000-00	-		
0x064	_	_	RCLELW[B,H,W]	RCLESW[B,H,W]		
03004	<u>-</u>		00000000	00000000		
0x068 - 0x0FC	-	-	-	-		



1.20 GPIO

1.20.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products

GPIO Base_Address: 0x4006_F000

Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x000		PFR0[B,H,W] 0000 0000 1111				
0x004		_	B,H,W]			
			0 0000 0000 0000			
0x008			B,H,W]			
			0 0000 0000 0000			
0x00C		•	B,H,W]			
			0 0000 0000 0000			
0x010			B,H,W]			
		000	0 0000 0000 0000			
0x014		•	B,H,W]			
		000	0 0000 0000 0000			
0x018		PFR6[B,H,W]			
		000	0 0000 0000 0000			
0x01C		PFR7[B,H,W]				
0.010		0000 0000 0000 0000				
0x020		PFR8[B,H,W]				
0,020		0000 0000 0000 0000				
0x024		PFR9[B,H,W]			
0,024		000	0 0000 0000 0000			
0x028	PFRA[B,H,W]					
0,020	0000 0000 0000 0000					
0x02C		PFRB[B,H,W]				
0x020		0000 0000 0000 0000				
0x030		PFRC[B,H,W]			
0x030		0000 0000 0000 0000				
0x034		PFRD[B,H,W]				
0x034	0000 0000 0000 0000					
0x038	PFRE[B,H,W]					
0,000		0000 0000 0000 0000				
0.000		PFRF[B,H,W]			
0x03C		000	0 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-		



Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x100		PCR0[B,H,W]					
0.2100		C	000 0000 0001 1111				
0x104		PCR	1[B,H,W]				
0,104		0	000 0000 0000 0000				
0x108		PCR	2[B,H,W]				
0.7100		0	000 0000 0000 0000				
0x10C		PCR	3[B,H,W]				
0.7100		0	000 0000 0000 0000				
0x110		PCR	4[B,H,W]				
0.7110		0	000 0000 0000 0000				
0x114		PCR	5[B,H,W]				
0.7114		0	000 0000 0000 0000				
0x118		PCR	6[B,H,W]				
0.110		0000 0000 0000 0000					
0x11C		PCR7[B,H,W]					
OXTIC		0000 0000 0000 0000					
0x120		-					
0x124		PCR	9[B,H,W]				
0.7124		0	000 0000 0000 0000				
0x128		PCR	A[B,H,W]				
0.7120		0	000 0000 0000 0000				
0x12C		PCR	B[B,H,W]				
0.1120		0	000 0000 0000 0000				
0x130		PCR	C[B,H,W]				
0.130		0	000 0000 0000 0000				
0x134		PCR	D[B,H,W]				
0.7134		0000 0000 0000 0000					
0x138		PCR	E[B,H,W]				
0.130		0000 0000 0000 0000					
0x13C		PCR	F[B,H,W]				
UXTOC		0	000 0000 0000 0000				
0x140 - 0x1FC	-	-	-	-			





Base_Address	Register					
+ Address	+3 +2 +1 +0					
0x200	DDR0[B,H,W]					
0x200		000	0000 0000 0000			
0x204		DDR1	[B,H,W]			
0.004		000	0000 0000 0000			
0x208		DDR2	[B,H,W]			
0,200		000	00 0000 0000 0000			
0x20C		DDR3	[B,H,W]			
0,200		000	00 0000 0000 0000			
0x210		DDR4	[B,H,W]			
0,210		000	00 0000 0000 0000			
0x214		DDR5	[B,H,W]			
0,214		000	00 0000 0000 0000			
0x218		DDR6	[B,H,W]			
0,210		000	00 0000 0000 0000			
0x21C		DDR7	[B,H,W]			
OXZIC	0000 0000 0000 0000					
0x220	DDR8[B,H,W]					
UNZZU		000	00 0000 0000 0000			
0x224		DDR9	[B,H,W]			
UNZZT		000	00 0000 0000 0000			
0x228		DDRA	[B,H,W]			
UNEEU		000	00 0000 0000 0000			
0x22C		DDRB	[B,H,W]			
UNE CO		0000 0000 0000 0000				
0x230		DDRC	[B,H,W]			
0,200		0000 0000 0000 0000				
0x234	DDRD[B,H,W]					
07.20 1	0000 0000 0000 0000					
0x238	DDRE[B,H,W]					
UNEGO		000	00 0000 0000 0000			
0x23C		DDRF	[B,H,W]			
0A200		000	00 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-		



Base_Address	Register					
+ Address	+3 +2 +1 +0					
0200	PDIR0[B,H,W]					
0x300		00	000 0000 0000 0000			
0×204		PDIR	1[B,H,W]			
0x304		00	000 0000 0000 0000			
0x308		PDIR	2[B,H,W]			
0x306		00	000 0000 0000 0000			
0×20€		PDIR	3[B,H,W]			
0x30C		00	000 0000 0000 0000			
0v210		PDIR	4[B,H,W]			
0x310		00	000 0000 0000 0000			
0v214		PDIR	5[B,H,W]			
0x314		00	000 0000 0000 0000			
0v240		PDIR	6[B,H,W]			
0x318		00	000 0000 0000 0000			
0x31C	PDIR7[B,H,W]					
0X31C	0000 0000 0000 0000					
0x320	PDIR8[B,H,W]					
0.320		00	000 0000 0000 0000			
0x324		PDIR	9[B,H,W]			
0X324		00	000 0000 0000 0000			
0x328		PDIRA	A[B,H,W]			
0.020		00	000 0000 0000 0000			
0x32C		PDIRI	3[B,H,W]			
0,020		00	000 0000 0000 0000			
0x330		PDIRO	C[B,H,W]			
0,000		00	000 0000 0000 0000			
0x334	PDIRD[B,H,W]					
0,004	0000 0000 0000 0000					
0x338	PDIRE[B,H,W]					
0.000	0000 0000 0000 0000					
0x33C		PDIRI	F[B,H,W]			
0.000		00	000 0000 0000			
0x340 - 0x3FC	-	-	-	-		





Address	Base_Address	Register					
0x404	+ Address	+3	+2	+1	+0		
0x404	0x400		PDOR	[B,H,W]			
0x404 0x408 PDCR2[B,H,W] 0x410 0x410 0x411 0x414 PDCR3[B,H,W] 0x00 0000 0000 0000 0x414 PDCR5[B,H,W] 0x00 0000 0000 0000 0x418 PDCR5[B,H,W] 0x410 0x418 PDCR5[B,H,W] 0x410 0x418 PDCR5[B,H,W] 0x410 0x410 0x418 PDCR6[B,H,W] 0x410 0x418 PDCR6[B,H,W] 0x410 0x418 PDCR7[B,H,W] 0x410 0x410 0x420 PDCR7[B,H,W] 0x420 PDCR8[B,H,W] 0x420 PDCR8[B,H,W] 0x420 PDCR8[B,H,W] 0x420 0x424 PDCR8[B,H,W] 0x426 PDCR6[B,H,W] 0x427 0x428 PDCR6[B,H,W] 0x428 PDCR6[B,H,W] 0x428 PDCR6[B,H,W] 0x420 0x420 PDCR6[B,H,W] 0x420 0x430 PDCR6[B,H,W] 0x430 PDCR6[B,H,W] 0x430 PDCR6[B,H,W] 0x430 0x430 PDCR6[B,H,W] 0x500 0x440 - 0x4FC -			000	0 0000 0000 0000			
DX408	0x404						
0x408 0x40C PDOR3[B,H,W] 0x410 PDOR4[B,H,W] PDOR5[B,H,W] 0x414 PDOR5[B,H,W] 0x418 PDOR6[B,H,W] 0x418 PDOR7[B,H,W] 0x410 0x410 PDOR7[B,H,W] 0x410 0x410 PDOR7[B,H,W] 0x410 0x410 PDOR7[B,H,W] 0x410 0x410 PDOR7[B,H,W] 0x420 PDOR8[B,H,W] 0x420 PDOR8[B,H,W] 0x420 PDOR8[B,H,W] 0x424 PDOR8[B,H,W] 0x424 PDOR8[B,H,W] 0x428 PDOR8[B,H,W] 0x428 PDOR8[B,H,W] 0x420 0x428 PDOR8[B,H,W] 0x430 PDOR8[B,H,W] 0x504 PDOR8[B,H,W]							
DX40C	0x408						
0x410 0x4110 0x4110 0x414 PDORS[B,H,W] 0x414 PDORS[B,H,W] 0x418 PDORS[B,H,W] 0x418 PDORS[B,H,W] 0x410 0x410 0x418 PDORS[B,H,W] 0x410 0x410 0x4118 PDORS[B,H,W] 0x410 PDORS[B,H,W] 0x410 PDORS[B,H,W] 0x420 PDORS[B,H,W] 0x420 PDORS[B,H,W] 0x424 PDORS[B,H,W] 0x428 PDORS[B,H,W] 0x428 PDORS[B,H,W] 0x428 PDORS[B,H,W] 0x428 PDORS[B,H,W] 0x420 PDORS[B,H,W] 0x420 0x421 PDORS[B,H,W] 0x422 PDORS[B,H,W] 0x428 PDORS[B,H,W] 0x428 PDORS[B,H,W] 0x420 0x420 PDORS[B,H,W] 0x420 0x420 PDORS[B,H,W] 0x420 0x420 PDORS[B,H,W] 0x430 PDORS[B,H,W] 0x504 - 0x57C PSPSRB,H,W] 0x504 - 0x57C PSPSRB,H,W] 0x508							
Description	0x40C						
0x410 0x414 PDORS[B,H,W]							
December 2000 December 200	0x410						
0x414							
DX418	0x414						
0x418 ————————————————————————————————————							
0x420	0x418						
0x420 0x424 0x424	0::440		PDOR7	[B,H,W]			
0x424 0x424	0x41C		000	0000 0000 0000			
0x424 0x428 0x428 0x42C 0x430 0x434 0x438 0x440 - 0x4FC 0x500 0	0×420		PDOR	[B,H,W]			
0x424	0.420		000	0 0000 0000 0000			
0x428	0x424		PDORS	[B,H,W]			
0x428 0x42C PDORB[B,H,W] 0x430 PDORC[B,H,W] 0x434 PDORD[B,H,W] 0x438 PDORF[B,H,W] 0x43C PDORF[B,H,W] 0x440 - 0x4FC - - - - ADE[B,H,W] 0x500 ADE[B,H,W] 0x504 - 0x57C - - - SPSR[B,H,W]			000	0 0000 0000 0000			
0x42C PDORB[B,H,W] 0x430 PDORC[B,H,W] 0x434 PDORD[B,H,W] 0x434 PDORD[B,H,W] 0x438 PDORE[B,H,W] 0x43C PDORF[B,H,W] 0x43C PDORF[B,H,W] 0x440 - 0x4FC - - 0x500 1111 1111 1111 1111 1111 1111 1111 0x504 - 0x57C - - 0x580 SPSR[B,H,W]	0x428						
0x42C							
PDORC[B,H,W]	0x42C						
0x430 0x434 PDORD[B,H,W]							
PDORD[B,H,W]	0x430						
0x434 0x438							
0x438 PDORE[B,H,W] 0x43C PDORF[B,H,W] 0x440 - 0x4FC - - - 0x500 1111 1111 1111 1111 1111 1111 1111 11	0x434						
0x438 0000 0000 0000 0000 0x43C PDORF[B,H,W] 0x440 - 0x4FC - - - 0x500 ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 - - 0x504 - 0x57C - - - 0x580 SPSR[B,H,W]							
0x440 - 0x4FC	0x438						
0x440 - 0x4FC							
0x500 ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 11	0x43C						
0x500	0x440 - 0x4FC						
0x504 - 0x57C SPSR[B,H,W]	0.500	ADE[B,H,W]					
0x580 SPSR[B,H,W]00 01	0,300	1111 1111 1111 1111 1111 1111					
0x58000 01	0x504 - 0x57C						
	0x580						
	0x584 - 0x5FC	-		I	-		



Base_Address	Register					
+ Address	+3	+3 +2 +1 +0				
0,4600	EPFR00[B,H,W]					
0x600	001100- 000000					
0x604		EPFR0	1[B,H,W]			
0,004		0000 0000 0000 0000	00 0000 0000 0000			
0x608		EPFR0	2[B,H,W]			
0,000		0000 0000 0000 0000	00 0000 0000 0000			
0x60C		EPFR0	3[B,H,W]			
0.000		0000 0000 0000 0000	00 0000 0000 0000			
0x610			4[B,H,W]			
			00 0000 -000 00			
0x614			5[B,H,W]			
			00 000000 00			
0x618			6[B,H,W]			
			0000 0000 0000 0000			
0x61C			7[B,H,W]			
			0 0000 0000 0000 8[B,H,W]			
0x620			o[b,n,vv]) 0000 0000 0000 0000			
			9[B,H,W]			
0x624			9[0,11,77]			
			0[B,H,W]			
0x628			0000 0000 0000 0000			
			1[B,H,W]			
0x62C			0000 0000 0000 0000			
		EPFR1:	2[B,H,W]			
0x630			00 000000 00			
0004		EPFR1:	3[B,H,W]			
0x634		00 000000 00	00 000000 00			
0x638		EPFR1	4[B,H,W]			
0.036		00 0000 0000 00)00 0000			
0x63C		EPFR1	5[B,H,W]			
0,000		0000 0000 0000 0000	0000 0000 0000 0000			
0x640		EPFR1	6[B,H,W]			
0X0 10	00 0000 0000 0000 0000 0000 0000					
0x644	EPFR17[B,H,W]					
	0000 0000 0000 0000 0000					
0x648	EPFR18[B,H,W]					
	00 0000 0000 0000 0000 0000					
0x64C	EPFR19[B,H,W]					
EPFR20[B,H,W]						
0x650		0 0000 <u>0</u> 000 0	0000 0000 0000 0000			
0x654 - 0x6FC	-	-	-	-		





Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x700		PZR0	[B,H,W]			
0.7700		000	00 0000 0000 0000			
0x704			[B,H,W]			
<i>5</i> 6 .			00 0000 0000 0000			
0x708			[B,H,W]			
			00 0000 0000 0000			
0x70C			[B,H,W]			
			00 0000 0000 0000			
0x710			[B,H,W]			
			00 0000 0000 0000			
0x714			[B,H,W] 00 0000 0000 0000			
			[B,H,W]			
0x718			00 0000 0000 0000			
			[B,H,W]			
0x71C			00 0000 0000 0000			
		PZR8	[B,H,W]			
0x720			00 0000 0000 0000			
0704		PZR9	[B,H,W]			
0x724		000	0000 0000 0000			
0x728		PZRA	[B,H,W]			
0.77.20		000	0000 0000 0000			
0x72C		PZRB	[B,H,W]			
0.720		000	00 0000 0000 0000			
0x730			[B,H,W]			
			00 0000 0000 0000			
0x734	PZRD[B,H,W]					
			00 0000 0000 0000			
0x738	PZRE[B,H,W]					
	0000 0000 0000 0000 P7REIR H WI					
0x73C	PZRF[B,H,W] 0000 0000 0000					
0x740 - 0xEFC			-	_		
0xF00 - 0xF04	_	*				
0xF08 – 0xFDC	-					
0xFE0		*				
0xFE4 - 0xFFC	-	-	-	-		



1.20.2 TYPE3-M4 Product

GPIO Base_Address : 0x4006_F000

Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0,4000		PFR0[B,H,W]					
0x000		000	00 0000 0001 1111				
0v004		PFR1[B,H,W]				
0x004		000	0000 0000 0000				
0x008		PFR2[B,H,W]				
0x006		000	00 0000 0000 0000				
0x00C		PFR3[B,H,W]				
UXUUC		000	0000 0000 0000				
0v010		PFR4[B,H,W]				
0x010		000	0000 0000 0000				
0::044		PFR5[B,H,W]				
0x014		000	00 0000 0000 0000				
0::040		PFR6[B,H,W]				
0x018		000	0000 0000 0000				
0::040		PFR7[B,H,W]					
0x01C		0000 0000 0000 0000					
0000		PFR8[B,H,W]					
0x020		000	0000 0000 0000				
0::004		PFR9[B,H,W]				
0x024		000	0000 0000 0000				
0000		PFRA[B,H,W]					
0x028		0000 0000 0000 0000					
0000		PFRB[B,H,W]				
0x02C		0000 0000 0000 0000					
0020		PFRC[B,H,W]				
0x030		0000 0000 0000 0000					
0::024		PFRD[B,H,W]					
0x034		0000 0000 0000 0000					
0,020		PFRE[B,H,W]					
0x038		0000 0000 0000 0000					
0.020		PFRF[B,H,W]				
0x03C		000	0000 0000 0000				
0x040 - 0x0FC	-	-	-	-			





Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x100		PCF	R0[B,H,W]				
0.00		(0000 0000 0001 1111				
0x104		PCF	R1[B,H,W]				
0.104		(0000 0000 0000 0000				
0x108		PCF	R2[B,H,W]				
5X155		(0000 0000 0000 0000				
0x10C			R3[B,H,W]				
SX.55		(0000 0000 0000 0000				
0x110			R4[B,H,W]				
		(0000 0000 0000 0000				
0x114			R5[B,H,W]				
-		(0000 0000 0000 0000				
0x118			R6[B,H,W]				
		0000 0000 0000 0000					
0x11C		PCR7[B,H,W]					
0.400		(0000 0000 0000 0000				
0x120		DO!	-				
0x124			R9[B,H,W]				
		0000 0000 0000 0000					
0x128			RA[B,H,W]				
		0000 0000 0000 0000					
0x12C		PCRB[B,H,W] 0000 0000 0000					
0x130		PCRC[B,H,W] 0000 0000 0000					
		PCRD[B,H,W]					
0x134		0000 0000 0000					
		PCRE[B,H,W]					
0x138		0000 0000 0000 0000					
		PCRF[B,H,W]					
0x13C			0000 0000 0000 0000				
0x140 - 0x1FC	-	-	-	-			



Base_Address	Register					
+ Address	+3 +2 +1 +0					
0x200	DDR0[B,H,W]					
0x200		000	0000 0000 0000			
0x204		DDR1	[B,H,W]			
0.204		000	0000 0000 0000			
0x208		DDR2	[B,H,W]			
0/200		000	00 0000 0000 0000			
0x20C		DDR3	[B,H,W]			
0,200		000	00 0000 0000 0000			
0x210		DDR4	[B,H,W]			
		000	00 0000 0000 0000			
0x214			[B,H,W]			
		000	00 0000 0000 0000			
0x218			[B,H,W]			
			00 0000 0000 0000			
0x21C	DDR7[B,H,W]					
	0000 0000 0000 0000					
0x220			[B,H,W]			
			00 0000 0000 0000			
0x224			[B,H,W] 00 0000 0000 0000			
0x228		DDRA[B,H,W]				
		0000 0000 0000 0000 DDRB[B,H,W]				
0x22C			00 0000 0000 0000			
0x230	DDRC[B,H,W]					
	DDRD[B,H,W]					
0x234	0000 0000 0000					
	DDRE[B,H,W]					
0x238	0000 0000 0000					
2 222		DDRF	[B,H,W]			
0x23C		000	00 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-		





Base_Address	Register					
+ Address	+3 +2 +1 +0					
0200	PDIR0[B,H,W]					
0x300		000	0000 0000 0000			
0×204		PDIR1	[B,H,W]			
0x304		000	0000 0000 0000			
0x308		PDIR2	[B,H,W]			
0x306		000	0000 0000 0000			
0×30C		PDIR3	[B,H,W]			
0x30C		000	0000 0000 0000			
0v210		PDIR4	[B,H,W]			
0x310		000	0000 0000 0000			
0::24.4		PDIR5	[B,H,W]			
0x314		000	0000 0000 0000			
0240		PDIR6	[B,H,W]			
0x318		000	0000 0000 0000			
0x31C	PDIR7[B,H,W]					
UXSTC	0000 0000 0000 0000					
0x320	PDIR8[B,H,W] 0000 0000 0000					
0x320						
0x324		PDIR9	[B,H,W]			
0x324		000	0000 0000 0000			
0x328		PDIRA	[B,H,W]			
0,320		0000 0000 0000 0000				
0x32C		PDIRE	8[B,H,W]			
0,520		0000 0000 0000 0000				
0x330		PDIRC	[B,H,W]			
0,000		0000 0000 0000 0000				
0x334	PDIRD[B,H,W]					
0,004	0000 0000 0000 0000					
0x338	PDIRE[B,H,W]					
0.000		0000 0000 0000 0000				
0x33C		PDIRF	[B,H,W]			
0.000		000	00 0000 0000 0000	,		
0x340 - 0x3FC	-	-	-	-		



Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x400		PDOR	[B,H,W]				
0,400		000	00 0000 0000 0000				
0x404			[B,H,W]				
		000	00 0000 0000 0000				
0x408			2[B,H,W]				
			00 0000 0000 0000				
0x40C			B[B,H,W]				
			00 0000 0000 0000				
0x410			I[B,H,W]				
			00 0000 0000 0000				
0x414			5[B,H,W]				
			00 0000 0000 0000				
0x418			S[B,H,W]				
			00 0000 0000 0000				
0x41C			7[B,H,W] 00 0000 0000 0000				
0x420			B[B,H,W] 00 0000 0000 0000				
			0[B,H,W]				
0x424			00 0000 0000 0000				
			N[B,H,W]				
0x428			00 0000 0000 0000				
			B[B,H,W]				
0x42C			00 0000 0000 0000				
		PDORC	[B,H,W]				
0x430			0000 0000 0000				
0::404		PDORD	D[B,H,W]				
0x434		000	0000 0000 0000				
0.420	PDORE[B,H,W]						
0x438	0000 0000 0000 0000						
0x43C	PDORF[B,H,W]						
0,430	0000 0000 0000 0000						
0x440 - 0x4FC							
0x500	ADE[B,H,W]						
	1111 1111 1111 1111 1111 1111						
0x504 - 0x57C	-						
0x580	SPSR[B,H,W]						
		1	00 01 I	T			
0x584 - 0x5FC	=	-	-	-			



Base_Address	Register						
+ Address	+3 +2 +1 +0						
0x600		EPFR00[B,H,W]					
	00001100- 000000						
0x604			1[B,H,W]				
			00 0000 0000 0000				
0x608			2[B,H,W] 00 0000 0000 0000				
0x60C			B[B,H,W] D0 0000 0000 0000				
0x610			4[B,H,W] 00 0000 -000 00				
0x614			5[B,H,W] 00 000000 00				
0x618			6[B,H,W] 0000 0000 0000 0000				
0x61C			7[B,H,W] 0 0000 0000 0000				
			B[B,H,W]				
0x620			• · · •				
	0000 0000 0000 0000 0000 0000 0000						
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000						
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000						
	EPFR11[B,H,W]						
0x62C			0000 0000 0000 0000				
			2[B,H,W]				
0x630			00 000000 00				
0x634	EPFR13[B,H,W] 00 000000 0000 000000 00						
		EPFR14	4[B,H,W]				
0x638			00 0000				
		EPFR1	5[B,H,W]				
0x63C			0000 0000 0000 0000				
		EPFR10	6[B,H,W]				
0x640		00 0000 0000 0000 0000 0000 0000					
	EPFR17[B,H,W]						
0x644	0000 0000 0000 0000 0000 0000						
0040		EPFR18[B,H,W]					
0x648	00 0000 0000 0000 0000 0000 0000						
0v640		EPFR19	9[B,H,W]				
0x64C							
Overo		EPFR20	D[B,H,W]				
0x650		0 0000 0000 0	000 0000 0000 0000				



Base_Address		Reç	jister				
+ Address	+3	+3 +2 +1 +0					
0.454		EPFR2	1[B,H,W]				
0x654							
0x658		EPFR2	2[B,H,W]				
0.000							
0x65C		EPFR2	3[B,H,W]				
OxooC		000	00 0000 0000 0000				
0x660		EPFR2	4[B,H,W]				
08000		0000 0000 0000					
0x664		EPFR2	5[B,H,W]				
0x004		0000					
0,4669		EPFR26[B,H,W]					
0x668		00 00	00 0000 0000 0000				
0x66C - 0x6FC	-	-	-	-			





Base_Address	Register						
+ Address	+3	+2 +1	+0				
0×700		PZR0[B,H,W]					
0x700	0000 0000 0000 0000						
0×704		PZR1[B,H,W]					
0x704	0000 0000 0000 0000						
0700		PZR2[B,H,W]					
0x708		0000 0000 0000 0000					
0.700		PZR3[B,H,W]					
0x70C		0000 0000 0000 0000					
. =		PZR4[B,H,W]					
0x710		0000 0000 0000 0000					
		PZR5[B,H,W]					
0x714		0000 0000 0000 0000					
		PZR6[B,H,W]					
0x718		0000 0000 0000 0000					
		PZR7[B,H,W]					
0x71C		0000 0000 0000 0000					
		PZR8[B,H,W]					
0x720		0000 0000 0000 0000					
0x724	PZR9[B,H,W] 0000 0000 0000						
0x728		PZRA[B,H,W]					
		0000 0000 0000 0000					
0x72C		PZRB[B,H,W]					
		0000 0000 0000 0000					
0x730		PZRC[B,H,W]					
		0000 0000 0000 0000					
0x734		PZRD[B,H,W]					
		0000 0000 0000 0000					
0x738		PZRE[B,H,W]					
		0000 0000 0000 0000					
0x73C		PZRF[B,H,W]					
om 00		0000 0000 0000 0000					
0x740		PDSR0[B,H,W]					
OXI 10		0000 0000 0000 0000					
0x744		PDSR1[B,H,W]					
OX7 44		0000 0000 0000 0000					
0x748		PDSR2[B,H,W]					
0.8746		0000 0000 0000 0000					
0v74C		PDSR3[B,H,W]					
0x74C		0000 0000 0000 0000					
0.750		PDSR4[B,H,W]					
0x750		0000 0000 0000 0000					
0.754		PDSR5[B,H,W]					
0x754		0000 0000 0000 0000					



Base_Address	Register					
+ Address	+3	+2	+1	+0		
0.750		PDSR6[B,H,W]				
0x758			0000 0000 0000 0000			
0x75C		PDS	SR7[B,H,W]			
0.730			0000 0000 0000 0000			
0x760			SR8[B,H,W]			
5.K. 55			0000 0000 0000 0000			
0x764			SR9[B,H,W]			
0.7.01			0000 0000 0000 0000			
0x768		PDS	SRA[B,H,W]			
0X1 00			0000 0000 0000 0000			
0x76C		PDSRB[B,H,W]				
OXI OC		0000 0000 0000 0000				
0x770		PDSRC[B,H,W]				
OXITO			0000 0000 0000 0000			
0x774		PDS	RD[B,H,W]			
OXI I			0000 0000 0000 0000			
0x778		PDS	RE[B,H,W]			
OXITO			0000 0000 0000 0000			
0x77C		PDS	RF[B,H,W]			
OXITO		0000 0000 0000 0000				
0x780 - 0xEFC	-	-	-	-		
0xF00 - 0xF04		*				
0xF08 - 0xFDC	-					
0xFE0			*			
0xFE4 - 0xFFC	=	=	-	=		



1.20.3 TYPE4-M4 Product

GPIO Base_Address: 0x4006_F000

Base_Address	Register							
+ Address	+3	+3 +2 +1 +0						
0,000	PFR0[B,H,W]							
0x000	0000 0000 0001 1111							
0x004		PFR	1[B,H,W]					
0x004		C	000 0000 0000 0000					
0x008		PFR	2[B,H,W]					
0.000		C	000 0000 0000 0000					
0x00C		PFR	3[B,H,W]					
UXUUC		C	000 0000 0000 0000					
0x010		PFR	4[B,H,W]					
0.010		C	000 0000 0000 0000					
0v04.4		PFR	85[B,H,W]					
0x014		C	000 0000 0000 0000					
0.049		PFR	86[B,H,W]					
0x018	0000 0000 0000 0000							
0x01C	PFR7[B,H,W]							
OXOTC	0000 0000 0000 0000							
0x020	PFR8[B,H,W]							
0x020		0000 0000 0000 0000						
0x024		PFR	89[B,H,W]					
0x024		C	000 0000 0000 0000					
0x028		PFR	A[B,H,W]					
0.028		C	000 0000 0000 0000					
0x02C		PFR	B[B,H,W]					
0x02C		C	000 0000 0000 0000					
0x030		PFR	C[B,H,W]					
0x030		C	000 0000 0000 0000					
0x034		PFR	D[B,H,W]					
0.0004		C	000 0000 0000 0000					
0x038		PFR	E[B,H,W]					
08030		C	000 0000 0000 0000					
0x03C		PFR	F[B,H,W]					
0,030		C	000 0000 0000 0000					
0x040 - 0x0FC	=	-	-	-				



Base_Address		Register					
+ Address	+3	+3 +2 +1 +0					
0×100		PCR0[B,H,W]					
0x100		00	000 0000 0001 1111				
0x104		PCR ²	[B,H,W]				
0.8104		00	00 0000 0000 0000				
0x108		PCR2	2[B,H,W]				
0.7100		00	00 0000 0000 0000				
0x10C		PCR	B[B,H,W]				
0.7100		00	00 0000 0000 0000				
0x110		PCR4	I[B,H,W]				
0.7110		00	00 0000 0000 0000				
0x114		PCR	5[B,H,W]				
5		00	00 0000 0000 0000				
0x118			6[B,H,W]				
		0000 0000 0000 0000					
0x11C		PCR7[B,H,W]					
		0000 0000 0000 0000					
0x120			-	_			
0x124			P[B,H,W]				
		0000 0000 0000 0000					
0x128			A[B,H,W]				
		0000 0000 0000 0000					
0x12C			B[B,H,W]				
		0000 0000 0000 0000					
0x130			C[B,H,W] 00 0000 0000 0000				
				_			
0x134			D[B,H,W] .00,0000,0000,0000				
		0000 0000 0000 0000 PCRE[B,H,W]					
0x138			00 0000 0000 0000				
			F[B,H,W]				
0x13C			00 0000 0000 0000				
0x140 - 0x1FC	-	-	-	_			





Base_Address	Register					
+ Address	+3 +2 +1 +0					
0,200	DDR0[B,H,W] 0000 0000 0000					
0x200						
0x204	DDR1[B,H,W]					
0x204			0000 0000 0000 0000			
0x208		DD	R2[B,H,W]			
0.208			0000 0000 0000 0000			
0x20C		DD	R3[B,H,W]			
0.200			0000 0000 0000 0000			
0x210		DD	R4[B,H,W]			
0.210			0000 0000 0000 0000			
0x214		DD	PR5[B,H,W]			
0.82.14			0000 0000 0000 0000			
0v219	DDR6[B,H,W] 0000 0000 0000 0000					
0x218						
0x21C	DDR7[B,H,W]					
0X21C			0000 0000 0000 0000			
0x220	DDR8[B,H,W] 0000 0000 0000					
0.220						
0x224		DD	R9[B,H,W]			
0.224			0000 0000 0000 0000			
0x228		DD	PRA[B,H,W]			
UNZZU			0000 0000 0000 0000			
0x22C		DD	RB[B,H,W]			
UAZZC			0000 0000 0000 0000			
0x230		DD	RC[B,H,W]			
0,230			0000 0000 0000 0000			
0x234		DD	RD[B,H,W]			
0,254			0000 0000 0000 0000			
0x238		DD	RE[B,H,W]			
0,200			0000 0000 0000 0000			
0x23C		DD	PRF[B,H,W]			
UXZSC			0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-		



Base_Address		Re	gister			
+ Address	+3 +2 +1 +0					
0200	PDIR0[B,H,W]					
0x300	0000 0000 0000 0000					
0x304		PDIR	1[B,H,W]			
0x304		00	000 0000 0000 0000			
0x308		PDIR	2[B,H,W]			
0x308		00	000 0000 0000 0000			
0x30C		PDIR	3[B,H,W]			
0.300		00	000 0000 0000 0000			
0x310		PDIR	4[B,H,W]			
0.510		00	000 0000 0000 0000			
0x314		PDIR	5[B,H,W]			
0.314		00	000 0000 0000 0000			
0x318		PDIR	6[B,H,W]			
0.316	0000 0000 0000 0000					
0x31C	PDIR7[B,H,W]					
0.310	0000 0000 0000 0000					
0x320	PDIR8[B,H,W]					
0.0020	0000 0000 0000 0000					
0x324		PDIR	9[B,H,W]			
0.024		00	000 0000 0000 0000			
0x328		PDIR	A[B,H,W]			
0,020		00	000 0000 0000 0000			
0x32C		PDIR	B[B,H,W]			
0,020		00	000 0000 0000 0000			
0x330		PDIR	C[B,H,W]			
0,000		00	000 0000 0000 0000			
0x334	PDIRD[B,H,W]					
0.004	0000 0000 0000 0000					
0x338		PDIR	E[B,H,W]			
0.000		00	000 0000 0000 0000			
0x33C		PDIR	F[B,H,W]			
0.000		00	000 0000 0000 0000	<u></u>		
0x340 - 0x3FC	-	-	-	-		





Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x400		PDOR0[B,H,W]					
0.400		0000 0000 0000 0000					
0x404		PDOR1[B,H,W]					
			00 0000 0000 0000				
0x408			2[B,H,W]				
			00 0000 0000 0000				
0x40C			B[B,H,W]				
			00 0000 0000 0000				
0x410			4[B,H,W]				
			00 0000 0000 0000				
0x414			5[B,H,W]				
			00 0000 0000 0000				
0x418			6[B,H,W] 00 0000 0000 0000				
0x41C			7[B,H,W] 00 0000 0000 0000				
0x420		PDOR8[B,H,W] 0000 0000 0000					
			9[B,H,W]				
0x424			00 0000 0000 0000				
		PDORA	λ[B,H,W]				
0x428			00 0000 0000 0000				
_		PDORE	B[B,H,W]				
0x42C		000	00 0000 0000 0000				
0420		PDORG	C[B,H,W]				
0x430		000	00 0000 0000 0000				
0x434		PDORE	D[B,H,W]				
0,454		000	0000 0000 0000				
0x438		PDORE	E[B,H,W]				
0.430		000	00 0000 0000 0000				
0x43C			F[B,H,W]				
	0000 0000 0000 0000						
0x440 - 0x4FC							
0x500	ADE[B,H,W]						
	1111 1111 1111 1111 1111 1111 1111						
0x504 - 0x57C	-	-	-	-			
0x580	SPSR[B,H,W]						
0.584 0.550			00 01 T				
0x584 - 0x5FC	-	-	-	-			



Base_Address	Register							
+ Address	+3	+3 +2 +1 +0						
0000		EPFR00[B,H,W]						
0x600	00001100- 000000							
0.004		EPFR01[B,H,W]						
0x604		0000 0000 0000 0000	0000 0000 0000					
0000		EPFR02	2[B,H,W]					
0x608		0000 0000 0000 0000	0000 0000 0000					
0x60C		EPFR03	3[B,H,W]					
0,000		0000 0000 0000 0000	00 0000 0000 0000					
0x610		EPFR04	4[B,H,W]					
		00 000000 00	00 0000 -000 00					
0x614			5[B,H,W]					
		00 000000 00	00 000000 00					
0x618			6[B,H,W]					
			0000 0000 0000 0000					
0x61C			7[B,H,W]					
			0 0000 0000 0000					
0x620	EPFR08[B,H,W]							
	0000 0000 0000 0000 0000 0000 0000							
0x624	EPFR09[B,H,W]							
	0000 0000 0000 0000 0000 0000 0000							
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000							
0x62C		EPFR11[B,H,W] 00 0000 0000 0000 0000 0000						
0x630	EPFR12[B,H,W] 00 000000 0000 000000 00							
		EPFR13[B,H,W]						
0x634	00 000000 0000 000000 00							
0000		EPFR14	4[B,H,W]					
0x638		00 0000 0000 00	00 0000					
0x63C		EPFR1	5[B,H,W]					
0x03C		0000 0000 0000 0000	0000 0000 0000 0000					
0x640			6[B,H,W]					
0,040		00 0000 0000 0000	0000 0000 0000 0000					
0x644			7[B,H,W]					
			0000 0000 0000					
0x648			B[B,H,W]					
			0 0000 0000 0000					
0x64C		EPFR19	9[B,H,W]					
0x650			D[B,H,W]					
	0000 0000 0000 0000 0000 0000							



Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x654	EPFR21[B,H,W]					
0x658			2[B,H,W]			
			ND 11147			
0x65C			B[B,H,W] 0 0000 0000 0000			
			4[B,H,W]			
0x660			0000 0000 0000			
0,4664		EPFR2	5[B,H,W]			
0x664			0000			
0x668		EPFR26	6[B,H,W]			
			00 0000 0000 0000			
0x66C			7[B,H,W]			
			0000 0000 0000 0000			
0x670			B[B,H,W]			
			0000 0000 0000 0000			
0x674			9[B,H,W]			
			0000 0000 0000 0000			
0x67C			D[B,H,W] 0000 0000 0000			
0x680 – 0x6FC	-	-	-	_		
0,000 0,010			<u>I</u> B,H,W]			
0x700			0 0000 0000 0000			
		PZR1[B,H,W]			
0x704			0 0000 0000 0000			
0700		PZR2[B,H,W]			
0x708		000	0000 0000 0000			
0x70C		PZR3[B,H,W]			
0.700	0000 0000 0000 0000					
0x710		PZR4[B,H,W]				
		000	0 0000 0000 0000			
0x714			B,H,W]			
			0 0000 0000 0000			
0x718			B,H,W]			
	0000 0000 0000 0000					
0x71C	PZR7[B,H,W]					
	0000 0000 0000 0000					
0x720			B,H,W]			
			0 0000 0000 0000			
0x724			B,H,W]			
			0 0000 0000 0000			
0x728			B,H,W] 0 0000 0000 0000			
		000	0000 0000 0000			



Base_Address		Register				
+ Address	+3	+1	+0			
0.720		PZRB[B,H,W]			
0x72C		000	0000 0000 0000			
0x730		PZRC[[B,H,W]			
0.27.50		000	0000 0000 0000			
0x734		PZRD[B,H,W]				
0x734		0000 0000 0000 0000				
0.720		PZRE[B,H,W]				
0x738		000	0000 0000 0000			
0x73C		PZRF[B,H,W]			
0.7.30		000	0000 0000 0000			
0x740 - 0xEFC	-	-	-	-		
0xF00 - 0xF04	*					
0xF08 - 0xFDC						
0xFE0	*					
0xFE4 - 0xFFC	-	-	-	-		



1.20.4 TYPE5-M4 Product

GPIO Base_Address: 0x4006_F000

Base_Address	Register							
+ Address	+3	+3 +2 +1 +0						
0x000		PFR0[B,H,W]						
0x000	0000 0000 0001 1111							
0x004		PF	R1[B,H,W]					
0,004			0000 0000 0000 0000					
0x008		PF	R2[B,H,W]					
0,000			0000 0000 0000 0000					
0x00C		PF	R3[B,H,W]					
0,000			0000 0000 0000 0000					
0x010		PF	R4[B,H,W]					
0.010			0000 0000 0000 0000					
0x014		PF	R5[B,H,W]					
0.014			0000 0000 0000 0000					
0x018	PFR6[B,H,W]							
0.010			0000 0000 0000 0000					
0x01C		PF	R7[B,H,W]					
		0000 0000 0000 0000						
0x020			R8[B,H,W]					
			0000 0000 0000 0000					
0x024			R9[B,H,W]					
			0000 0000 0000 0000					
0x028			RA[B,H,W]					
			0000 0000 0000 0000					
0x02C			RB[B,H,W]					
		0000 0000 0000 0000						
0x030			RC[B,H,W]					
			0000 0000 0000 0000					
0x034		PFRD[B,H,W]						
			0000 0000 0000 0000					
0x038		PFRE[B,H,W]						
			0000 0000 0000 0000					
0x03C			RF[B,H,W]					
0.040.0.050			0000 0000 0000 0000					
0x040 - 0x0FC								



Base_Address	Register					
+ Address	+3 +2 +1 +0					
0v400	PCR0[B,H,W]					
0x100	0000 0000 0001 1111					
0x104		PCR	1[B,H,W]			
0.104		0	000 0000 0000 0000			
0x108		PCR	2[B,H,W]			
0.7100		0	000 0000 0000 0000			
0x10C			3[B,H,W]			
SX.00		0	000 0000 0000 0000			
0x110			4[B,H,W]			
			000 0000 0000 0000			
0x114			5[B,H,W]			
			000 0000 0000 0000			
0x118			6[B,H,W]			
	0000 0000 0000 0000					
0x11C	PCR7[B,H,W]					
0.400	0000 0000 0000 0000					
0x120		DCD	OLD TTWA			
0x124			.9[B,H,W] 000 0000 0000 0000			
			A[B,H,W]			
0x128			000 0000 0000 0000			
			B[B,H,W]			
0x12C			000 0000 0000 0000			
			C[B,H,W]			
0x130			000 0000 0000 0000			
		PCR	D[B,H,W]			
0x134	0000 0000 0000 0000					
0.400	PCRE[B,H,W]					
0x138	0000 0000 0000 0000					
0.420		PCR	F[B,H,W]			
0x13C		0	000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-		





Base_Address	Register					
+ Address	+3 +2 +1 +0					
0,200	DDR0[B,H,W]					
0x200		00	00 0000 0000 0000			
0x204		DDR1	[B,H,W]			
0.004		00	00 0000 0000 0000			
0x208		DDR2	[B,H,W]			
0.200		00	00 0000 0000 0000			
0x20C		DDR3	[B,H,W]			
0x20C		00	00 0000 0000 0000			
0x210		DDR4	[B,H,W]			
0.210		00	00 0000 0000 0000			
0v214		DDR5	[B,H,W]			
0x214		00	00 0000 0000 0000			
0v240		DDR6	[B,H,W]			
0x218		00	00 0000 0000 0000			
0v24C	DDR7[B,H,W] 0000 0000 0000					
0x21C						
0x220	DDR8[B,H,W]					
0x220	0000 0000 0000 0000					
0x224		DDR9	[B,H,W]			
0.224		00	00 0000 0000 0000			
0x228		DDRA	[B,H,W]			
0,220		00	00 0000 0000 0000			
0x22C		DDRB	[B,H,W]			
UAZZO		00	00 0000 0000 0000			
0x230		DDRC	[B,H,W]			
0,200		00	00 0000 0000 0000			
0x234		DDRD	[B,H,W]			
0,204	0000 0000 0000 0000					
0x238		DDRE[B,H,W]				
0,200		00	00 0000 0000 0000			
0x23C		DDRF	[B,H,W]			
0,200		00	00 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-		



Base_Address	ess Register					
+ Address	+3 +2 +1 +0					
0200	PDIR0[B,H,W]					
0x300		00	00 0000 0000 0000			
0x304		PDIR ²	1[B,H,W]			
0x304		00	00 0000 0000 0000			
0x308		PDIR	2[B,H,W]			
0x308		00	00 0000 0000 0000			
0x30C		PDIR	B[B,H,W]			
0.300		00	00 0000 0000 0000			
0x310		PDIR	4[B,H,W]			
0.310		00	00 0000 0000 0000			
0x314		PDIR	5[B,H,W]			
0.314		00	00 0000 0000 0000			
0x318		PDIR	6[B,H,W]			
0.316	0000 0000 0000 0000					
0x31C	PDIR7[B,H,W] 0000 0000 0000 0000					
0.310						
0x320	PDIR8[B,H,W]					
0.0020		0000 0000 0000 0000				
0x324		PDIR	9[B,H,W]			
0.024		0000 0000 0000 0000				
0x328		PDIR/	A[B,H,W]			
0,020		00	00 0000 0000 0000			
0x32C		PDIRE	B[B,H,W]			
0,020		00	00 0000 0000 0000			
0x330		PDIRO	C[B,H,W]			
0,000		00	00 0000 0000 0000			
0x334		PDIRI	D[B,H,W]			
0,004		0000 0000 0000 0000				
0x338		PDIRE	E[B,H,W]			
0.000		00	00 0000 0000 0000			
0x33C		PDIRI	F[B,H,W]			
0.000		00	00 0000 0000 0000			
0x340 - 0x3FC	=	-	-	-		





Base_Address	Register						
+ Address	+3	+3 +2 +1 +0					
0x400		PDORG	D[B,H,W]				
	0000 0000 0000 0000						
0x404			I[B,H,W]				
			00 0000 0000 0000				
0x408			2[B,H,W]				
			00 0000 0000 0000				
0x40C			B[B,H,W] 00 0000 0000 0000				
0x410			4[B,H,W] 00 0000 0000 0000				
			5[B,H,W]				
0x414			00 0000 0000 0000				
			6[B,H,W]				
0x418			00 0000 0000 0000				
		PDOR7	7[B,H,W]				
0x41C			00 0000 0000 0000				
0::400		PDOR	B[B,H,W]				
0x420		000	0000 0000 0000				
0x424		PDORS	9[B,H,W]				
0.424		000	00 0000 0000 0000				
0x428		PDORA	A[B,H,W]				
OX 120		0000 0000 0000 0000					
0x42C			B[B,H,W]				
			00 0000 0000 0000				
0x430			C[B,H,W]				
			00 0000 0000 0000				
0x434			D[B,H,W]				
			00 0000 0000 0000				
0x438			E[B,H,W] 00 0000 0000 0000				
0x43C	PDORF[B,H,W] 0000 0000 0000						
0x440 - 0x4FC							
		ADE[B,H,W]					
0x500	1111 1111 1111 1111 1111 1111						
0x504 - 0x57C	-						
0.4500		SPSR	[B,H,W]				
0x580			00 01				
0x584 - 0x5FC	-	-	-	-			



Base_Address	Register						
+ Address	+3 +2 +1 +0						
0.000		EPFR00[B,H,W]					
0x600	l	000011	00- 000000				
0.004		EPFR0	1[B,H,W]				
0x604	l	0000 0000 0000 0000	00 0000 0000 0000				
0000		EPFR02	2[B,H,W]				
0x608	l	0000 0000 0000 0000	00 0000 0000 0000				
0x60C		EPFR0	3[B,H,W]				
0,000							
0x610	l	EPFR0-	4[B,H,W]				
		00 000000 00	00 0000 -000 00				
0x614	l		5[B,H,W]				
		00 000000 00	00 000000 00				
0x618	l		6[B,H,W]				
			0000 0000 0000 0000				
0x61C	l		7[B,H,W]				
			0 0000 0000 0000				
0x620	l		B[B,H,W]				
	0000 0000 0000 0000 0000 0000 0000						
0x624	EPFR09[B,H,W]						
	0000 0000 0000 0000 0000 0000 0000						
0x628	EPFR10[B,H,W]						
	0000 0000 0000 0000 0000 0000 0000						
0x62C	EPFR11[B,H,W] 00 0000 0000 0000 0000 0000						
0x630	l	EPFR12[B,H,W] 00 000000 0000 000000 00					
		EPFR13[B.H.W]					
0x634	l	00 000000 0000 000000 00					
		EPFR1	4[B,H,W]				
0x638	l	00 0000 0000 00					
0000		EPFR1	5[B,H,W]				
0x63C	l	0000 0000 0000 0000	0000 0000 0000 0000				
0x640		EPFR10	6[B,H,W]				
0x040	00 0000 0000 0000 0000 0000 0000						
0x644	EPFR17[B,H,W]						
0.044							
0x648	1		8[B,H,W]				
			0 0000 0000 0000				
0x64C	1	EPFR19	9[B,H,W]				
0x650	1		D[B,H,W]				
	0000 0000 0000 0000 0000 0000						





Base_Address		Register				
+ Address	+3	+2	+1	+0		
0x654		EPFR2 ⁻	[B,H,W]			
0x658		EPFR22	P[B,H,W]			
0x65C			B[B,H,W] 0 0000 0000 0000			
0x660		EPFR24[B,H,W] 0000 0000 0000				
0x664		EPFR25[B,H,W]				
0x668		EPFR26[B,H,W] 00 0000 0000 0000				
0x66C - 0x680	-	-	-	-		
0x684		EPFR33[B,H,W] 0000 0000 0000 0000 0000				
0x688	-	-	-	-		
0x68C		EPFR35[B,H,W] 0000 0000 0000				
0x690 - 0x6FC	-	-	-	-		



Base_Address		Reg	jister			
+ Address	+3 +2 +1					
0700		PZR0	[B,H,W]			
0x700	0000 0000 0000 0000					
0.704		PZR1	[B,H,W]			
0x704		000	0000 0000 0000			
0700		PZR2	[B,H,W]			
0x708		000	0000 0000 0000			
0700		PZR3	[B,H,W]			
0x70C		000	0000 0000 0000			
0740		PZR4	[B,H,W]			
0x710		000	0000 0000 0000			
0×714		PZR5	[B,H,W]			
0x714		000	0000 0000 0000			
0740		PZR6	[B,H,W]			
0x718		000	0000 0000 0000			
0.710		PZR7	[B,H,W]			
0x71C		000	0000 0000 0000			
0.720		PZR8	[B,H,W]			
0x720		000	0000 0000 0000			
0×704		PZR9	[B,H,W]			
0x724	0000 0000 0000 0000					
0x728	PZRA[B,H,W] 0000 0000 0000					
0.7720						
0x72C	PZRB[B,H,W]					
0X120		000	00 0000 0000 0000			
0x730		PZRC	[B,H,W]			
0X100		000	00 0000 0000 0000			
0x734		PZRD	[B,H,W]			
OX O T		000	00 0000 0000 0000			
0x738		PZRE	[B,H,W]			
5X1 00		000	00 0000 0000 0000			
0x73C			[B,H,W]			
OXI OC		000	00 0000 0000 0000			
0x740			D[B,H,W]			
			00 0000 0000 0000			
0x744			I[B,H,W]			
-			00 0000 0000 0000			
0x748	PDSR2[B,H,W]					
-			00 0000 0000 0000			
0x74C			B[B,H,W]			
			00 0000 0000 0000			
0x750			4[B,H,W]			
			00 0000 0000 0000			
0x754			5[B,H,W]			
		000	0000 0000 0000			





Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x758	PDSR6[B,H,W]					
0x756	0000 0000 0000 0000					
0x75C		PDSI	R7[B,H,W]			
0X/3C		0	000 0000 0000 0000			
0x760		PDSI	R8[B,H,W]			
02700		0	000 0000 0000 0000			
0x764		PDSI	R9[B,H,W]			
02704		0	000 0000 0000 0000			
0x768		PDSI	RA[B,H,W]			
02700		0	000 0000 0000 0000			
0x76C		PDSI	RB[B,H,W]			
02700		0000 0000 0000 0000				
0x770		PDSRC[B,H,W]				
OXITO		0000 0000 0000 0000				
0x774		PDSRD[B,H,W]				
5 /11 1		0	000 0000 0000 0000			
0x778			RE[B,H,W]			
		0	000 0000 0000 0000			
0x77C			RF[B,H,W]			
	0000 0000 0000 0000					
0x780 - 0xEFC						
0xF00 – 0xF04	*					
0xF08 - 0xFDC	-	-	-	-		
0xFE0		T	*			
0xFE4 - 0xFFC	=	-	-	=		



1.21 LVD

LVD Base_Address : 0x4003_5000

Base_Address	Register Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	LVD_CTL[B,H,W] 000111
0x004	-	-	-	LVD_STR[B,H,W] 0
0x008	-	-	-	LVD_CLR[B,H,W] 1
0x00C		LVD_RLR[W] 00000000 00000000 000000001		
0x010	-	-	-	LVD_STR2 [B,H,W] 0
0x014 - 0x0FC	-	-	-	-

1.22 DS_Mode

DS_Mode Base_Address: 0x4003_5100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	*
0x004	-	-	-	RCK_CTL[B,H,W] 01
0x008 - 0x6FC	=	-	-	=
0x700	-	-	-	PMD_CTL[B,H,W] 0
0x704	-	-	-	WRFSR[B,H,W] 00
0x708	-	-		[B,H,W] 0000000
0x70C	-	-		B,H,W] 00000-00
0x710	-	-	-	WILVR[B,H,W] 00000
0x714	-	-	-	DSRAMR[B,H,W] 00
0x718 - 0x7FC	-	-	-	-
0x800	BUR04[B,H,W] 00000000	BUR03[B,H,W] 00000000	BUR02[B,H,W] 00000000	BUR01[B,H,W] 00000000
0x804	BUR08[B,H,W] 00000000	BUR07[B,H,W] 00000000	BUR06[B,H,W] 0000000	BUR05[B,H,W] 0000000
0x808	BUR012[B,H,W] 00000000	BUR11[B,H,W] 00000000	BUR10[B,H,W] 00000000	BUR09[B,H,W] 00000000
0x80C	BUR16[B,H,W] 00000000	BUR15[B,H,W] 00000000	BUR14[B,H,W] 00000000	BUR13[B,H,W] 00000000
0x810 - 0xEFC	-	-	-	-



1.23 USB Clock

USB Clock Base_Address : 0x4003_6000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	UCCR[B,H,W] -0000000
0x004	-	-	-	UPCR1[B,H,W] 00
0x008	-	-	-	UPCR2[B,H,W] 000
0x00C	-	-	-	UPCR3[B,H,W] 00000
0x010	-	-	-	UPCR4[B,H,W] -0111011
0x014	-	-	-	UP_STR[B,H,W] 0
0x018	-	-	-	UPINT_ENR[B,H,W] 0
0x01C	-	-	-	UPINT_CLR[B,H,W] 0
0x020	-	-	-	UPINT_STR[B,H,W]
0x024	-	-	-	UPCR5[B,H,W] 0100
0x028	-	-	-	UPCR6[B,H,W] 0010
0x02C	-	-	-	UPCR7[B,H,W] 0
0x030	-	-	-	USBEN0[B,H,W] 0
0x034	-	-	-	USBEN1[B,H,W] 0
0x038 - 0x0FC	-	-	-	-



1.24 CAN Prescaler

CAN_Prescaler Base_Address: 0x4003_7000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	CANPRE[B,H,W] 1011
0x004 - 0xFFC	-	-	-	-

1.25 MFS

 $MFS~ch.0~Base_Address: 0x4003_8000$

MFS ch.1 Base_Address: 0x4003_8100

MFS ch.2 Base_Address: 0x4003_8200

MFS ch.3 Base_Address: 0x4003_8300

MFS ch.4 Base_Address: 0x4003_8400

MFS ch.5 Base_Address: 0x4003_8500

 $MFS~ch.6~Base_Address: 0x4003_8600$

 $MFS~ch.7~Base_Address: 0x4003_8700$

MFS ch.8 Base_Address: 0x4003_8800

MFS ch.9 Base_Address: 0x4003_8900

MFS ch.10Base_Address : 0x4003_8A00

MFS ch.11 Base_Address: 0x4003_8B00

MFS ch.12Base_Address: 0x4003_8C00

 $MFS\ ch.13Base_Address: 0x4003_8D00$

MFS ch.14Base_Address : 0x4003_8E00

MFS ch.15Base_Address : 0x4003_8F00

Base_Address		Register				
+ Address	+3	+2	+1	+0		
0x000	-	-	SCR / IBCR[B,H,W] 000000	SMR[B,H,W] 000-00-0		
0x004	-	-	SSR[B,H,W] 0-000011	ESCR / IBSR[B,H,W] 00000000		
0x008	-	-	RDR/TDR[H,W] 00000000 00000000			
00000		(*1) RDR/	TDR[H,W]			
		00000000 00000000	00000000 00000000			





Base_Address		Register				
+ Address	+3	+3	+3	+3		
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000		
0x010	-	-	ISMK[B,H,W]	ISBA[B,H,W]		
0x014	-	-	FCR1[B,H,W] 00100	FCR0[B,H,W] -0000000		
0x018	-	-	FBYTE2[B,H,W] 00000000	FBYTE1[B,H,W] 00000000		
0x01C	-	-	SCSTR1/ EIBCR[B,H,W] 00000000	SCSTR0/ NFCR[B,H,W] 00000000		
0x020	-	-	SCSTR3[B,H,W] 00000000	SCSTR2[B,H,W] 00000000		
0x024	-	-	SACSR1[B,H,W] 00000000	SACSR0[B,H,W] 00000000		
0x028	-	-	STMR1[B,H,W] 00000000	STMR0[B,H,W] 00000000		
0x02C	-	-	STMCR1[B,H,W] 00000000	STMCR0[B,H,W] 00000000		
0x030	-	-	SCSCR1[B,H,W] 00000000	SCSCR0[B,H,W] 00100000		
0x034	-	-	SCSFR1[B,H,W] 10000000	SCSFR0[B,H,W] 10000000		
0x038	-	-	-	SCSFR2[B,H,W] 10000000		
0x03C	-	-	TBYTE1[B,H,W] 00000000	TBYTE0[B,H,W] 00000000		
0x040	-	-	TBYTE3[B,H,W] 00000000	TBYTE2[B,H,W] 00000000		
0x0144 - 0x1FC	-	-	-	-		

Note:

- (*1): RDR/TDR register's higher 16 bits can be accessed by word operation in I2S mode.



1.26 CRC

CRC Base_Address: 0x4003_9000

Base_Address		Register					
+ Address	+3	+3 +2 +1 +0					
0x000	_	_	_	CRCCR[B,H,W]			
0,000				-0000000			
0x004		CRCINIT[B,H,W]					
0x004		11111111 11111111 111111111					
0x008		CRCIN[B,H,W]					
0x006		00000000 000000000 000000000 000000000					
0000	CRCR[B,H,W]						
0x00C		11111111 11111111	11111111 11111111				

1.27 Watch Counter

Watch Counter Base_Address : 0x4003_A000

Base_Address		Register			
+ Address	+3	+2	+1	+0	
0000		WCCR[B,H,W]	WCRL[B,H,W]	WCRD[B,H,W]	
0x000	-	00000	000000	000000	
0x004 - 0x00C	-	-	-	-	
0x010	-	-	CLK_SE 000		
0x014	-	-	-	CLK_EN[B,H,W] 00	
0x018 - 0xFFC	=	-	=	-	



1.28 RTC

1.28.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE6-M4 Products

RTC Base_Address: 0x4003_B000

Base_Address	Register				
+ Address	+3	+2	+1	+0	
0400				WTCR10[B,H,W]	
0x100	-	1	-	00000000	
0x104				WTCR11[B,H,W]	
0.8104	-	-	-	00000	
0x108	_	_	_	WTCR12[B,H,W]	
0.100			_	00000000	
0x10C	_	_	_	WTCR13[B,H,W]	
0,100				00000000	
0x110	-	<u>-</u>	_	WTCR20[B,H,W]	
				000000	
0x114	-	-	_	WTCR21[B,H,W]	
				000 *	
0x118	-	-	-		
0x11C	-	-	-	WTSR[B,H,W]	
				-0000000	
0x120	-	-	-	WTMIR[B,H,W]	
				-0000000	
0x124	-	-	-	WTHR[B,H,W]	
				000000	
0x128	-	-	-	WTDR[B,H,W] 000000	
				WTDW[B,H,W]	
0x12C	-	-	-	000	
				WTMOR[B,H,W]	
0x130	-	-	-	00000	
				WTYR[B,H,W]	
0x134	-	-	-	00000000	
				ALMIR[B,H,W]	
0x138	-	-	=	-0000000	
0.400				ALHR[B,H,W]	
0x13C	-	-	-	000000	
0v4.40	_		_	ALDR[B,H,W]	
0x140	<u>-</u>	<u>-</u>	=	000000	
0x144				ALMOR[B,H,W]	
UX 144	<u>-</u>	<u>-</u>	-	00000	
0x148	_	_	_	ALYR[B,H,W]	
0.140	-	-	_	00000000	
0x14C	-	<u>-</u>	_	WTTR0[B,H,W]	
0.7.70				00000000	
0x150	-	-	_	WTTR1[B,H,W]	
200				00000000	
0x154	-	-	_	WTTR2[B,H,W]	
-				00	



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x158	-	-	-	WTCAL0[B,H,W] 00000000	
0x15C	-	-	-	WTCAL1[B,H,W] 00	
0x160	-	-	-	WTCALEN[B,H,W]	
0x164	-	-	-	WTDIV[B,H,W] 0000	
0x168	-	-	-	WTDIVEN[B,H,W]	
0x16C	-	-	-	WTCALPRD[B,H,W] 010011	
0x170	-	-	-	WTCOSEL[B,H,W]	
0x174	-	-	-	VB_CLKDIV[B,H,W] 00000111	
0x178	-	-	-	WTOSCCNT[B,H,W]	
0x17C	-	-	-	CCS[B,H,W] 00001000	
0x180	-	-	-	CCB[B,H,W] 00010000	
0x184	-	-	-	*	
0x188	-	-	-	BOOST[B,H,W] 11	
0x18C	-	-	-	EWKUP[B,H,W] 0	
0x190	-	-	-	VDET[B,H,W] 00	
0x194	-	-	-	*	
0x198	-	-	-	HIBRST[B,H,W] 0	
0x19C	-	-	-	VBPFR[B,H,W] 011100	
0x1A0	-	-	-	VBPCR[B,H,W] 0000	
0x1A4	-	-	-	VBDDR[B,H,W]	
0x1A8	-	-	-	VBDIR[B,H,W] 0000	
0x1AC	-	-	-	VBDOR[B,H,W] 1111	
0x0B0	-	-	-	VBPZR[B,H,W] 11	
0x1B4-1FF	-	-	-	-	





Base_Address	Register				
+ Address	+3	+2	+1	+0	
	BREG03[B,H,W]	BREG02[B,H,W]	BREG01[B,H,W]	BREG00[B,H,W]	
0x200	00000000	00000000	00000000	0000000	
	BREG07[B,H,W]	BREG06[B,H,W]	BREG05[B,H,W]	BREG04[B,H,W]	
0x204	00000000	00000000	00000000	00000000	
	BREG0B[B,H,W]	BREG0A[B,H,W]	BREG09[B,H,W]	BREG08[B,H,W]	
0x208	00000000	00000000	00000000	00000000	
	BREG0F[B,H,W]	BREG0E[B,H,W]	BREG0D[B,H,W]	BREG0C[B,H,W]	
0x20C	00000000	00000000	00000000	00000000	
	BREG13[B,H,W]	BREG12[B,H,W]	BREG11[B,H,W]	BREG10[B,H,W]	
0x210	00000000	00000000	00000000	00000000	
	BREG17[B,H,W]	BREG16[B,H,W]	BREG15[B,H,W]	BREG14[B,H,W]	
0x214	00000000	00000000	00000000	00000000	
	BREG1B[B,H,W]	BREG1A[B,H,W]	BREG19[B,H,W]	BREG18[B,H,W]	
0x218	00000000	00000000	00000000	00000000	
	BREG1F[B,H,W]	BREG1E[B,H,W]	BREG1D[B,H,W]	BREG1C[B,H,W]	
0x21C	00000000	00000000	00000000	00000000	
	BREG23[B,H,W]	BREG22[B,H,W]	BREG21[B,H,W]	BREG20[B,H,W]	
0x220	00000000	00000000	00000000	00000000	
	BREG27[B,H,W]	BREG26[B,H,W]	BREG25[B,H,W]	BREG24[B,H,W]	
0x224	00000000	00000000	00000000	00000000	
	BREG2B[B,H,W]	BREG2A[B,H,W]	BREG29[B,H,W]	BREG28[B,H,W]	
0x228	00000000	00000000	00000000	00000000	
	BREG2F[B,H,W]	BREG2E[B,H,W]	BREG2D[B,H,W]	BREG2C[B,H,W]	
0x22C	00000000	00000000	00000000	00000000	
	BREG33[B,H,W]	BREG32[B,H,W]	BREG31[B,H,W]	BREG30[B,H,W]	
0x230	00000000	00000000	00000000	00000000	
	BREG37[B,H,W]	BREG36[B,H,W]	BREG35[B,H,W]	BREG34[B,H,W]	
0x234	00000000	00000000	00000000	00000000	
	BREG3B[B,H,W]	BREG3A[B,H,W]	BREG39[B,H,W]	BREG38[B,H,W]	
0x238	00000000	00000000	00000000	00000000	
	BREG3F[B,H,W]	1			
0x23C	00000000	BREG3E[B,H,W] 00000000	BREG3D[B,H,W] 00000000	BREG3C[B,H,W] 00000000	
0x240	BREG43[B,H,W]	BREG42[B,H,W]	BREG41[B,H,W]	BREG40[B,H,W]	
+	00000000	00000000	00000000	00000000	
0x244	BREG47[B,H,W]	BREG46[B,H,W]	BREG45[B,H,W]	BREG44[B,H,W] 00000000	
	00000000	00000000	00000000		
0x248	BREG4B[B,H,W]	BREG4A[B,H,W]	BREG49[B,H,W]	BREG48[B,H,W]	
	00000000	00000000	00000000	00000000	
0x24C	BREG4F[B,H,W]	BREG4E[B,H,W]	BREG4D[B,H,W]	BREG4C[B,H,W]	
	00000000	00000000	00000000	00000000	
0x250	BREG53[B,H,W]	BREG52[B,H,W]	BREG51[B,H,W]	BREG50[B,H,W]	
	00000000	00000000	00000000	00000000	
0x254	BREG57[B,H,W]	BREG56[B,H,W]	BREG55[B,H,W]	BREG54[B,H,W]	
	00000000	00000000	00000000	00000000	
0x258	BREG5B[B,H,W]	BREG5A[B,H,W]	BREG59[B,H,W]	BREG58[B,H,W]	
	00000000	00000000	00000000	00000000	



Base_Address		Reg	ister			
+ Address	+3	+2	+1	+0		
0.050	BREG5F[B,H,W]	BREG5E[B,H,W]	BREG5D[B,H,W]	BREG5C[B,H,W]		
0x25C	00000000	00000000	00000000	00000000		
0000	BREG63[B,H,W]	BREG62[B,H,W]	BREG61[B,H,W]	BREG60[B,H,W]		
0x260	00000000	00000000	00000000	00000000		
0004	BREG67[B,H,W]	BREG66[B,H,W]	BREG65[B,H,W]	BREG64[B,H,W]		
0x264	00000000	00000000	00000000	00000000		
0000	BREG6B[B,H,W]	BREG6A[B,H,W]	BREG69[B,H,W]	BREG68[B,H,W]		
0x268	00000000	00000000	00000000	00000000		
0.000	BREG6F[B,H,W]	BREG6E[B,H,W]	BREG6D[B,H,W]	BREG6C[B,H,W]		
0x26C	00000000	00000000	00000000	00000000		
0070	BREG73[B,H,W]	BREG72[B,H,W]	BREG71[B,H,W]	BREG70[B,H,W]		
0x270	00000000	00000000	00000000	00000000		
0074	BREG77[B,H,W]	BREG76[B,H,W]	BREG75[B,H,W]	BREG74[B,H,W]		
0x274	00000000	00000000	00000000	00000000		
0,4270	BREG7B[B,H,W]	BREG7A[B,H,W]	BREG79[B,H,W]	BREG78[B,H,W]		
0x278	00000000	00000000	00000000	00000000		
0,270	BREG7F[B,H,W]	BREG7E[B,H,W]	BREG7D[B,H,W]	BREG7C[B,H,W]		
0x27C	00000000	00000000	00000000	00000000		
0x280-0xFFC	-	-	-	-		

1.28.2 TYPE4-M4 Product

RTC Base_Address: 0x4003_B000

Base_Address		Reg	ister			
+ Address	+3	+2	+1	+0		
0x100	-	-	-	WTCR10[B,H,W] 00000000		
0x104	-	-	-	WTCR11[B,H,W] 00000		
0x108	-	-	-	WTCR12[B,H,W] 00000000		
0x10C	-	-	-	WTCR13[B,H,W] 00000000		
0x110	-	-	-	WTCR20[B,H,W] 000000		
0x114	-	-	-	WTCR21[B,H,W]		
0x118	-	-	-	*		
0x11C	-	-	-	WTSR[B,H,W] -0000000		
0x120	-	-	-	WTMIR[B,H,W] -0000000		
0x124	-	-	-	WTHR[B,H,W] 000000		

A. Register Map



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x128	-	-	-	WTDR[B,H,W] 000000	
0x12C	-	-	-	WTDW[B,H,W] 000	
0x130	-	-	-	WTMOR[B,H,W] 00000	
0x134	-	-	-	WTYR[B,H,W] 00000000	
0x138	-	-	-	ALMIR[B,H,W] -0000000	
0x13C	-	-	-	ALHR[B,H,W] 000000	
0x140	-	-	-	ALDR[B,H,W] 000000	
0x144	-	-	-	ALMOR[B,H,W] 00000	
0x148	-	-	-	ALYR[B,H,W] 00000000	
0x14C	-	-	-	WTTR0[B,H,W] 00000000	
0x150	-	-	-	WTTR1[B,H,W] 00000000	
0x154	-	-	-	WTTR2[B,H,W] 00	
0x158	-	-	-	WTCAL0[B,H,W] 00000000	
0x15C	-	-	-	WTCAL1[B,H,W] 00	
0x160	-	-	-	WTCALEN[B,H,W] 0	
0x164	-	-	-	WTDIV[B,H,W] 0000	
0x168	-	-	-	WTDIVEN[B,H,W] 00	
0x16C	-	-	-	WTCALPRD[B,H,W] 010011	
0x170	-	-	-	WTCOSEL[B,H,W]	
0x174	-	-	-	VB_DIVCLK[B,H,W] 00000111	
0x178	-	-	-	WTOSCCNT[B,H,W]	
0x17C	-	-	-	CCS[B,H,W] 11001110	
0x180	-	-	-	CCB[B,H,W] 11001110	



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x184	-	-	-	*	
				BOOST[B,H,W]	
0x188	-	-	-	11	
				EWKUP[B,H,W]	
0x18C	-	-	-	0	
0x190	-	-	-	VDET[B,H,W]	
0.404				*	
0x194	-	-	-		
0x198	-	-	-	HIBRST[B,H,W]	
				0	
0x19C	-	-	_	VBPFR[B,H,W]	
				011100	
0x1A0	_	<u>-</u>	_	VBPCR[B,H,W]	
0,7,10				0000	
0x1A4				VBDDR[B,H,W]	
UXTA4	-	-	-	0000	
				VBDIR[B,H,W]	
0x1A8	-	-	-	XXXX	
				VBDOR[B,H,W]	
0x1AC	-	-	-	1111	
				VBPZR[B,H,W]	
0x1B0	=	-	-	11	
0x1B4-1FF	_		_		
5X121111	BREG03[B,H,W]	BREG02[B,H,W]	BREG01[B,H,W]	BREG00[B,H,W]	
0x200	00000000	00000000	00000000	00000000	
	BREG07[B,H,W]	BREG06[B,H,W]	BREG05[B,H,W]	BREG04[B,H,W]	
0x204	00000000	00000000	00000000	00000000	
	BREG0B[B,H,W]	BREG0A[B,H,W]	BREG09[B,H,W]	BREG08[B,H,W]	
0x208	00000000	00000000	00000000	00000000	
	BREG0F[B,H,W]	BREG0E[B,H,W]	BREG0D[B,H,W]	BREG0C[B,H,W]	
0x20C	00000000	00000000	00000000	00000000	
	BREG13[B,H,W]	BREG12[B,H,W]	BREG11[B,H,W]	BREG10[B,H,W]	
0x210	00000000	00000000	00000000	0000000	
0.044	BREG17[B,H,W]	BREG16[B,H,W]	BREG15[B,H,W]	BREG14[B,H,W]	
0x214	00000000	00000000	00000000	0000000	
0040	BREG1B[B,H,W]	BREG1A[B,H,W]	BREG19[B,H,W]	BREG18[B,H,W]	
0x218	00000000	00000000	00000000	00000000	
0x21C	BREG1F[B,H,W]	BREG1E[B,H,W]	BREG1D[B,H,W]	BREG1C[B,H,W]	
UAZIO	00000000	00000000	00000000	00000000	
0x220	BREG23[B,H,W]	BREG22[B,H,W]	BREG21[B,H,W]	BREG20[B,H,W]	
0,220	00000000	00000000	00000000	00000000	
0x224	BREG27[B,H,W]	BREG26[B,H,W]	BREG25[B,H,W]	BREG24[B,H,W]	
0,224	00000000	00000000	00000000	0000000	
0x228	BREG2B[B,H,W]	BREG2A[B,H,W]	BREG29[B,H,W]	BREG28[B,H,W]	
0,220	00000000	00000000	00000000	00000000	
0x22C	BREG2F[B,H,W]	BREG2E[B,H,W]	BREG2D[B,H,W]	BREG2C[B,H,W]	





Base_Address	Register				
+ Address	+3	+2	+1	+0	
	00000000	00000000	00000000	00000000	
	BREG33[B,H,W]	BREG32[B,H,W]	BREG31[B,H,W]	BREG30[B,H,W]	
0x230	00000000	00000000	00000000	00000000	
	BREG37[B,H,W]	BREG36[B,H,W]	BREG35[B,H,W]	BREG34[B,H,W]	
0x234	00000000	00000000	00000000	00000000	
	BREG3B[B,H,W]	BREG3A[B,H,W]	BREG39[B,H,W]	BREG38[B,H,W]	
0x238	00000000	00000000	00000000	00000000	
	BREG3F[B,H,W]	BREG3E[B,H,W]	BREG3D[B,H,W]	BREG3C[B,H,W]	
0x23C	00000000	00000000	00000000	00000000	
	BREG43[B,H,W]	BREG42[B,H,W]	BREG41[B,H,W]	BREG40[B,H,W]	
0x240	00000000	00000000	00000000	00000000	
	BREG47[B,H,W]	BREG46[B,H,W]	BREG45[B,H,W]	BREG44[B,H,W]	
0x244	00000000	00000000	00000000	00000000	
	BREG4B[B,H,W]	BREG4A[B,H,W]	BREG49[B,H,W]	BREG48[B,H,W]	
0x248	00000000	00000000	00000000	00000000	
	BREG4F[B,H,W]	BREG4E[B,H,W]	BREG4D[B,H,W]	BREG4C[B,H,W]	
0x24C	00000000	00000000	00000000	00000000	
	BREG53[B,H,W]	BREG52[B,H,W]	BREG51[B,H,W]	BREG50[B,H,W]	
0x250	00000000	00000000	00000000	00000000	
	BREG57[B,H,W]	BREG56[B,H,W]	BREG55[B,H,W]	BREG54[B,H,W]	
0x254	0000000	00000000	00000000	00000000	
0.050	BREG5B[B,H,W]	BREG5A[B,H,W]	BREG59[B,H,W]	BREG58[B,H,W]	
0x258	00000000	00000000	00000000	00000000	
0.050	BREG5F[B,H,W]	BREG5E[B,H,W]	BREG5D[B,H,W]	BREG5C[B,H,W]	
0x25C	00000000	00000000	00000000	00000000	
0000	BREG63[B,H,W]	BREG62[B,H,W]	BREG61[B,H,W]	BREG60[B,H,W]	
0x260	00000000	00000000	00000000	00000000	
0004	BREG67[B,H,W]	BREG66[B,H,W]	BREG65[B,H,W]	BREG64[B,H,W]	
0x264	00000000	00000000	00000000	00000000	
0000	BREG6B[B,H,W]	BREG6A[B,H,W]	BREG69[B,H,W]	BREG68[B,H,W]	
0x268	00000000	00000000	00000000	00000000	
0,260	BREG6F[B,H,W]	BREG6E[B,H,W]	BREG6D[B,H,W]	BREG6C[B,H,W]	
0x26C	00000000	00000000	00000000	00000000	
0v270	BREG73[B,H,W]	BREG72[B,H,W]	BREG71[B,H,W]	BREG70[B,H,W]	
0x270	00000000	00000000	00000000	00000000	
0v274	BREG77[B,H,W]	BREG76[B,H,W]	BREG75[B,H,W]	BREG74[B,H,W]	
0x274	00000000	00000000	00000000	00000000	
0v270	BREG7B[B,H,W]	BREG7A[B,H,W]	BREG79[B,H,W]	BREG78[B,H,W]	
0x278	00000000	00000000	00000000	00000000	
0x270	BREG7F[B,H,W]	BREG7E[B,H,W]	BREG7D[B,H,W]	BREG7C[B,H,W]	
0x27C	00000000	00000000	00000000	00000000	
0x280-0xFFC	-	-	-	-	



1.28.3 TYPE5-M4 Product

RTC Base_Address : 0x4003_B000

Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x000	WTCR1 [B,H,W]				
0.000	00000000 0000000000000 -00000-0				
0x004			2[B,H,W]		
0,004			0000		
0x008			[B,H,W]		
0,000		00000000 0	0000000 00000000	1	
0x00C	WTDR[B,H,W]	WTHR[B,H,W]	WTMIR[B,H,W]	WTSR[B,H,W]	
0,000	000000	000000	-0000000	-0000000	
0x010		WTYR[B,H,W]	WTMOR[B,H,W]	WTDW[B,H,W]	
00010	-	00000000	00000	000	
0x014	ALDR[B,H,W]	ALHR[B,H,W]	ALMIR[B,H,W]		
0x014	000000	000000	-0000000	-	
0x018		ALYR[B,H,W]	ALMOR[B,H,W]		
0x016	-	00000000	00000	-	
0x01C	WTTR [B,H,W]				
0,010	00 00000000 00000000				
0x020		_	WTCLKM[B,H,W]	WTCLKS[B,H,W]	
0,020	-	-	00	0	
0x024	_	WTCALEN[B,H,W]	WTCAL	_[B,H,W]	
0x024	-	0	00 (0000000	
0x028			WTDIVEN[B,H,W]	WTDIV[B,H,W]	
0x026	-	-	00	0000	
0x02C				WTCALPRD[B,H,W],	
UXUZC	<u>-</u>	-	-	010011	
0x030	_	_	_	WTCOSEL[B,H,W],	
0.000	<u>-</u>			0	
0x034-0x0FF	=	-	-	-	



1.29 Low-speed CR Prescaler

Low-speed CR Prescaler Base_Address : 0x4003_C000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W], 000000
0x004 - 0x0FC	-	-	-	-



1.30 Peripheral Clock Gating 1.30.1 **TYPE1-M1, TYPE2-M4 Products**

	Peripheral Clock	Gating I	Base_Address : 0x4	003_C100		
Base_Address	Register					
+ Address	+3	+2	+1	+0		
0,000		CKEN0[B,H,W]				
0x000	1-1-11111 11111111 11111111					
0.004		MRST0[B,H,W]				
0x004		0-00000 00000000 00000000				
0x008 - 0x00F	-	=	-	-		
0.010		CKEN1[B,H,W]				
0x010		11111111				
0.014		MRST1[B,H,W]				
0x014	00000000					
0x018 – 0x01F	-	=	-	-		
	CKEN2[B,H,W]					
0,4030	0**-00					
0x020	Products with CAN : *="1"					
	Products without CAN: *="0"					
0x024	MRST2[B,H,W]					
		000				
0x028 - 0x67C	-	-	-	-		

1.30.2 **TYPE3-M4, TYPE4-M4 Products**

Peripheral Clock Gating

Base_Address	Register			
+ Address	+3	+2	+1	+0
	CKEN0[B,H,W]			
0x000	1-11111 1111111111			
0004		MRST0	[B,H,W]	
0x004	0-00000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0040	CKEN1[B,H,W]			
0x010	11111111			
0.044	MRST1[B,H,W]			
0x014	00000000			
0x018 – 0x01F	-	-	-	-
	CKEN2[B,H,W]			
0000	0111000 -***00			
0x020	Products with : *="1"			
	Products without CAN: *="0"			
0::004	MRST2[B,H,W]			
0x024	0000000 -00000			
0x028 - 0x67C	-	-	-	-

Base_Address: 0x4003_C100



1.30.3 TYPE5-M4, TYPE6-M4 Products

Peripheral Clock Gating Base_Address : 0x4003_C100

Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x000	CKEN0[B,H,W]					
	1-1-11111 111111111					
0,004	MRST0[B,H,W]					
0x004		0-00000 00000000 00000000				
0x008 – 0x00F	-					
0x010	CKEN1[B,H,W]					
00010	11111111					
0x014	MRST1[B,H,W]					
00014	00000000					
0x018 – 0x01F	-					
	CKEN2[B,H,W]					
0x020	011100 11110 -***00					
0x020	Products with: *="1"					
	Products without CAN : *="0"					
0,024	MRST2[B,H,W]					
0x024	0000-00 00000 -00000					
0x028 - 0x67C						



1.31 Smart Card Interface

Smart Card Interface ch.0 Base_Address : 0x4003_C900

Smart Card Interface ch.1 Base_Address : 0x4003_C980

Base_Address	Register				
+ Address	+3	+2	+1 +0		
000			GLOBALCONTROL1[H,W]		
0x00	-	-	-0001000 00000000		
004			STATUS[H,W]		
0x04	-	-	000000 00000001		
0.00	PORTCONT		TROL[H,W]		
0x08	-	-	000000 00-0-0		
0x0C			DATA	DATA[H,W]	
UXUC	-	-	0 00000000		
0x10			CARDCLOCK [H,W]		
0.10	-	-	00000000	00101000	
0x14			BAUDRATE[H,W]		
0.114	-	-	0000001	01110100	
0v19			GUARDTIMER[H,W]		
0.00	0x18		00	00000000	
0x1C			IDLETIMER[H,W]		
OXIC	-	-	00000000 00000000		
0x20	20		GLOBALCONTROL2[H,W]		
0x20	-	-	1-00		
0x24 -			DATA_FIFO[H,W]		
		-	0 00000000		
0x28			FIFO_LEVEL_READ[H,W]		
0.20	-	-	00000000 00000000		
0x2C			FIFO_LEVEL_WRITE[H,W]		
0.20	-	-	00000000 00000000		
0x30	_	_	FIFO_MC	DE[H,W]	
0.30	-	-	00000000	00000000000	
0x34		_	FIFO_CLEAR_M	SB_WRITE[H,W]	
0.0.04	<u>-</u>		0		
0x38			FIFO_CLEAR_MSB_ READ[H,W]		
0.00	<u>-</u>		0		
0x3C	-	-	-	-	
0x40	<u> </u>		IRQ_STA	TUS[H,W]	
	-	_	00000000		
0x44- 0x7C	-	-	-	-	



1.32 MFSI2S

MFSI2S ch.A Base_Address : 0x4003_CA00

Base_Address + Address		Register			
	+3	+2	+1	+0	
			CNTLREG[B, H,W] 0-0 -0000-01		
0x00	-	-			
0.04			I2SCLK[B, H,W]		
0x04	-	-	00 00000000		
0x08			I2SST[B,H,W]	I2SRST[B,H,W]	
UXU8	-	-	00	00000000	
0x0C- 0xFC	-	-	-	-	

Note:

- In TYPE5-M4 product, MFSI2S ch.A applies to MFS ch.1.



1.33 I2S Prescaler

1.33.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 Products

I2S_Prescaler Base_Address: 0x4003_D000

Base_Address		Register				
+ Address	+3	+2	+1	+0		
0000		ICO	CR[B,H,W]			
0x000			00			
0x004		IPC	R1[B,H,W]			
0x004			0			
0x008		IPC	R2[B,H,W]			
0x008			000			
0x00C		IPC	R3[B,H,W]			
0.000			00001			
0x010		IPC	R4[B,H,W]			
0.010						
0x014		IP_STR[B,H,W]				
0.014	0					
0x018		IPINT.	_ENR[B,H,W]			
0.010			0			
0x01C		IPINT	_CLR[B,H,W]			
0,010			0			
0x020		IPINT	_STR[B,H,W]			
0.020		0				
0x024		IPCR5[B,H,W]				
0.024			0011000			
0x028 – 0xFFC	<u>-</u>	_	_	_		



1.33.2 TYPE4-M4 Product

I2S_Prescaler Base_Address : 0x4003_D000

+ Address	Base_Address		Register						
0x000 IPCR1[B,H,W] 0x008 IPCR2[B,H,W] 0x00C IPCR3[B,H,W] 0x010 IPCR4[B,H,W] 0x014 IPSTR[B,H,W] 0x018 IPINT_ENR[B,H,W] 0x01C IPINT_CLR[B,H,W] 0x020 IPCR5[B,H,W] 0x024 IPCR5[B,H,W] 0x030 ICCR_1[B,H,W] 0x034 IPCR5_1[B,H,W]	+ Address	+3	+3 +2 +1 +0						
0x004	0x000		ICCR[B,H,W]						
0x004	0,000		00						
0x008	0x004								
0x00C 0x00C IPCR3[B,H,W]				0					
0x00C	0x008								
0x00C				000					
0x010 IPCR4[B,H,W]	0x00C								
0x010 0x014 IP_STR[B,H,W] 0x018 IPINT_ENR[B,H,W] 0x01C IPINT_CLR[B,H,W] 0x020 IPINT_STR[B,H,W] 0x024 IPCR5[B,H,W] 0x024 IPCR5[B,H,W] 0x026 IPCR5[B,H,W] 0x027 IPCR5[B,H,W] 1PCR5[B,H,W] 1PCR5[B,H,W] 1PCR5[B,H,W] 1PCR5[B,H,W]		_		00001					
0x014 IP_STR[B,H,W]	0x010								
0x014 0x018 IPINT_ENR[B,H,W] 0x01C IPINT_CLR[B,H,W] 0x020 IPINT_STR[B,H,W] 0x024 IPCR5[B,H,W] 0x028 - 0x02C - - 0x030 ICCR_1[B,H,W] 0x034 IPCR5_1[B,H,W]									
0x018 IPINT_ENR[B,H,W]	0x014		IP_STR[B,H,W]						
0x01C IPINT_CLR[B,H,W]			0						
0x01C	0x018								
0x01C0 0x0200 IPINT_STR[B,H,W]0 0x0240 IPCR5[B,H,W]0011000 0x028 - 0x02C									
0x020 IPINT_STR[B,H,W] 0 IPCR5[B,H,W] 0 0x024 IPCR5[B,H,W] 0 IPCR5[B,H,W] 0 IPCR5[B,H,W] 0 IPCR5[B,H,W] IPCR5[B,H,W] IPCR5[B,H,W] IPCR5[B,H,W] IPCR5[B,H,W]	0x01C								
0x024 IPCR5[B,H,W]									
0x024	0x020								
0x024									
0x028 - 0x02C	0x024								
0x030 ICCR_1[B,H,W]000 IPCR5_1[B,H,W]									
0x030000 0x034 IPCR5_1[B,H,W]	0x028 – 0x02C	-							
0x034 IPCR5_1[B,H,W]	0x030								
0x034									
	0x034								
0x038 – 0xFFC	0x038 – 0xFFC			-	-				



1.34 GDC_Prescaler

GDC_Prescaler Base_Address: 0x4003_D100

Base_Address	Register						
+ Address	+3 +2 +1 +1						
0x000			R[B,H,W] 0				
0x004			R1[B,H,W] 00				
0x008			R2[B,H,W] 000				
0x00C			R3 [B,H,W] 				
0x010			R4 [B,H,W]				
0x014		GP_STR[B,H,W] 0					
0x018		GPINT_ENR[B,H,W] 0					
0x01C		GPINT_CLR[B,H,W]					
0x020			STR[B,H,W] 0				
0x024	-	-	-	-			
0x028		GCSR[B,H,W] 00					
0x02C		GRCR[B,H,W] 0					
0x030			R[B,H,W] 0				
0x034- 0xFFC	-	-	-	-			

Note:

- For the register details of GDC, refer to the Chapter:GDC.



1.35 EXT-Bus I/F 1.35.1 TYPE1-M4 Product

EXT-Bus I/F Base_Address : 0x4003_F000

Base_Address	Register						
+ Address	+3 +2 +1 +0						
0x0000	MODE0[W]						
020000	000-00 00000000						
0x0004		MO	DE1[W]				
00004			-000-00 00000000				
0x0008		MO	DE2[W]				
SACCOC.			-000-00 00000000				
0x000C			DE3[W]				
			-000-00 00000000				
0x0010			DE4[W]				
			-000-00 00000001				
0x0014			DE5[W]				
			-000-00 00000000				
0x0018	MODE6[W]						
	00-00 00000000						
0x001C			DE7[W]				
	000-00 00000000						
0x0020	TIM0[W] 00000101 01011111 11110000 00001111						
			M1[W]				
0x0024							
		00000101 01011111 11110000 00001111 TIM2[W]					
0x0028	00000101 01011111 11110000 00001111						
		TII	M3[W]				
0x002C			11 11110000 00001111				
2 2222		TII	M4[W]				
0x0030	00000101 01011111 11110000 00001111						
0,0024	TIM5[W]						
0x0034	00000101 01011111 11110000 00001111						
0x0038		TII	M6[W]				
UXUUSO		00000101 0101111	11 11110000 00001111				
0x003C		TII	M7[W]				
0,0000		00000101 0101111	11 11110000 00001111				



Base_Address	ister					
+ Address	+3	+2	+1	+0		
0x0040		AREA				
0,00 10			00000000			
0x0044	AREA1[W]					
		0001111 00010000 AREA2[W]				
0x0048						
		AREA				
0x004C		0001111				
00050		AREA	\4[W]			
0x0050		0001111	01000000			
0x0054		AREA				
0,0001		0001111				
0x0058			A6[W]			
			01100000			
0x005C			47[W] 01110000			
		ATIM				
0x0060						
0.0004		ATIM				
0x0064			-0100 01011111			
0x0068		ATIM				
0,0000						
0x006C	ATIM3[W]					
		ATIN				
0x0070		ATIN				
		ATIM				
0x0074						
0.0070		ATIM				
0x0078			-0100 01011111			
0x007C		ATIM	17[W]			
			-0100 01011111	T		
0x0080 -	-	-	-	-		
0x00FC		SDMO	DE[W]			
0x0100			01001100-000			
0x0104	REFTIM[W] 0 00000000 00000000110011					
0v0109	PWRDWN[W]					
0x0108	00000000 00000000					
0x010C	SDTIM[W]					
		00 01000010 0				
0x0110			MD[W] 0000000 00000000			
0x0114 -		U00000 0C	000000 00000000			
0x01FC	-	-	-	-		





Base_Address	Register					
+ Address	+3	+ 2	+1	+ 0		
0x0200		MEMCERR[W]				
0x0204 – 0x02FC	-	-	-	-		
0x0300			.KR[W] 			
0x0304		EST 0				
0x0308		WEAD 00000000 00000000 00000000				
0x030C			CLR[W] 1			
0x0310			DDE[W] 1			
0x031C - 0x0EFC	-	-	-	-		
0x0F00 - 0x0F14	*	*	*	*		
0x0F18 – 0x0FFC	-	-	-	-		



1.35.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

EXT-Bus I/F Base_Address : 0x4003_F000

Base_Address	Register							
+ Address	+3	+3 +2 +1 +0						
0x0000		MODE0[W]						
000000		000-00 00000000						
0x0004		MODE1[W]						
0,0004		(000-00 00000000					
0x0008		MODE2[W]						
0,000			000-00 00000000					
0x000C			DE3[W]					
			000-00 00000000					
0x0010			DE4[W]					
			000-00 00000001					
0x0014			DE5[W]					
			000-00 00000000					
0x0018		MODE6[W]						
		000-00 00000000						
0x001C			DE7[W]					
	000-00 00000000							
0x0020		TIM0[W]						
		00000101 01011111 11110000 00001111 TIM1[W]						
0x0024			1 11110000 00001111					
			12[W]					
0x0028			12[VV] 1 11110000 00001111					
			13[W]					
0x002C			1 11110000 00001111					
		TIM	14[W]					
0x0030			1 11110000 00001111					
		TIM	15[W]					
0x0034		00000101 01011117	1 11110000 00001111					
00000		TIM	16[W]					
0x0038		00000101 0101111	1 11110000 00001111					
0,000		TIM	17[W]					
0x003C		00000101 01011111	1 11110000 00001111					



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x0040			40[W]		
0,0040			00000000		
0x0044			41[W]		
	0001111 00010000				
0x0048	AREA2[W] 0001111 00100000				
0x004C			43[W] 00110000		
			44[W]		
0x0050			01000000		
		AREA			
0x0054			01010000		
00050		AREA	46[W]		
0x0058		0001111	01100000		
0x005C			47[W]		
0.0000			01110000		
0x0060			10[W]		
0.0000			-0100 01011111		
0x0064			11[W]		
		ATIN			
0x0068			12[W]		
			-0100 01011111 13[W]		
0x006C			-0100 01011111		
			14[W]		
0x0070					
00074		ATIM	15[W]		
0x0074			-0100 01011111		
0x0078		ATIM	16[W]		
0,0076					
0x007C			17[W]		
			-0100 01011111	T	
0x0080 -	-	-	-	-	
0x00FC		CDMC	DERM!		
0x0100			DE[W] 01001100-000		
0x0104	REFTIM[W] 0 00000000 000000000110011				
0.0105			WN[W]		
0x0108	00000000 00000000				
0×010C	SDTIM[W]				
0x010C		000 01000010	00010001 010001		
0x0110		SDCM	MD[W]		
0.0110		000000 00	0000000 00000000	T	
0x0114 -	-	-	_	_	
0x01FC					



	Register				
+3	+ 2	+1	+ 0		
	MEMCERR[W]				
-	-	-	-		
	EST 0				
	WEAD 00000000 000000000 000000000				
-	-	-	-		
*	*	*	*		
-	-	-	-		
	-	+3 +2 MEN	+3 +2 +1 MEMCERR[W]		



1.36 USB

USB ch.0 Base_Address : 0x4004_0000 USB ch.1 Base_Address : 0x4005_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x2100		_	HCNT1[B,H,W]	HCNT0[B,H,W]
0X2100	-	-	001	00000000
0x2104	_	_	HERR[B,H,W]	HIRQ[B,H,W]
0/2 104	_	-	00000011	0-00000
0x2108	_	_	HFCOMP[B,H,W]	HSTATE[B,H,W]
0X2100			00000000	010010
0x210C	-	_	·	1/0)[B,H,W]
				0000000
0x2110	-	-	HADR[B,H,W]	HRTIMER(2)[B,H,W]
			-0000000	00
0x2114	-	-	·	0)[B,H,W]
				0000000
0x2118	-	-	· ·	1/0)[B,H,W]
			000 0	0000000
0x211C	<u>-</u>	-	_	HTOKEN[B,H,W]
				00000000
0x2120	_	_	UDCC[B,H,W]
0X2120			1	0100-00
0x2124	_	_		[H,W]
0X212-7			0	1000000
0x2128	_	_		[H,W]
0X2120			01100001	00000000
0x212C	-	_		:[H,W]
				-1000000
0x2130	-	_		:[H,W]
				-1000000
0x2134	-	_		:[H,W]
				-1000000
0x2138	-	=		:[H,W]
				-1000000
0x213C	-	-		P[H,W]
			000 00000000	
0x2140	-	-	UDCIE[B,H,W]	UDCS[B,H,W]
			000000	000000
0x2144	_	-	EP0IS[H,W]	
0,2111			101	
0x2148	_	-	EP0OS[H,W]	
5/L 140			10000	XXXXXXX
0x214C	_	_		[H,W]
UAZ 140			100-000X X	XXXXXXX



Base_Address	Register			
+ Address	+3	+2	+1	+0
0x2150			EP2S	[H,W]
UX2150	-	•	100-000	XXXXXX
0x2154			EP3S	[H,W]
0.72 1.34	<u>-</u>		100-000	XXXXXXX
0x2158	_	_	EP4S	[H,W]
0A2 130			100-000	XXXXXXX
0x215C	_	_	EP5S	[H,W]
0X213C			100-000	XXXXXXX
0x2160	-	-	EP0DTH[B,H,W]	EP0DTL[B,H,W]
0.00			XXXXXXXX	XXXXXXXX
0x2164 -		EP1DTH[B,H,W]	EP1DTL[B,H,W]	
0,2104	-		XXXXXXX	XXXXXXXX
0x2168	_	_	EP2DTH[B,H,W]	EP2DTL[B,H,W]
0,2100			XXXXXXXX	XXXXXXXX
0x216C	_	_	EP3DTH[B,H,W]	EP3DTL[B,H,W]
0,2100			XXXXXXXX	XXXXXXXX
0x2170	_	_	EP4DTH[B,H,W]	EP4DTL[B,H,W]
UNZ 11 U	_	_	XXXXXXXX	XXXXXXXX
0x2174	_	_	EP5DTH[B,H,W]	EP5DTL[B,H,W]
0,2174	-	_	XXXXXXXX	XXXXXXXX
0x2178 -	_	_	_	_
0x217C	-	_		



1.37 DMAC

DMAC Base_Address : 0x4006_0000

Base_Address	Register						
+ Address	+3	+2	+1	+0			
0x0000		DI	MACR[B,H,W]				
000000		00-00000)				
0x0010	DMACA0[B,H,W]						
00010		0000000 00	000000000000000000000000000000000000000				
0x0014		DM	IACB0[B,H,W]				
0,0014	000000 00000000 000000000						
0x0018	DMACSA0[B,H,W] 00000000 00000000 000000000						
0,0010							
0x001C		DM.	ACDA0[B,H,W]				
0,0010	00000000 00000000 00000000 00000000						
0x0020		DM	IACA1[B,H,W]				
0,0020		0000000 00	0000 00000000 00000000				
0x0024		DM	IACB1[B,H,W]				
0x0024		000000 000	00000 000000000				
0x0028		DM.	ACSA1[B,H,W]				
0x0026		00000000 0000	00000 00000000 00000000				
0x002C	DMACDA1[B,H,W]						
0,0020	00000000 00000000 00000000						
0x0030	DMACA2[B,H,W]						
0,0000	00000000 00000 00000000 00000000						
0x0034	DMACB2[B,H,W]						
0,000	000000 00000000 000000000						
0x0038		DM.	ACSA2[B,H,W]				
0.0000		00000000 0000	00000 00000000 00000000				
0x003C		DM	ACDA2[B,H,W]				
олосос		00000000 0000	00000 00000000 00000000				
0x0040		DM	IACA3[B,H,W]				
0,00010			0000 00000000 00000000				
0x0044			IACB3[B,H,W]				
			00000 000000000				
0x0048			ACSA3[B,H,W]				
			00000 00000000 00000000				
0x004C			ACDA3[B,H,W]				
			00000 00000000 00000000				
0x0050			IACA4[B,H,W]				
			0000 00000000 00000000				
0x0054			IACB4[B,H,W]				
			00000 000000000				
0x0058			ACSA4[B,H,W]				
			00000 00000000 00000000				
0x005C			ACDA4[B,H,W]				
			00000 000000000 000000000				
0x0060			IACA5[B,H,W]				
0,0000		0000000 00	0000 00000000 00000000				



Base_Address	Register						
+ Address	+3	+2	+1	+0			
0x0064	DMACB5[B,H,W]						
UXUU64		000000 000000	000 000000000				
0x0068		DMACS	SA5[B,H,W]				
0x0000		0000000 0000000	00 00000000 00000000				
0x006C		DMACI	DA5[B,H,W]				
0x006C		0000000 0000000	00 00000000 00000000				
0x0070		DMAC	A6[B,H,W]				
0x0070		00000000 0000	0 00000000 00000000				
0,0074	DMACB6[B,H,W]						
0x0074		000000 000000	000 000000000				
0x0078	DMACSA6[B,H,W]						
0X0078	00000000 00000000 00000000 00000000						
0x007C	DMACDA6[B,H,W]						
0x007C		0000000 0000000	00 00000000 00000000				
0x0080		DMAC	A7[B,H,W]				
0x0000		00000000 0000	0 00000000 00000000				
0x0084		DMAC	B7[B,H,W]				
0x0064		000000 000000	000 000000000				
0,000		DMACS	SA7[B,H,W]				
0x0088		0000000 0000000	00 00000000 00000000				
0,0000		DMACI	DA7[B,H,W]				
0x008C		00000000 00000000 00000000 00000000					
0x0090 -							
0x00FC	-	-	_	-			



1.38 DSTC

DSTC Base_Address : 0x4006_1000

Base_Address			Register			
+ Address	+3	+2	+1	+0		
0x0000		DE	STP[B,H,W]			
0x0000	00000000 00000000 00000000					
0x0004		HWD	DESP[B,H,W]			
00004		00XXXXXX XXXX	XX00 00000000 00000000			
0x0008	SW	/TR[H]	CFG[B]	CMD[B]		
020000	0000000	00000000	01000000	0000001		
0x000C		MON	IERS[B,H,W]			
			X00 XXXXXXXX XXX00000			
0x0010			NB[31:0] [B,H,W]			
			000 00000000 00000000			
0x0014			NB[63:32] [B,H,W]			
			000 00000000 00000000			
0x0018			IB[95:64] [B,H,W]			
			000 00000000 00000000			
0x001C			B[127:96] [B,H,W]			
			000 00000000 00000000			
0x0020	DREQENB[159:128] [B,H,W]					
	00000000 00000000 00000000					
0x0024	DREQENB[191:160] [B,H,W] 00000000 00000000 000000000					
0x0028	DREQENB[223:192] [B,H,W] 00000000 00000000 000000000					
0x002C	DREQENB[255:224] [B,H,W]					
	0000000 0000000 00000000 00000000					
0x0030	HWINT[31:0] [B,H,W] 00000000 00000000 000000000					
0x0034	HWINT[63:32] [B,H,W] 00000000 00000000 00000000					
	HWINT[95:64] [B,H,W]					
0x0038	00000000 00000000 000000000					
			127:96] [B,H,W]			
0x003C			000 00000000 00000000			
			159:128] [B,H,W]			
0x0040			000 00000000 00000000			
		HWINT[191:160] [B,H,W]			
0x0044			000 00000000 00000000			
00040		HWINT[2	223:192] [B,H,W]			
0x0048			000 00000000 00000000			
0×0040		HWINT[2	255:224] [B,H,W]			
0x004C		0000000 00000	000 00000000 00000000			
0x0050		HWINTC	LR[31:0] [B,H,W]			
UCUUXU		0000000 00000	000 00000000 00000000			
0x0054		HWINTCI	_R[63:32] [B,H,W]			
0.00004		00000000 00000	000 00000000 00000000			



Base_Address		R	Register		
+ Address	+3	+2	+1	+0	
		HWINTCL	R[95:64] [B,H,W]	l	
0x0058			000 00000000 00000000		
		HWINTCLF	R[127:96] [B,H,W]		
0x005C	00000000 00000000 00000000 00000000				
		HWINTCLR	[159:128] [B,H,W]		
0x060			000 00000000 00000000		
		HWINTCLR	![191:160] [B,H,W]		
0x064			000 00000000 00000000		
		HWINTCLR	[223:192] [B,H,W]		
0x068		000000 000000	000 00000000 00000000		
0.000		HWINTCLR	[255:224] [B,H,W]		
0x06C			000 00000000 00000000		
0.072		DQMSk	([31:0] [B,H,W]		
0x070			000 00000000 00000000		
0.074			[63:32] [B,H,W]		
0x074			000 00000000 00000000		
0070		DQMSK	[95:64] [B,H,W]		
0x078		0000000 000000	000 00000000 00000000		
0.070		DQMSK[127:96] [B,H,W]		
0x07C		0000000 000000	000 00000000 00000000		
0000	DQMSK[159:128] [B,H,W] 00000000 00000000 000000000				
0x080					
0004	DQMSK[191:160] [B,H,W]				
0x084	00000000 00000000 000000000				
0,4000		DQMSK[2	223:192] [B,H,W]		
0x088		0000000 000000	000 00000000 00000000		
0,000		DQMSK[2	255:224] [B,H,W]		
0x08C		0000000 0000000	000 00000000 00000000		
0x090		DQMSKC	LR[31:0] [B,H,W]		
0x090		000000 0000000	000 00000000 00000000		
0x004		DQMSKCL	_R[63:32] [B,H,W]		
0x094		0000000 0000000	000 00000000 00000000		
0x098		DQMSKCL	_R[95:64] [B,H,W]		
00030		0000000 000000	000 00000000 00000000		
0x09C		DQMSKCL	R[127:96] [B,H,W]		
0,000		0000000 000000	000 00000000 00000000		
0x0A0		DQMSKCLF	R[159:128] [B,H,W]		
UNUNU		0000000 000000	000 00000000 00000000		
0x0A4		DQMSKCLF	R[191:160] [B,H,W]		
0,0,14		0000000 000000	000 00000000 00000000		
0x0A8	DQMSKCLR[223:192] [B,H,W]				
5,0,10	00000000 00000000 00000000				
0x0AC		DQMSKCLF	R[255:224] [B,H,W]		
5,0,10		0000000 000000	000 00000000 00000000	1	
0x00B0 -	_	_	_	_	
0x0FFC				_	



1.39 CAN

CAN ch.0 Base_Address : 0x4006_2000
CAN ch.1 Base_Address : 0x4006_3000

se_Address	Register				
+ Address	+3	+2	+1	+0	
0x0000	STATR[I	B,H,W]	CTRLR[B	,H,W]	
0.0000	00	000000	000)-0001	
0x0004	BTR[B,H,W]		ERRCNT[B,H,W]		
00004	-0100011 00000001		00000000 00000000		
0x0008	TESTR[B,H,W]	INTR[B,	H,W]	
0x0000	X(00000	00000000	0000000	
0x000C			BRPER[E	s,H,W]	
0x0000	-	<u>-</u>		-0000	
0x0010	IF1CMSK	[[B,H,W]	IF1CREQ[B,H,W]	
000010	00	000000	0 000	000001	
0v0014	IF1MSK2	[B,H,W]	IF1MSK1[I	B,H,W]	
0x0014	11-11111 1	11111111	11111111 1	1111111	
0,0040	IF1ARB2	[B,H,W]	IF1ARB1[I	3,H,W]	
0x0018	00000000		00000000		
			IF1MCTR[B,H,W]		
0x001C			0000000 0000		
0::0020 IF1DTA2[B,H,W]		[B,H,W]	IF1DTA1[B,H,W]		
0x0020	0000000 0000000		0000000 0000000		
IF1DTB2[B,H,W]			IF1DTB1[I		
0x0024	00000000 00000000		00000000		
0x0028 -					
0x002F	=	-	=	-	
	IF1DTA1	[B,H,W]	IF1DTA2[B,H,W]		
0x0030	00000000		00000000 00000000		
	IF1DTB1	[B,H,W]	IF1DTB2[B,H,W]		
0x0034	00000000		00000000		
0x0038 -					
0x003C	-	-	-	-	
	IF2CMSK	(IB.H.WI	IF2CREQ[B.H.W1	
0x0040	00		0 00000001		
	IF2MSK2		IF2MSK1[B,H,W]		
0x0044	11-11111 ′		11111111 1		
	IF2ARB2	[B.H.W]	IF2ARB1[I	3.H.W1	
0x0048	00000000		00000000		
			IF2MCTR[
0x004C	-	-	00000000		
	IF2DTA2	[B.H.W]	IF2DTA1[8		
0x0050	00000000		00000000 00000000		
	IF2DTB2		IF2DTB1[I		
0x0054	00000000	- · · · -	00000000		
0x0058 -					
0x005C	-	-	-	=	



Base_Address		Reg	ister	
+ Address	+3	+2	+1	+0
00000	IF2DTA1[B,H,W]		IF2DTA2	[B,H,W]
0x0060	00000000	00000000	00000000	00000000
0.0004	IF2DTB1	[B,H,W]	IF2DTB2	[B,H,W]
0x0064	00000000	00000000	00000000	00000000
0x0068 -				
0x007C	-	-	-	-
0x0080	TREQR2[B,H,W]		TREQR1	[B,H,W]
0x0080	00000000 00000000		00000000 00000000	
0x0084 -				
0x008F	-	-	-	-
0.0000	NEWDT2[B,H,W]		NEWDT1	[B,H,W]
0x0090	00000000 00000000		00000000 00000000	
0x0094 -				
0x009F	-	-	-	-
00040	INTPND2	[B,H,W]	INTPND1[B,H,W]	
0x00A0	00000000	00000000	00000000 00000000	
0x00A4 -				
0x00AF	-	<u>-</u>	-	
0x00B0	MSGVAL2	2[B,H,W]	MSGVAL1[B,H,W]	
UXUUDU	00000000	00000000	00000000	00000000
0x00B4 -				
0x0FFC	-	-	-	-



1.40 Ethernet-MAC

Ethernet-MAC Base_Address : 0x4006_4000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000 – 0x1FFC	xxxxxxx	xxxxxxx	xxxxxxx	xxxxxxx

Note:

- For the register details of Ethernet-MAC block, refer to the "Ethernet part".

1.41 Ethernet-Control

Ethernet-Control Base_Address: 0x4006_6000

Base_Address	Register				
+ Address	+3 +2 +1 +0				
0x000 - 0xFFC	XXXXXXXX	XXXXXXXX	XXXXXXX	XXXXXXXX	

Note:

- For the register details of Ethernet-Control block, refer to the Ethernet part.



1.42 I2S

I2S ch.0 Base_Address : 0x4006_C000

I2S ch.1 Base_Address: 0x4006_C800

Base_Address	Register						
+ Address	+3	+2	+1	+0			
0000	RXFDAT[B,H,W]						
0x000		00000000 00000000 00000000					
0x004		TXF	DAT[B,H,W]				
0x004	00000000 00000000 00000000 00000000						
0x008		CNTF	REG[B,H,W]				
00000		0000000 0000000	000 00000000 00000000				
0x00C		MCR0	REG[B,H,W]				
UXUUC		-000000 000000	000 -0000000 00000000				
0x010	MCR1REG[B,H,W]						
0.010		00000000 00000000 00000000 00000000					
0x014		MCR2REG[B,H,W]					
0.014	00000000 00000000 00000000 00000000						
0x018	OPRREG[B,H,W]						
0.010		0	00				
0x01C		SR	ST[B,H,W]				
0,010		0					
0x020		INTO	NT[B,H,W]				
0.020		-11111111111	1110000000000				
0x024		STAT	TUS[B,H,W]				
0.024		00000000000	00 00000000 00000000				
0x028	DMAACT[B,H,W]						
0,020		0	00				
0x02C		TSTF	REG[B,H,W]				
0.020			0				
0x030 - 0xFFC	-	-	-	-			

1.43 SD-Card

SD-Card Base_Address: 0x4006_E000

Base_Address	Register			
+ Address	+3 +2 +1 +0			
0x000 – 0xFFC	XXXXXXXX	XXXXXXX	XXXXXXX	XXXXXXX

Note:

For the register details of SD-Card block, refer to the Chapter SD Card Interface.



1.44 CAN FD

CAN FD Base_Address: 0x4007_0000

Base_Address	Register						
+ Address	+3	+2	+1	+0			
0x000	CREL[B,H,W]						
0,000		00110000 00010011 00000101 0000110					
0x004		ENDN[B,H,W]				
0,001		10000111 01100101	01000011 00100001	T			
0x008	-	-	-	-			
0x00C			B,H,W]				
		00000 000000					
0x010		TEST[
			000000 X000				
0x014		RWD[I					
			000000 00000000				
0x018			[B,H,W]				
0x01C		BTP[E	· · · · · -				
		00 00000000 -	001010 00110011				
0x020		_	B,H,W]				
		000000					
0x024 TSCV[B,H,W]							
		00000000 00000000					
0x028		TOCC[
			11000				
0x02C		_	B,H,W]				
		11 ⁻	T	T			
0x030 - 0x03C	-	-	-	-			
0x040			3,H,W]				
			0000000 00000000				
0x044		PSR[E					
		0 I	00111 00000111	<u> </u>			
0x048 - 0x04C	-	-	-	-			
0x050			H,W]				
	00000000 00000000 00000000						
0x054			H,W]				
		00000000 00000000 000000000					
0x058	ILS[B,H,W]						
		00000000 00000000 00000000					
0x05C			,H,W]				
0.000 0.070			00 I				
0x060 - 0x07C	=	-	-	-			



Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x080		GF	C[B,H,W]			
0,000						
0x084		SIDF	C[B,H,W]			
0,004	00000000 00000000 000000					
0x088	XIDFC[B,H,W]					
0,000		0000000	00000000 000000			
0x08C	=	-	-	=		
0x090			M[B,H,W]			
			1 11111111 11111111			
0x094			S[B,H,W]			
			0000000 00000000			
0x098			Γ1[B,H,W]			
			00 00000000 00000000			
0x09C			Г2[B,H,W]			
			00 00000000 00000000			
0x0A0			OC[B,H,W]			
	00000000 -0000000 0000000 000000					
0x0A4			OS[B,H,W]			
	000000000000000					
0x0A8	RXF0A[B,H,W] 000000					
0x0AC	RXBC[B,H,W]					
		00000000 000000				
0x0B0	RXF1C[B,H,W]					
			00 00000000 000000			
0x0B4			S[B,H,W]			
			0000000 -0000000			
0x0B8			A[B,H,W] 			
			6C[B,H,W]			
0x0BC			000 -000-000			
			C[B,H,W]			
0x0C0			00 00000000 000000			
			QS[B,H,W]			
0x0C4)00000 <u>-</u> 000000			
			6C[B,H,W]			
0x0C8			·000			
			RP[B,H,W]			
0x0CC			00 00000000 00000000			
			AR[B,H,W]			
0x0D0	00000000 00000000 000000000					
0x0D4			CR[B,H,W] 00 00000000 00000000			
			O[B,H,W]			
0x0D8			00 00000000 00000000			
			CF[B,H,W]			
0x0DC			00 00000000 00000000			



Base_Address	Register					
+ Address	+3	+2	+1	+0		
0x0E0	TXBTIE[B,H,W]					
UXUEU		00000000 000000000 00000000 00000000				
0x0E4	TXBCIE[B,H,W]					
UXUE4		00000000 00000000	00000000 00000000			
0x0E8 - 0x0EC	-	-	-	-		
0x0F0		TXEFC	[B,H,W]			
UXUFU		000000000000	0000000 000000			
0x0F4	TXEFS[B,H,W]					
UXUF4		0000000 -	00000000000			
0x0F8	TXEFA[B,H,W]					
UXUFO	00000					
0x0FC - 0x1FC	-	-	-	-		
0x200	FDSEAR[B,H,W]		FDESR[B,H,W]	FDECR[B,H,W]		
0,200	00000000	00000000	00	0000		
0x204	FDDEAR[B,H,W]		FDESCR[B,H,W]			
0,204	00000000	0000000	00	-		
0x208		FDFEC	R[B,H,W]			
0,200	0					
0x20C	-	-	-	-		
0x210	TSMDR	R[B,H,W]	TSCNTR[B,H,W]			
0,210		0		0		
0x214	TSDIVR[B,H,W]					
0,214	00000000 00000000					
0x218	TSCPCL	R[B,H,W]	TSCDTR[B,H,W]			
0,210	00000000	00000000	00000000	00000000		
0x21C - 0xFFC	-	-	-	-		

CAN FD Message RAM

Base_Address		Message RAM				
+ Address	+3	+2	+1	+0		
		Rx Buffer and FIFO Element [W]				
		Tx Buffer Element [W]				
0x8000 -		Tx Event FIFO Element [W]				
0xBFFC	Filter Element [W]					
		Extended Message ID Filter Element [W]				

Note:

- For the register details of CAN FD Message RAM block, refer to the Chapter CAN FD Controller.



1.45 Programmable-CRC

Programmable-CRC Base_Address: 0x4008_0000

Base_Address		Register				
+ Address	+3	+2	+1	+0		
0000		CRCn_PC	DRY[B,H,W]			
0x000		00000100 1100000	1 00011101 10110111			
0x004		CRCn_SE	ED[B,H,W]			
0x004		11111111 11111111 111111111				
0x008		CRCn_FXOR[B,H,W]				
0x008	11111111 11111111 111111111					
0x00C		CRCn_CFG[B,H,W]				
0x00C		00000000 11100000 00000000 00000000				
0x010		CRCn_W	/R[B,H,W]			
0.010		00000000 00000000 00000000 00000000				
0x014		CRCn_RD[B,H,W]				
0.014		00000000 00000000 00000000 00000000				
0x018 - 0xFFC	-	-	-	-		

1.46 WorkFlash_IF

WorkFlash_IF Base_Address: 0x200E_0000

Base_Address		Register				
+ Address	+3	+3 +2 +1 +0				
0x000		WFASZR[B,H,W]				
0x004		WFRWTR[B,H,W]				
0x008		WFSTR[B,H,W]				
0x00C - 0xFFF	-	-	-	-		

Note:

 For the register details of Workflash IF block, refer to the Flash Programming Manual of the product used.



1.47 High-Speed Quad SPI Controller 1.47.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 Products

High-Speed Quad SPI Controller Base_Address : 0xD000_0000

Base_Address		Reg	ister		
+ Address	+3	+2	+1	+0	
0x000		HSSPIn_MC	CTRL[B,H,W]		
0,000			000-00		
0x004		HSSPIn_PCC0[B,H,W]			
			0000000 00000000		
0x008			CC1[B,H,W]		
			0000000 00000000		
0x00C			CC2[B,H,W] 0000000 00000000		
			CC3[B,H,W]		
0x010		_	000000 00000000		
			TXF[B,H,W]		
0x014			0000000		
0040		HSSPIn_T	XE[B,H,W]		
0x018			0000000		
0x01C		HSSPIn_T	XC[B,H,W]		
0X01C			0000000		
0x020		_	RXF[B,H,W]		
			0000000		
0x024		HSSPIn_RXE[B,H,W]			
			0000000		
0x028			RXC[B,H,W] 000000		
			ULTF[B,H,W]		
0x02C		_	00000		
			ULTC[B,H,W]		
0x030			00000		
			HSSPIn_DMDMAEN	HSSPIn_DMCFG	
0x034	-	-	[B,H,W]	[B,H,W]	
			00	001	
	HSSPIn_DMTRP	HSSPIn_DMPSEL	HSSPIn_DMSTOP	HSSPIn_DMSTART	
0x038	[B,H,W]	[B,H,W]	[B,H,W]	[B,H,W]	
	0000	00	0	0	
0,4030	HSSPIn_DM	1BCS[B,H,W]	HSSPIn_DM	BCC[B,H,W]	
0x03C	00000000 00000000 00000000 00000000			00000000	
0.040	HSSPIn_DMSTATUS[B,H,W]				
0x040	0000000000				
0x044	-	-	-	-	
	-	-	-	-	
		HQQDIn EIE	OCEGIR H WI	l	
0x04C					
0x044 0x048	-	- - HSSPIn_FIF6			



Base_Address		Reg	ister			
+ Address	+3	+2	+1	+0		
0,050		HSSPIn_TXF	FIFO0[B,H,W]			
0x050		00000000 00000000	00000000 00000000			
0054		HSSPIn_TXF	FIFO1[B,H,W]			
0x054		00000000 00000000	00000000 00000000			
0050		HSSPIn_TXF	FIFO2[B,H,W]			
0x058	00000000 00000000 00000000					
	HSSPIn_TXFIFO3[B,H,W]					
0x05C		0000000 00000000	00000000 00000000			
		HSSPIn_TXF	FIFO4[B,H,W]			
0x060		0000000 00000000	0000000 00000000			
		HSSPIn_TXF	FIFO5[B,H,W]			
0x064		0000000 0000000	00000000 00000000			
		HSSPIn TXI	FIFO6[B,H,W]			
0x068		_	00000000 00000000			
			FIFO7[B,H,W]			
0x06C		_	00000000 00000000			
			FIFO8[B,H,W]			
0x070		_	00000000 00000000			
			FIFO9[B,H,W]			
0x074		-	00000000 00000000			
			TFO10[B,H,W]			
0x078		_	00000000 00000000			
0x07C	HSSPIn_TXFIFO11[B,H,W] 00000000 00000000 00000000 00000000					
0x080	HSSPIn_TXFIFO12[B,H,W]					
			00000000 00000000			
0x084		_	TFO13[B,H,W]			
			00000000 00000000			
0x088		-	TFO14[B,H,W]			
			00000000 00000000			
0x08C		_	TFO15[B,H,W]			
			00000000 00000000			
0x090		_	FIFO0[B,H,W]			
			00000000 00000000			
0x094		_	FIFO1[B,H,W]			
			00000000 00000000			
0x098		_	FIFO2[B,H,W]			
			00000000 00000000			
0x09C		_	FIFO3[B,H,W]			
-			00000000 00000000			
0x0A0		_	FIFO4[B,H,W]			
			00000000 00000000			
0x0A4		_	FIFO5[B,H,W]			
O/O/ LT		00000000 00000000	00000000 00000000			
0x0A8		HSSPIn_RXI	FIFO6[B,H,W]			
0,000		00000000 00000000	00000000 00000000			
0x0AC		HSSPIn_RXI	FIFO7[B,H,W]			
UXUAC		0000000 00000000	00000000 00000000			



Base_Address		Reg	jister		
+ Address	+3	+2	+1	+0	
0x0B0		HSSPIn_RXI	FIFO8[B,H,W]		
ОХОВО	00000000 00000000 00000000				
0x0B4		HSSPIn_RXI	FIFO9[B,H,W]		
0X0D4		00000000 00000000	00000000 00000000		
0x0B8		HSSPIn_RXF	FIFO10[B,H,W]		
OXOBO		00000000 00000000	00000000 00000000		
0x0BC		HSSPIn_RXF	FIFO11[B,H,W]		
CAODO		00000000 00000000	00000000 00000000		
0x0C0		HSSPIn_RXF	FIFO12[B,H,W]		
one or		00000000 00000000	00000000 00000000		
0x0C4		HSSPIn_RXF	FIFO13[B,H,W]		
0,004		00000000 00000000	00000000 00000000		
0x0C8		HSSPIn_RXF	FIFO14[B,H,W]		
0,000		00000000 00000000	00000000 00000000		
0x0CC			FIFO15[B,H,W]		
			00000000 00000000		
0x0D0		HSSPIn_CS	SCFG[B,H,W]		
0.020	000000000				
0x0D4	HSSPIn_CSITIME[B,H,W]				
	11111111 11111111				
0x0D8	HSSPIn_CSAEXT[B,H,W]				
	00000000 00000000 000				
0x0DC	HSSPIn_RD0	CSDC1[B,H,W]	HSSPIn_RDC	SDC0[B,H,W]	
		00000	00000000		
0x0E0	-	CSDC3[B,H,W]	HSSPIn_RDC		
		00000	00000000		
0x0E4	HSSPIn_RDCSDC5[B,H,W]		HSSPIn_RDCSDC4[B,H,W] 000000000000		
		00000			
0x0E8	-	CSDC7[B,H,W]	HSSPIn_RDCSDC6[B,H,W]		
		00000	000000000000		
0x0EC	_	CSDC1[B,H,W]	HSSPIn_WRCSDC0[B,H,W]		
		00000	00000000		
0x0F0	_	CSDC3[B,H,W]	HSSPIn_WRCSDC2[B,H,W]		
		00000	000000000000		
0x0F4		CSDC5[B,H,W] 00000	HSSPIn_WRCSDC4[B,H,W] 000000000000		
		OSDC7[B,H,W]	HSSPIn_WRC		
0x0F8		00000	00000000		
	000000		MID[B,H,W]	0000	
0x0FC			00000110 00110000		
0x100 - 0x3FC	-	-	-	_	
0.7100 - 0.01 0	-	<u>-</u>	_	QDCLKR[B,H,W]	
0x400	-	-	-	1111	
				DBCNT[B,H,W]	
0x404	-	-	-	00	
0x408 - 0xFFC	-	-	-	00	



1.47.2 TYPE4-M4 Product

High-Speed Quad SPI Controller Base_Address : 0xD0A0_4000

Base_Address		Reg	ister	
+ Address	+3	+2	+1	+0
0x000		HSSPIn_M(CTRL[B,H,W]	
0,000				
0x004		HSSPIn_P	CC0[B,H,W]	
0,0004		1111111 00	0000000 00000000	
0x008		HSSPIn_P	CC1[B,H,W]	
0,000		1111111 00	0000000 00000000	
0x00C		HSSPIn_P	CC2[B,H,W]	
oxooc .		1111111 00	0000000 00000000	
0x010		HSSPIn_P	CC3[B,H,W]	
0.0.0		1111111 00	0000000 00000000	
0x014		HSSPIn_1	TXF[B,H,W]	
0.011			0000000	
0x018		HSSPIn_1	TXE[B,H,W]	
0.0.0			0000000	
0x01C		-	TXC[B,H,W]	
0,0.0			0000000	
0x020		HSSPIn_F	RXF[B,H,W]	
0,1020			0000000	
0x024			RXE[B,H,W]	
			0000000	
0x028		_	RXC[B,H,W]	
			0000000	
0x02C		_	ULTF[B,H,W]	
0x030			ULTC[B,H,W]	
		 I	00000	1
			HSSPIn_DMDMAEN	HSSPIn_DMCFG
0x034	-	-	[B,H,W]	[B,H,W]
	LICCOL DATED	LICODIA DIADOCI	00	001
0x038	HSSPIn_DMTRP [B,H,W]	HSSPIn_DMPSEL [B,H,W]	HSSPIn_DMSTOP [B,H,W]	HSSPIn_DMSTART [B,H,W]
0x036	го,п,vvj 0000	00	[D, \pi, \vv] 0	0
		MBCS[B,H,W]	HSSPIn_DM	
0x03C		00000000	00000000	
0x040	HSSPIn_DMSTATUS[B,H,W]			
0x044				
0x048	<u>-</u>	-	_	_
		HSSPIn FIF	I OCFG[B,H,W]	l
0x04C			-00000_01110111	



Base_Address		Re	egister				
+ Address	+3	+2	+1	+0			
0.050		HSSPIn_T	XFIFO0[B,H,W]				
0x050	00000000 00000000 00000000 00000000						
0.054		HSSPIn_T	XFIFO1[B,H,W]				
0x054	00000000 00000000 00000000 00000000						
0050		HSSPIn_T	XFIFO2[B,H,W]				
0x058		0000000 0000000	00 0000000 00000000				
0050		HSSPIn_T	XFIFO3[B,H,W]				
0x05C		0000000 0000000	00 0000000 00000000				
0000		HSSPIn_T	XFIFO4[B,H,W]				
0x060		0000000 0000000	00 00000000 00000000				
0004		HSSPIn_T	XFIFO5[B,H,W]				
0x064		0000000 0000000	00 00000000 00000000				
0000		HSSPIn_T	XFIFO6[B,H,W]				
0x068		0000000 0000000	00 0000000 00000000				
0x06C		HSSPIn_T	XFIFO7[B,H,W]				
UXU6C		0000000 0000000	00 0000000 00000000				
0x070		HSSPIn_T	XFIFO8[B,H,W]				
0x070		0000000 0000000	00 00000000 000000000				
0074		HSSPIn_T	XFIFO9[B,H,W]				
0x074		0000000 0000000	00 0000000 00000000				
0070		HSSPIn_TX	(FIFO10[B,H,W]				
0x078	00000000 00000000 000000000						
0,070		HSSPIn_TX	(FIFO11[B,H,W]				
0x07C		0000000 0000000	00 0000000 00000000				
0000		HSSPIn_TX	(FIFO12[B,H,W]				
0x080		0000000 0000000	00 00000000 00000000				
0004		HSSPIn_TX	(FIFO13[B,H,W]				
0x084		0000000 0000000	00000000 00000000				
0x088		HSSPIn_TX	(FIFO14[B,H,W]				
0x066		0000000 0000000	00000000 00000000				
0,000		HSSPIn_TX	(FIFO15[B,H,W]				
0x08C		0000000 0000000	00000000 00000000				
0x090		HSSPIn_R	XFIFO0[B,H,W]				
0.090		0000000 0000000	00000000 00000000				
0x094		HSSPIn_R	XFIFO1[B,H,W]				
0.094		0000000 0000000	00000000 00000000				
0x098		HSSPIn_R	XFIFO2[B,H,W]				
0.090		0000000 0000000	00000000 00000000				
0x09C		HSSPIn_R	XFIFO3[B,H,W]				
0x09C		0000000 0000000	00000000 00000000				
0x0A0		HSSPIn_R	XFIFO4[B,H,W]				
ONONO		0000000 0000000	00 00000000 00000000				
0x0A4		HSSPIn_R	XFIFO5[B,H,W]				
UXU/A4		0000000 0000000	00 00000000 00000000				
0x0A8		HSSPIn_R	XFIFO6[B,H,W]				
UNUMO		0000000 0000000	00 00000000 00000000				
0x0AC		HSSPIn_R	XFIFO7[B,H,W]				
UNUAC		0000000 0000000	00000000 00000000				



Base_Address	Register				
+ Address	+3	+2	+1	+0	
0000		HSSPIn_RXI	FIFO8[B,H,W]		
0x0B0		00000000 00000000	00000000 00000000		
0004		HSSPIn_RXI	FIFO9[B,H,W]		
0x0B4		00000000 00000000	00000000 00000000		
0000		HSSPIn_RXF	FIFO10[B,H,W]		
0x0B8		00000000 00000000 00000000			
0000	HSSPIn_RXFIFO11[B,H,W]				
0x0BC		00000000 00000000	00000000 00000000		
0000		HSSPIn_RXF	FIFO12[B,H,W]		
0x0C0		00000000 00000000	00000000 00000000		
0004		HSSPIn_RXF	FIFO13[B,H,W]		
0x0C4		00000000 00000000	00000000 00000000		
0.000		HSSPIn_RXF	FIFO14[B,H,W]		
0x0C8		00000000 00000000	00000000 00000000		
0,000	HSSPIn_RXFIFO15[B,H,W]				
0x0CC	00000000 00000000 00000000 00000000				
0000		HSSPIn_CS	SCFG[B,H,W]		
0x0D0		0000 -	0000000000		
0.004		HSSPIn_CS	ITIME[B,H,W]		
0x0D4	11111111 11111111				
0.000	HSSPIn_CSAEXT[B,H,W]				
0x0D8	0000000 00000000 000				
0.000	HSSPIn_RDCSDC1[B,H,W] HSS		HSSPIn_RDC	SDC0[B,H,W]	
0x0DC	0000000	00000	00000000	0000	
0.050	HSSPIn_RD0	CSDC3[B,H,W]	HSSPIn_RDC	SDC2[B,H,W]	
0x0E0	0000000	00000	00000000	0000	
0054	HSSPIn_RD0	CSDC5[B,H,W]	HSSPIn_RDCSDC4[B,H,W]		
0x0E4	0000000	00000	00000000	0000	
0050	HSSPIn_RD0	CSDC7[B,H,W]	HSSPIn_RDC	SDC6[B,H,W]	
0x0E8	0000000	00000	000000000000		
0050	HSSPIn_WR0	CSDC1[B,H,W]	HSSPIn_WRC	SDC0[B,H,W]	
0x0EC	0000000	00000	00000000	0000	
0x0F0	HSSPIn_WR0	CSDC3[B,H,W]	HSSPIn_WRCSDC2[B,H,W]		
UXUFU	0000000	00000	000000000000		
0x0F4	HSSPIn_WR0	CSDC5[B,H,W]	HSSPIn_WRCSDC4[B,H,W]		
0.01 4	0000000	00000	00000000	0000	
0x0F8	HSSPIn_WR0	CSDC7[B,H,W]	HSSPIn_WRCSDC6[B,H,W]		
UXUFO	0000000	00000	00000000	0000	
0x0FC		HSSPIn_N	MID[B,H,W]		
0.01 0	•	00000000 00000000	00000110 00110000	<u> </u>	
0x100 - 0x3FC	-	-	-	-	
0x400	_			QDCLKR[B,H,W]	
0.400	-	<u>-</u>	-	1111	
0x404				DBCNT[B,H,W]	
UX4U4		<u>-</u>		00	
0x408 - 0xFFC	-	=	-	-	



1.48 HyperBus Interface

HyperBus Interface Base_Address : 0xD0A0_5000

Base_Address		Register					
+ Address	+3	+3 +2 +1 +0					
0x000		CSR[B,H,W]					
		0000					
0x004		-	3,H,W]				
		0	0				
0x008		ISR[i	3,H,W]				
CACCC			0	T			
0x024	-	-	-	-			
0x010		MBR0	[B,H,W]				
0,010		00000000 00000000	00000000 00000000				
0x014		MBR1	[B,H,W]				
0.014		00000000 00000000 00000000 00000000					
0x018	MCR0[B,H,W]						
0x016	00						
0,010		MCR1[B,H,W]					
0x01C		00	0011				
0000		MTR0	[B,H,W]				
0x020		0000000 0000000	0 000000000000				
0004		MTR1	[B,H,W]				
0x024	00000000 00000000 000000000000						
0000		GPOR	[B,H,W]				
0x028		00					
0020		WPR	B,H,W]				
0x02C		0					
0000		TEST	[B,H,W]				
0x030			0				
0x034- 0xFFC	-	-	-	-			



1.49 GDC Sub System Controller

GDC Sub System Controller Base_Address : 0xD0A0_0000

Base_Address	Register						
+ Address	+3	+2	+1	+0			
0×000		LockUr	nlock[W]				
0x000		00000000 00000000 00000000 00000000					
0x004		LockStatus[W]					
0x004			00				
0x008		*[W]				
0x00C		CnfigClock	«Control[W]				
0,000			001				
0x010			ıptEnable[W]				
0.010			11				
0x014		*[W]				
0x018			uptClear[W]				
			00				
0x01C			uptStatus[W]				
			00				
0x020			evSelect[W]				
		1					
0x024	VramRemapDisable[W]						
		0					
0x028	PanicSwitch[W]						
		1					
0x02C			kDivider[W]				
			00000000				
0x030			gerMask[W]				
			0000000 00000000				
0x034			ainStatus[W] 0000				
0x038							
0x036			-				
0.030		den Lock	:Unlock[W]				
0x040			00000000 00000000				
			(Status[W]				
0x044			00				
0x048	dsp0_ClockDivider[W] 01000001 11100000						
			ainControl[W]				
0x04C			0				
			ockShift[W]				
0x050			1				





Base_Address	Register				
+ Address	+3	+2	+1	+0	
0x054	*[W]				
0x058	dsp0_PowerEnControl[W]				
SASS	0				
0x05C	dsp0_ClockGateModeLock[W] 00000000 00000000 00000000				
0x060	dsp0_ClockGateControl[W]				
0x064			-		
0x068			-		
0x06C			-		
0x070			-		
0x074			-		
		SDRAMC C	lcokDivider[W]		
0x078			0 00000000		
		SDRAMC_Do	mainControl[W]		
0x07C			l0		
		HSSPIC_CI	ockDivider[W]		
0x080			00000000		
		HSSPIC_Dor	mainControl[W]		
0x084		1	·0		
		RPCC_Clc	okDivider[W]		
0x088			000		
2 222		RPCC_Dom	ainControl[W]		
0x08C		1	·0		
0x090			-		
0x094			-		
0x098			-		
0x09C	-				
0x100		vram_Loc	kUnlock[W]		
0.00		00000000 00000000	00000000 00000000		
0×104		vram_Loc	kStatus[W]		
0x104			00		
0v108		vram_srar	m_select[W]		
0x108			0000 00000000		
0x10C	*[W]				



Base_Address	Register			
+ Address	+3	+2	+1	+0
0x110	*[W]			
0x114	*[W]			
0x118		*[1	W]	
0x11C		*[1	W]	
0x120		*[1	W]	
0x124		*[W]		
0x128	*[W]			
0x12C	-			
0x130	-			
0x134	-			
0x138			-	
0x13C	vram_sberraddr_s0[W] 00000000 00000000 00000000			
0x140	vram_sberraddr_s1[W] 00000000 00000000 00000000			
0x144			-	
0x148	vram_arbiter_priority[W] 00000000			
0x14C-0xFFC	-			



1.50 GDC Sub System SDRAM Controller

GDC Sub System SDRAM Controller Base_Address : 0xD0A0_3000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000-0x0FF		-		
0x100		SDMODE[W] 0 0001001100-000		
0x104		REFTIM[W]0 00000000 00000000110011		
0x108		PWRDWN[W]		
0x10C		SDTIM[W] 000 01000010 00010001 010001		
0x110		SDCMD[W] 0		
0x114-0xFFC		-		

B. List of Notes



This section explains notes for each function.

1. Notes when High-speed CR is Used for the Master Clock



1. Notes when High-speed CR is Used for the Master Clock

This section explains notes when the high-speed CR is used for the master clock.

The frequency of the high-speed CR varies depending on the temperature and/or the power supply voltage.

The following table shows notes on each function macro when the high-speed CR is used for the master clock.

Furthermore, pay attention to notes when the high-speed CR is used as an input clock of the PLL and the master clock is selected for PLL.

■ Notes on Each Macro

Macro	Function/Mode	Notes
Internal Bus Clock	HCLK/FCLK/PCLK0/ PCLK1/PCLK2/ TPIUCLK	When the frequency of the high-speed CR is the maximum value, the setting of the internal operating clock frequency shall not exceed the upper limit specified in the "data sheet" for the product that you are using.
Timer	Multi-function Timer Base Timer Watch Timer Dual Timer Watch Dog Timer Quadrature	The frequency variation of the high-speed CR should be considered for the timer count value of each macro.
A/D Converter	Sampling Time Compare Time	Considering the frequency variation of the high-speed CR, the sampling time and the compare time of the A/D converter shall satisfy the specification specified in the "data sheet" for the product that you are using.
USB		
Ethernet-MAC		As the frequency accuracy does not meet the required
CAN	<u>-</u>	specification, these macros cannot be used when the
CAN-FD		high-speed CR is used for the master clock.
I ² S		
	UART	Even if the frequency of the high-speed CR is the minimum or the maximum value, the baud rate error should be considered. The baud rate error shall not exceed the limit.
	CSIO	The frequency variation of the high-speed CR should be
Multi-Function	I2C	considered for the communication of each macro.
Serial Interface	LIN	As the required frequency accuracy cannot be met, this function cannot be used as master. As a slave, the specified baud rate has more error at the maximum/minimum frequency of high-speed clock. So, if the error limit of the baud rate is exceeded, this function cannot be used.
Debug Interface	Serial Wire	As the frequency variation of the high-speed CR, the SWV(Serial Wire View) may not be used.
External Bus Interface	Clock Output	When the external bus clock output is used, the frequency variation of the high-speed CR should be considered for devices to be connected.
High-Speed Quad SPI	-	The frequency variation of the high-speed CR should be considered for devices to be connected.



Macro	Function/Mode	Notes
SD card Interface	-	The frequency variation of the high-speed CR should be considered for devices to be connected.
	Panel Output	
GDC	High-Speed Quad SPI	The frequency variation of the high-speed CR should be
GDC	HyperBus Interface	considered for devices to be connected.
	SDRAM Interface	

Major Changes



Spansion Publication Number: MN709-00003

Page	Section	Changes		
Revision 1.0				
=	-	Initial release		
Revision 2.0				
6 to 7	The target products in this manual	Added TYPE1-M4, TYPE2-M4, TYPE3-M4 product		
	12 -bit A/D Converter bit A/D			
10	Converter bit A/D Converter bit A/D	Added "DMA transfer triggered by an interrupt request"		
18	Converter bit	Added "DMA transfer triggered by an interrupt request"		
	1. Overview			
	12 -bit A/D Converter bit A/D			
41	Converter bit A/D Converter bit A/D	Devised the description of the companying		
41	Converter bit	Revised the description of the explanation		
	3.6 Starting DMA			
=	-	Company name and layout design change		
Revision 3.0				
4	Peripheral Manual	Added "GDC Part"		
8	The target products in this manual	Added TYPE4-M4		
84	CHAPTER1-3:A/D Timer Trigger	Added "The multiple A/D converters can use same start factor."		
	Selection			
Revision 4.0				
6 to 10	The target products in this manual	Added TYPE5-M4 and TYPE6-M4 and the other target products.		
8	The target products in this manual	Revised TYPE4-M4 Product list.		
91 to 104	CHAPTER 1-4: A/D Converter	Added a new chapter.		
	Offset Calibration			
252	Appendixes	Corrected Base Address of GDC Sub System SDRAM Controller		
	A. Register Map			
	1. Register Map			

NOTE: Please see "Revision History" about later revised information.

Revision History



Document Revision History

Document	Document Number: 002-04860				
Revision	ECN No.	Origin of Change	Description of Change		
**	-	УОНО	Migrated to Cypress and assigned document number 002-04860. No change to document contents or format.		
*A	5277501	УОНО	Update to Cypress template. CHAPTER 1-2: 12-bit A/D Converter Changed the continuous detection time "0 to 7" to "1 to7" in Range comparison function of 1. Overview. (Page 22) Changed "Upper limit threshold setting register0(ADRCUT0)" to "Upper limit threshold setting register(WCMPDH)" in Figure 3-8 and 3-9 of 3.5 Range Comparison Function. (Page 42, 43) Changed "Lower limit threshold setting register0(ADRCLT0)" to "Lower limit threshold setting register(WCMPDL)" in Figure 3-8 and 3-9 of 3.5 Range Comparison Function. (Page 42, 43) Changed "ADRCCS[n].RCOTS1,RCOTS0="008"" to "WCMPCR.RCOCD2-0="011"" in Figure 3-9 of 3.5 Range Comparison Function. (Page 43) Changed "ADRCCS[n]" to "WCMPCR" in Figure 3-9 of 3.5 Range Comparison Function. (Page 43) Changed "ADRCCS[n]" to "WCMRCIF" in Figure 3-9 of 3.5 Range Comparison Function. (Page 43) Changed "ADRCOT.RCOOF[n]" to "WCMRCOT.RCOOF" in Figure 3-9 of 3.5 Range Comparison Function. (Page 43) Changed "ADRCOT.RCOOF[n]" to "WCMRCOT.RCOOF" in Figure 3-9 of 3.5 Range Comparison Function. (Page 43) Changed "ADRCOT.RCOOF[n]" to "WCMRCOT.RCOOF" in Figure 3-9 of 3.5 Range Comparison Function. (Page 43) Changed "SyCLSL(")" to "ENBLTIME" in Figure 4-1 of 4. Setup procedure Example. (Page 47) Added Example of setting register in 4.5 Setting Conversion Time. (Page 52) Changed INVL initial value "X" to "1" in 5.5 Scan Conversion FIFO Data Register(SCFD). (Page 61) Changed INVL initial value "X" to "1" in 5.9 Priority Conversion FIFO Data Register(PCFD). (Page 67) Changed ENABLETIME[15:8] to ENBLETIME[15:8] in 5.16 A/D Operaton Enable Setup Register(ADCEN). (Page 76) Changed bit "[31:16]" to "[15:0]" in 5.20 Range Comparison Channel Select Register(WCMPSR). (Page 80) Changed bit "[70]" to "[15:0]" to 5.20 Range Comparison Channel Select Register(WCMPSR). (Page 81) CHAPTER 1-4: A/D Converter Offset Calibration Changed Sigure 3-1 in 3.1.1 Setting the Value for Offset Calibration. (Page 94) Changed the formula in 3.1.4 Calculation Setting Register(CALSR). (Page 102) A		

Revision History



Document Title: 32-Bit Microcontroller FM4 Family Peripheral Manual Analog Macro Part Document Number: 002-04860 Origin of Revision ECN No. **Description of Change** Change - Changed PCFD bit12 initial values "X" to "1" in 1.14 A/DC. (Page 143) Changed LVD_STR2 initial values "0-----" to "0-----" in 1.21 LDV. (Page 201) Changed CLK_SEL bit1 initial values "-" to "0" in 1.27 Wacrh Counter. (Page 205) Changed WTDIVEN initial values "-----00" to "-----00" in 1.28.3 TYPE5-M4 of 1.28 RTC. (Page 213) *B 5736989 AESATMP8 Updated logo and Copyright. Added and changed to "Preface" Added to the Note "Whether a peripheral function is on board or not is dependent on product type. See data sheets for details." (Page 3) Added "Microcontroller Support Information:" (Page 3) Changed "CHAPTER 1-2: 10-bit A/D Converter" to "12-bit" (Page 3) *C 6175054 **KTOM** Changed part numbers in Table 3, 5, 6 to 8 digits description. (Page 8) Changed part numbers in Table 4 to 9 digits description. (Page 7) Added and changed to " CHAPTER 1-2:12-bit A/D Converter" Changed the formula of "Sampling time" to "50 ns \times 2 x {(9 + 1) \times 4 + 3} = 4300 ns" (Page 74)