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Research Article

# Design and Implementation of Adaptive FIR filter using Systolic Architecture

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***Abstract***

*The tremendous growth of computer and Internet technology wants a data to be process with a high speed and in a powerful manner. In such complex environment, the conventional methods of performing multiplications are not suitable to obtain the perfect solution. To obtain perfect solution parallel computing is use in contradiction. The DLMS adaptive algorithm minimizes approximately the mean square error by recursively altering the weight vector at each sampling instance. In order to obtain minimum mean square error and updated value of weight vector effectively, systolic architecture is used. Systolic architecture is an arrangement of processor where data flows synchronously across array element. This paper demonstrates an effective design for adaptive filter using Systolic architecture for DLMS algorithm, synthesized and simulated on Xilinx ISE  Project navigator tool in very high speed integrated circuit hardware description language (VHDL) and Field Programmable Gate Arrays (FPGAs). Here, by combining the concept of pipelining and parallel processing in to the systolic.*

***Keywords:*** *Systolic Architecture, DLMS algorithm, VHDL, FPGA, Xilinx ISE*

## 1. Introduction

Adaptive digital filters (ADFs) are widely used in various signal-processing applications, such as, echo cancellation, system identification, noise cancellation and channel equalization etc.  Many of these applications require real-time adaptive filtering to implement the necessary functionalities with desired quality. For such applications the ADFs are therefore realized through dedicated VLSI systems. Amongst the existing ADFs least mean square (LMS)-based finite impulse response (FIR) adaptive filter is the most popular one due to its inherent simplicity and satisfactory convergence performance. However, the delay in availability of the feedback error for updating the weights according to the LMS algorithm does not favors its pipeline implementation under high sampling rate condition. For that purpose the delayed LMS (DLMS) algorithm for pipeline implementation of LMS.

### *1.1 Systolic architecture*

In computer architecture, a systolic architecture is a pipelined network arrangement of Processing Elements (PEs) called cells. It is a specialized form of parallel computing, where cells compute the data which is coming as input and store them independently. Systolic architecture represent a network a processing element (PEs) that rhythmically compute and pass data through the stem, the PEs regularly pump data in an out such that regular flow of data is maintained, as a result systolic array feature modularity and regularity which are important property for VLSI design. The systolic array may be use as a coprocessor in combination of host computer pass through PEs and the final result is return to host computer as shown in figure 1.1.

In order to achieve the high speed and low power demand in ASP applications, parallel array multipliers are widely used. In DSP applications, most of the power is consumed by the multipliers. Hence, low power multipliers must be designed in order to reduce the power dissipation.

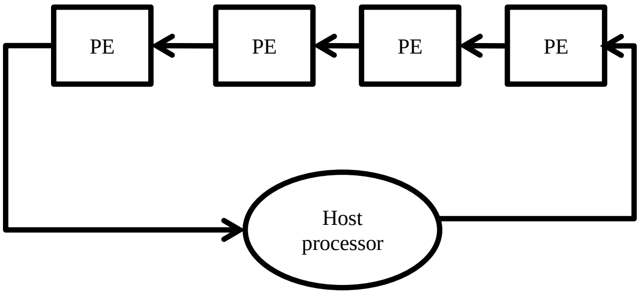

**Figure 1.1:** Basic Principle of systolic system

### *1.2 LMS (Least Mean Square) Algorithm*

The LMS adaptive algorithm minimizes approximately the mean-square error by recursively altering the weight vector at each sampling instance. Thus an adaptive FIR

*Corresponding author **Ravi H Bailmare** and **Pravin V Kinge** are ME students and **S.J.Honale** is a Faculty Member digital filter driven by the LMS algorithm can be described in vector form as

$$y(n)=W^T(n)X(n)$$
$$e(n)=d(n)-y(n)$$
$$W(n+1)=W(n)+\mu e(n)X(n)$$

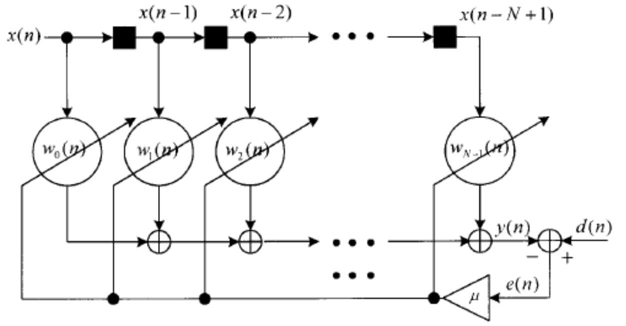

**Figure1.2:** Block diagram of an adaptive FIR digital filter driven by LMS algorithm

Where *d(n*) and *y(n*)denote the desired signal and output signal, respectively. The step-size *μ* is used for adaptation of the weight vector, and e(n) is the feedback error. In the above equations, the tap-weight vector *w(n)* and the tap-input vector *x(n)* are defined as.

$$W(n) = [w_0(n), w1(n),\ldots, wn_{-1}(n)]^T$$
$$X(n) =[x(n), x(n-1),\ldots, x(n-N+1)]^T$$

Where *N* is the length of an FIR digital filter and $[\bullet]^t$ denotes the transpose operator. The block diagram of the LMS adaptive FIR digital filter is depicted in figure 1.2 here the symbol ■ denotes the unit delay element. In this utilize the algebra for the design of a systolic-array implementation for adaptive filters based on the LMS algorithm. However, since the LMS algorithm contains a feedback loop, the delays created in the decomposition and retiming process prohibit the exact implementation of the algorithm. The design procedure leads to a systolic array which implements a special case of the so-called delayed LMS (DLMS) algorithm. The error ***e(n)*** used in this algorithm is available only after the processing delay of the systolic array, and thus, the update of the coefficients is performed with this delay.

### *1.3 DLMS (Delayed Least Mean Square) Algorithm*

LMS algorithm uses the feedback-error corresponding to the *n*th iteration for updating the filter weights to be used for computing the filter output for the (*n*+1)Th iteration. The DLMS algorithm is similar to the LMS algorithm, except that in case of DLMS algorithm, the weight increment terms to be used in the current iteration are estimated from the error value and input samples corresponding to a past iteration. Figure 1.3 shows the structure of conventional DLMS algorithm. The weight update equation algorithm is given by,

$$W(n+1) =W(n) +\mu e(n-D)X(n-D)$$

here *D* is the number of iterations by which the adaptation is delayed.

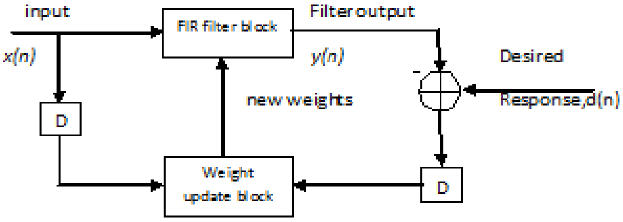

**Figure 1.3**: Conventional DLMS algorithm

## 2. Related Work

1. One of the important implementation i.e. Conversion of the delayed LMS algorithm into the LMS algorithm. they shown in which way the delayed LMS (DLMS) algorithm can be transformed into the standard LMS algorithm at only slightly increased computational expense (R. D. Poltmann, 1995).
2. Another important implementation, An Efficient Systolic Architecture for the DLMS Adaptive Filter and Its Applications. In this paper an efficient systolic architecture for the delay least-mean-square (DLMS) adaptive finite impulse response (FIR), digital filter based on a new tree-systolic processing element (PE) and an optimized tree-level rule. It provide comprehensive comparison results for different -tap adaptive FIR filter structure and verify our systolic-array architecture of adaptive equalization and system identification applications ( Lan-Da Van, Wu-Shiung Feng, 2001).
3. Another important implementation, VHDL Generation of Optimized FIR Filters, this paper a near optimum algorithm for constant coefficient FIR filters was used. This algorithm uses general coefficient representation for the optimal sharing of partial products in Multiple Constants Multiplications (MCM). The software implementation was developed in C language and produces VHDL code for the optimized FIR filter from a coefficient specification file. The developed software was applied to several FIR filters and compared to Matlab's Filter Design & Analysis (FDA). The FDA toolbox includes a feature to generate optimized VHDL code from the generated coefficients and was used to compare to the developed software ( Fábio Fabian Daitx, Vagner S. Rosa, Eduardo Costa, Paulo Flores, Sérgio Bampi, 2008).
4. Another important implementation, A High-Speed FIR Adaptive Filter Architecture using a Modified Delayed LMS Algorithm. In this paper, a modified delayed least means square (DLMS) adaptive algorithm to achieve lower adaptation-delay. Authors proposed an efficient pipelined architecture for the implementation of this adaptive filter. They shown that the proposed DLMS adaptive filter can be implemented by a pipelined inner-product computation unit for calculation of feedback error, and a pipelined weight-update unit consisting of N parallel multiplies accumulators, for filter order N. They suggested a modified DLMS adaptive algorithm to achieve less adaptation-delay compared with the conventional DLMS algorithm, and shown that the

proposed DLMS algorithm can be implemented efficiently by a pipelined inner product computation unit and parallel and pipelined weight update unit using carry-save reductions. Substantial reduction of adaptation-delay, ADP and EPS over the existing structures has been achieved by the proposed design (Pramod K. Meher, Megha Maheshwari, 2011).

5. Another important implementation, A New Pipelined Architecture for the DLMS Algorithm. This paper presents a design of a systolic array architecture for the 1-dimensional Finite Impulse Response adaptive filter. The design is based on the Delayed Least Mean Squares algorithm (DLMS). The performance of the proposed design is analyzed in terms of speed up, adaptation delay and throughput. The different N-tap 1 -D adaptive filters are analyzed and it is shown that the proposed scheme is superior in terms of adaptation delay, speed and throughput without the need for additional hardware (K.R.Santha, V Vaidehi, 2005).
6. Another important implementation, Efficient Systolic Architectures for l-D and 2-D DLMS Adaptive Digital. Two efficient ***N***$^{th}$ tap 1-D and window size *N* x *N* 2-D systolic adaptive digital filters utilizing the tree-systolic PE has been presented in this paper. Under considering maximum number of tap-connections of the feedback error signal, the practical rule to decide the optimized tree level without sacrificing the systolic characteristics is provided. At last, they verify I-D and 2-D efficient systolic architectures via applications of adaptive equalizer and image restoration (Lan-Da Van, Wu-Shiung Feng, 2000).
7. Another important implementation, A Systolic Architecture for LMS Adaptive Filtering with Minimal Adaptation Delay. This paper presents a systolic architecture with minimal adaptation delay and input/output latency, thereby improving the convergence behavior to near that of the original LMS algorithm. The architecture is synthesized by using a number of function preserving transformations on the signal flow graph representation of the delayed LMS algorithm. With the use of carry-save arithmetic, the systolic folded pipelined architecture can support very high sampling rates, Elimited only by the delay of a full adder (S. Ramanathan, V. Visvanathan, 1996).
8. Another important implementation, Delayed Block LMS Algorithm and concurrent architecture for high-speed implementation of Adaptive FIR Filter. In this paper, proposed the DBLMS algorithm which takes a block of *L* input samples and yields a block of *L* outputs in every training cycle. The simulation result shows that the performance of DBLMS algorithm is equivalent to that of the DLMS algorithm. However, the DBLMS algorithm offers *L* fold higher parallelism compared with the DLMS algorithm. We have utilized the inherent parallelism in DBLMS algorithm to derive a highly concurrent systolic-like architecture for high-speed implementation of adaptive FIR filter. The proposed structure can provide *L* times higher throughput compared with the existing pipelined structures (Basant K. Mohanty, Promod K.Meher).
9. Another important implementation, Performance Evaluation of LMS and DLMS Digital Adaptive FIR Filters by Realization on FPGA. In this paper implement the adaptive digital Least Mean Square (LMS) and delayed-LMS (DLMS) Finite Impulse Response (FIR) filters on Field Programmable Gate Array (FPGA) chips for typical noise cancellation applications and compare the behavior of LMS and DLMS adaptive algorithms in terms of chip area utilization and the filter critical path time or filter frequency. The direct FIR architecture is considered for filter designing and the VHDL hardware description language is used for algorithm modeling. Demonstrate that the DLMS algorithm which has a pipeline architecture is faster than LMS algorithm while it uses more chip area due to using extra registers (Hesam Ariyadoost, Yousef S. Kavian, Karim Ansari-As, 2011)

## 3. Proposed Work

Proposed work use Systolic Array architecture, which consist of no of processing element connected to one another, basic processing element of systolic architecture is as shown in figure 3.1.

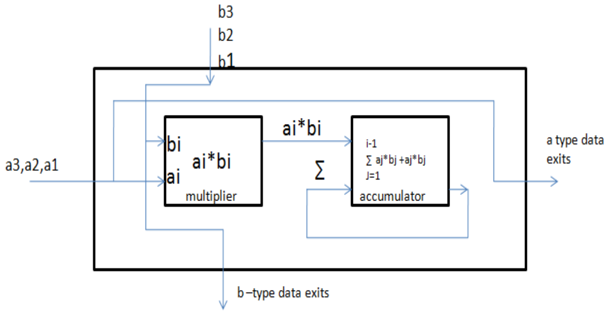

**Figure 3.1:** PE of systolic Architecture

Where A, B and C are the matrices with order m x k , k x n , and m x n respectively. Each PE of systolic array computes the multiplication of elements and accumulates to the corresponding element and then elements will be passed to neighbor PE in the systolic array. First elements αi,j in row i of matrix A are injected first into PE as pipeline with the sequence αi,k of and the input time to the element of αi+1,j is one time unit later than αi,j . Similarly, elements bi,j in column j of matrix B are injected first into PE as pipeline with the sequence of bk,j and the input time to the element of the sequence of bk,j+1is one time unit later than of bk,j .

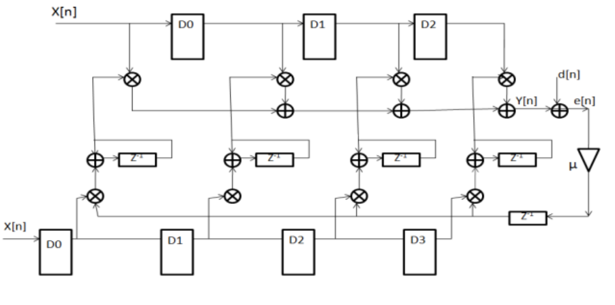

**Figure 3.2:** Direct form of DLMS adaptive FIR filter

The architecture of PE in this approach is shown in figure 3.1 which performs the Multiplication and Accumulation on data.

Figure 3.2 shows the direct forms of DLMS FIR filters, which mainly consists of shift registers, adders and multipliers. The signal samples are multiplied by filter coefficients and are gathered together in the adder block. The DLMS FIR filter consists of some registers in feedback line.

Figure 3.3 shows highly realizable systolic architecture of the DLMS adaptive digital filter. Where $z^{-1}$ denotes a unit delay, we insert a unit delay element in the feedback path so as to maintain the lowest critical period. And observe that when *p* is equal to zero, this architecture can be reduced to a fully pipelined architecture .On the other hand, if *p* is greater than zero, this architecture performs better convergence sacrificing systolic features.

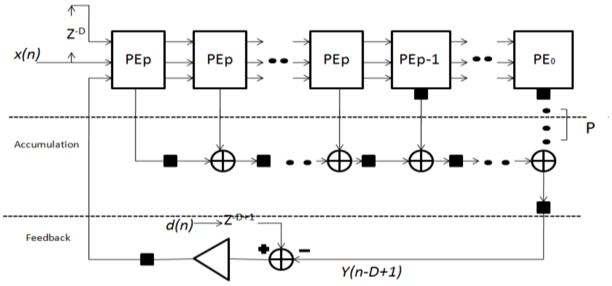

**Figure 3.3:** Systolic architecture with cascaded systolic-tree PEs

Architecture for realization of Adaptive FIR filter using DLMS algorithm consist of no. of PE's connected to one another. No of PE's is equal to no of Taps of an FIR filter, Propose work design for 4-Tap Fir filter therefore no PE's equal to 4. If Taps of filter increase then no of PE's increase. This architecture is use for obtaining mean square error. This MSE is again use for obtaining updated value of weight coefficient and the procedure is continuous until we get minimum MSE. Shows different simulation result and find out time require for obtaining minimum MSE for different input, and desired output combination.

## 4. Simulation Result

The simulation results for realization of adaptive digital FIR filters using DLMS algorithm on FPGA chip are presented and the performances of DLMS algorithm is obtain in terms of chip area utilization and time require for minimum MSE.

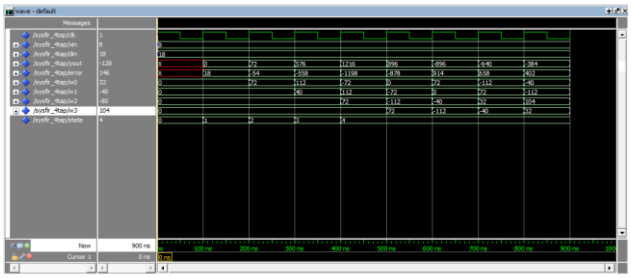
```
wave - default
Messages
/sysfir_4tap/clk     1
/sysfir_4tap/xin     8
/sysfir_4tap/din     18
/sysfir_4tap/yout    -128
/sysfir_4tap/error   146
/sysfir_4tap/w0      32
/sysfir_4tap/w1      -40
/sysfir_4tap/w2      -80
/sysfir_4tap/w3      104
/sysfir_4tap/state   4
Now                  900 ns
Cursor 1             0 ns
```

**Figure 4.1: S**imulation result for Xin=8 and Din=18

The digital adaptive filters were modeled by VHDL and implemented on Spartan 3 FPGA family. The Xilinx and modelsim software was used for synthesize and simulation of VHDL codes.

Initially the filter weights w0, w1, w2, and w3 are assumed to be zero and obtain the updated value for reducing the error using the inputs information and error values. In these simulation results the learning factor was assumed to be μ=0.5. Simulation result for different input and desired output combination are as shown in figures.

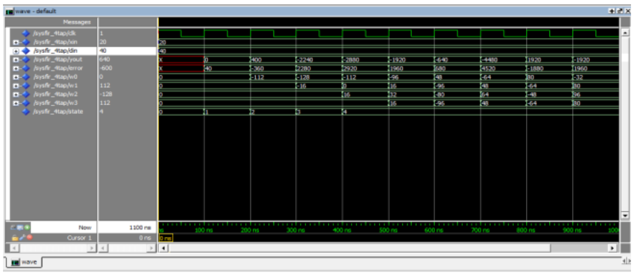
```
wave - default
Messages
/sysfir_4tap/clk     1
/sysfir_4tap/xin     20
/sysfir_4tap/din     40
/sysfir_4tap/yout    640
/sysfir_4tap/error   -600
/sysfir_4tap/w0      0
/sysfir_4tap/w1      112
/sysfir_4tap/w2      -128
/sysfir_4tap/w3      112
/sysfir_4tap/state   4
Now                  1100 ns
Cursor 1             0 ns
```

**Figure 4.2:** Simulation result for Xin=20 and Din=40

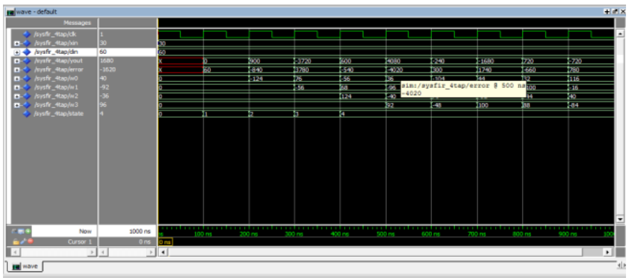
```
wave - default
Messages
/sysfir_4tap/clk     1
/sysfir_4tap/xin     30
/sysfir_4tap/din     60
/sysfir_4tap/yout    1680
/sysfir_4tap/error   -1620
/sysfir_4tap/w0      40
/sysfir_4tap/w1      -92
/sysfir_4tap/w2      -36
/sysfir_4tap/w3      96
/sysfir_4tap/state   4
Now                  1000 ns
Cursor 1             0 ns
```

**Figure 4.3:** Simulation result for Xin=30 and Din=60

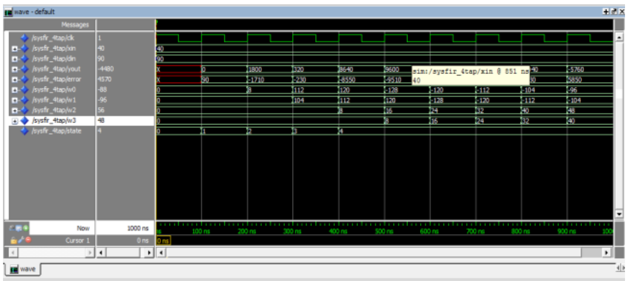
```
wave - default
Messages
/sysfir_4tap/clk     1
/sysfir_4tap/xin     40
/sysfir_4tap/din     90
/sysfir_4tap/yout    -4480
/sysfir_4tap/error   4570
/sysfir_4tap/w0      -88
/sysfir_4tap/w1      -96
/sysfir_4tap/w2      56
/sysfir_4tap/w3      48
/sysfir_4tap/state   4
Now                  1000 ns
Cursor 1             0 ns
```

**Figure 4.4:** Simulation result for Xin=40 and Din=90

Synthesis result for adaptive FIR filter using Xilinx is as shown in table 4.1.

**Table 4.1:** Synthesis Result

| Sr. no | Parameters | Utilization |
|---|---|---|
| 1 | No. of slices | 179 |
| 2 | Minimum period | 19.408 ns |
| 3 | Power supply | 0.060(W) |

## Conclusion

Systolic architecture can be used for design of multiplier, matrix multiplication & many DSP application i.e. RLS algorithm, LMS algorithm and FIR filter. Low adaptation delay architecture for implementation of DLMS adaptive filter is achieved by using an efficient implementation of systolic array structure by involving the concept of pipelining and parallel processing in order to reduce adaption delay, chip area and power consumption to a great extent. Design shows different adaption delay, chip area and power consumption for different input and desired output combination. The proposed structure significantly involves less adaption delay chip area and power consumption as compared to the existing structures. Systolic architecture of DLMS algorithm is design and implemented using Xilink ISE Project navigator tool and achieved the improved performance over the existing design.

## Reference

R. D. Poltmann 1995, Conversion of the delayed LMS Algorithm into the LMS algorithm, *IEEE Signal Processing Lett*, vol. 2, p. 223.

Lan-Da Van, Wu-Shiung Feng 2001, An Efficient Systolic Architecture for the DLMS Adaptive Filter and Its Applications, *IEEE transaction on circuit and system-II,* VOL.48, NO 4.

Fábio Fabian Daitx, Vagner S. Rosa, Eduardo Costa, Paulo Flores, Sérgio Bampi 2008, VHDL Generation of Optimized FIR Filters, *international conference on signal and system.*

Pramod K. Meher, Megha Maheshwari 2011, A High-Speed FIR Adaptive Filter Architecture using a Modified Delayed LMS Algorithm, *IEEE* 978-1-4244-9474-3/11/00.

K.R.Santha, V Vaidehi 2005, A New Pipelined Architecture for the DLMS Algorithm, *IEEE Indicon 2005 Conference, Chennai, India.*

Lan-Da Van, Wu-Shiung Feng 2000, Efficient Systolic Architectures for l-D and 2-D DLMS Adaptive Digital, *IEEE* 0-7803-6253-5/00/.

S. Ramanathan, V. Visvanathan 1996, A Systolic Architecture for LMS Adaptive Filtering with Minimal Adaptation Delay, *9th International Conference on VLSI Design.*

Basant K. Mohanty, Promod K.Meher, Delayed Block LMS Algorithm and concurrent architecture for high-speed implementation of Adaptive FIR Filter.

Hesam Ariyadoost, Yousef S. Kavian, Karim Ansari-As 2011, Performance Evaluation of LMS and DLMS Digital Adaptive FIR Filters by Realization on FPGA, *International Journal of Science & Emerging Technologies,* Vol-1 No. 1.

Bairu K. Saptalakar, Deepak kale, Mahesh Rachannavar, Pavankumar M. K. 2013, Design and Implementation of VLSI Systolic Array Multiplier for DSP Applications, *International Journal of Scientific Engineering and Technology (*ISSN: 2277-1581) Volume 2 Issue 3, PP : 156-159 1.

Purushothaman A, Dr.C.Vijaykumar 2011, Implementation of Low power systolic based RLS adaptive Filter using FPGA, *IEEE.*

Mahendra Vucha, Arvind Rajawat 2011, Design and FPGA Implementation of Systolic Array Architecture for Matrix Multiplication, *International Journal of Computer Applications*, (0975 – 8887) Volume 26– No.3.

C. Wenyang, L. Yanda. and J. Yuc 1991, Systolic Realization for 2D Convolution Using Conrigurable Functional Method in VLSI Parallel Array Designs, *Proc. IEEE, Computer und Digital Technology,* Vol. 138, No. 5, pp. 361- 370.

Peter Mc Curry, Fearghal Morgan, Liam Kilmartin 2001, Xilinx FPGA implementation of a pixel processor for object detection applications, In the Proc. *Irish Signals and Systems Conference,* Volume 3, Page(s), 346 – 349.

Feifei Dong, Sihan Zhang and Cheng Chen 2009, Improved Design and Analyze of Parallel Matrix Multiplication on Systolic Array Matrix, *IEEE*.

H. Herzberg, R. Haimi-Cohen, and Y. Be’ery 1992, A systolic array realization of an LMS adaptive filter and the effects of delayed adaptation, *IEEE Trans. Signal Processing*, vol. 40, pp. 2799–2803.

M. D. Meyer and D. P. Agrawal 1993, A high sampling rate delayed LMS filter architecture, *IEEE Trans. Circuits Syst. II*, vol. 40, pp. 727– 729.

H. T. Kung 1982, *Why systolic architectures*, *IEEE Computer*, vol. 15, pp. 37.