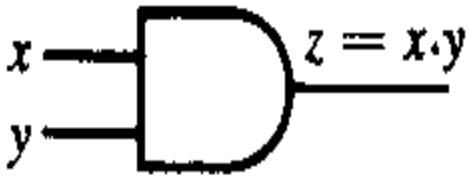
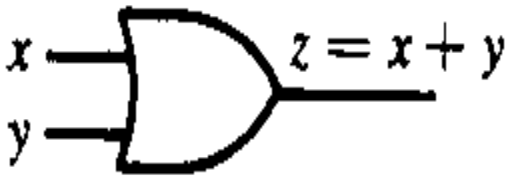
Basic Logic Gates

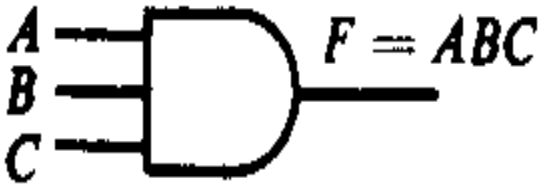


(a) Two-input AND gate

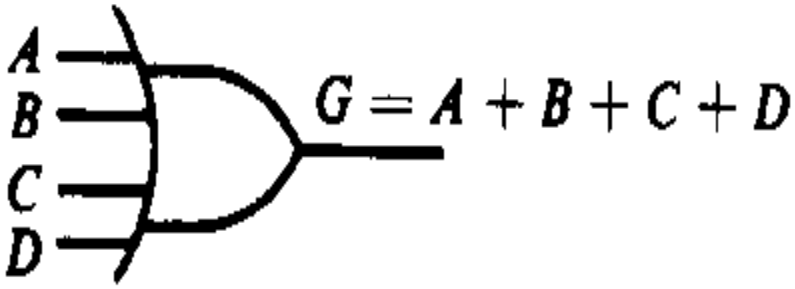


(b) Two-input OR gate

(c) NOT gate or inverter



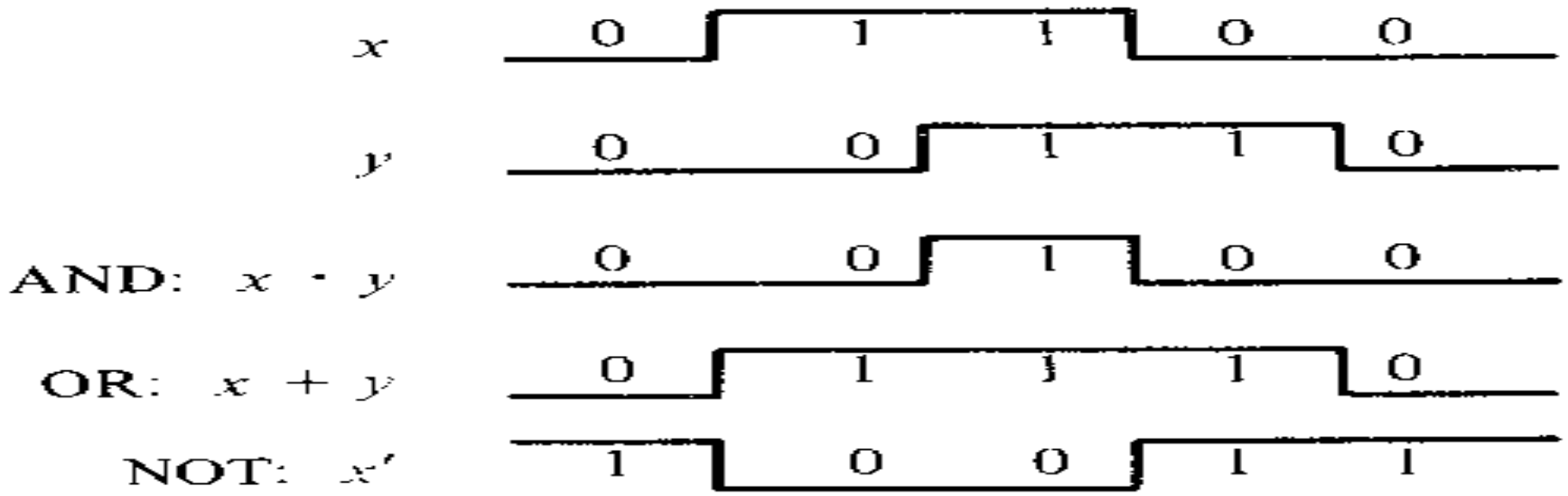
(d) Three -input AND gate

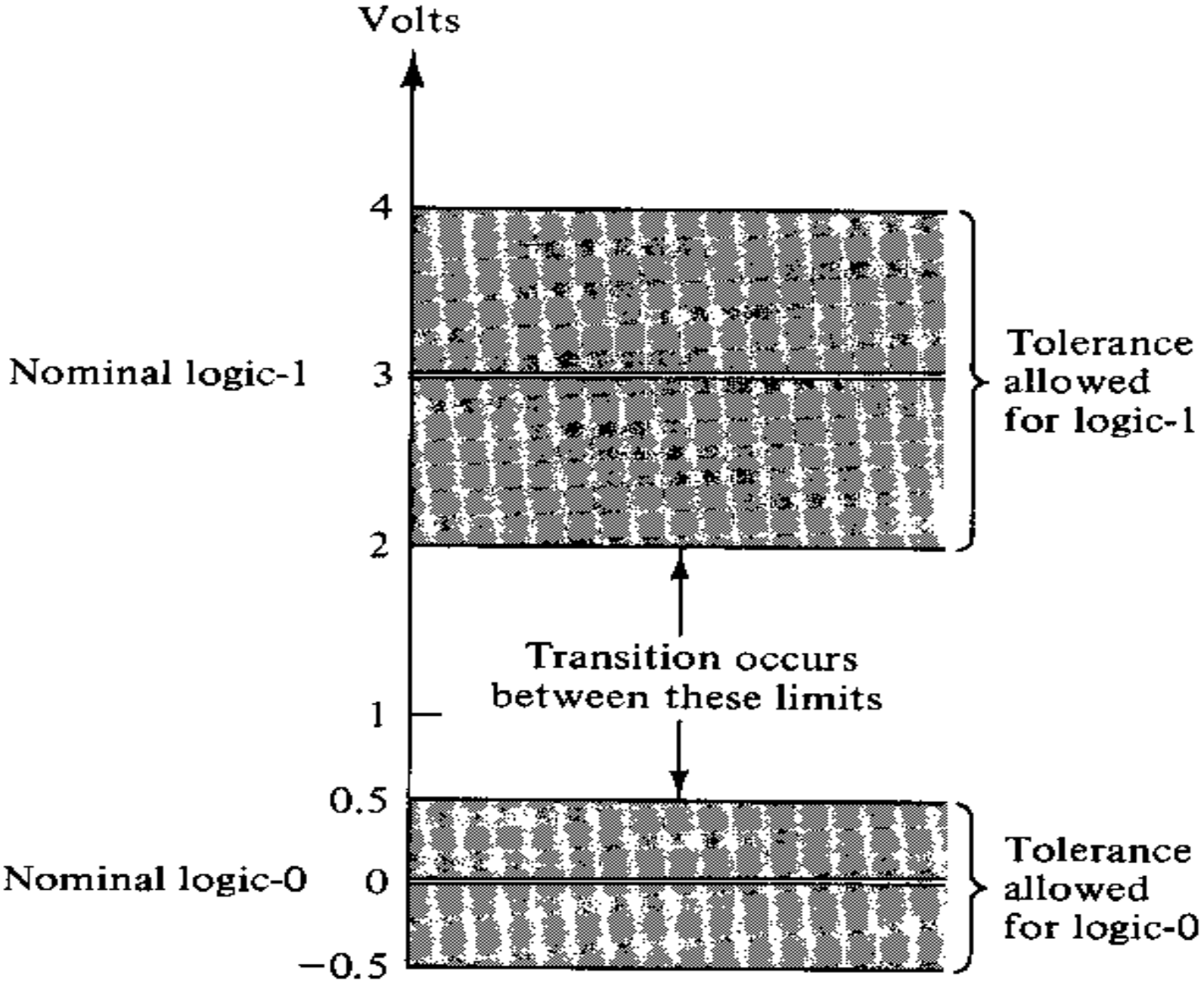


(e) Four -input OR gate

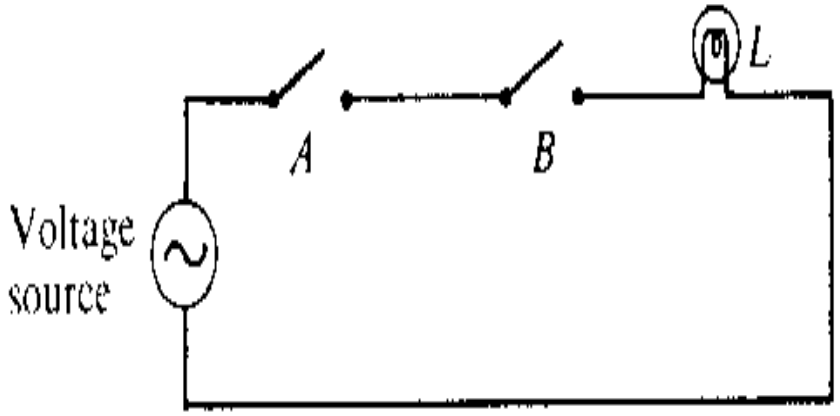
Truth Tables of Logical Operations

AND			OR			NOT	
x	y	$x \cdot y$	x	y	$x + y$	x	x'
0	0	0	0	0	0	0	1
0	1	0	0	1	1	1	0
1	0	0	1	0	1		
1	1	1	1	1	1		

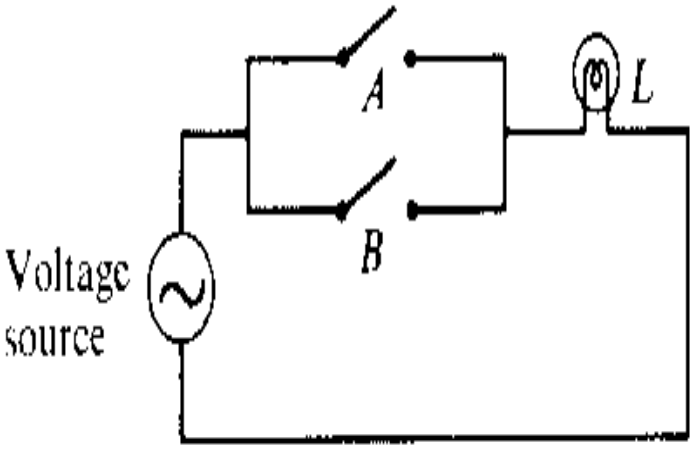



Volts
4
3
2
1
0.5
0
−0.5
Nominal logic-1
Nominal logic-0
Tolerance allowed for logic-1
Tolerance allowed for logic-0
Transition occurs between these limits

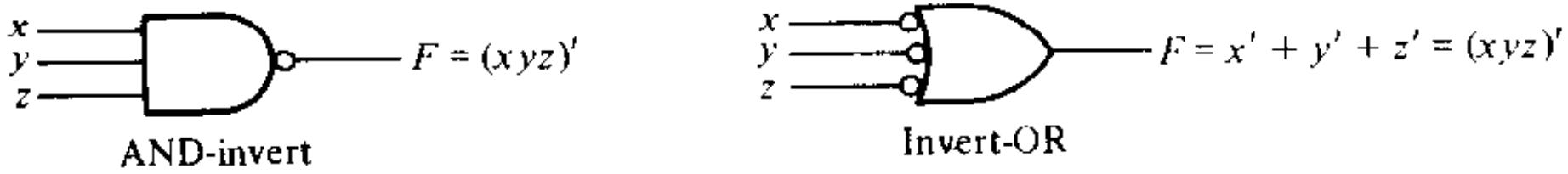
Electronic digital circuits are also called *logic circuits* because, with the proper input, they establish logical manipulation paths. Any desired information for computing or



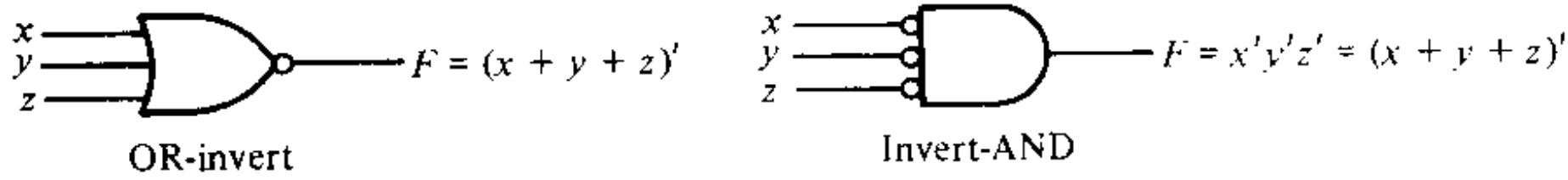
(a) Switches in series – logic AND



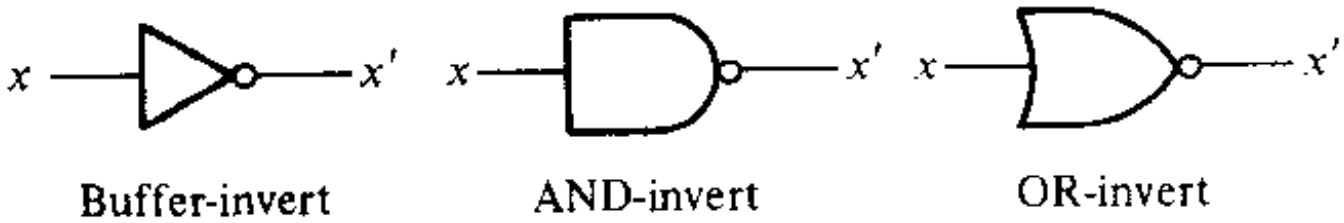
(b) Switches in parallel – logic OR



(a) Two graphic symbols for NAND gate.



(b) Two graphic symbols for NOR gate.



(c) Three graphic symbols for inverter.

Transistor Logic Circuits

Transistor Logic Circuits

Transistorized digital circuits basically fulfill the three logical functions of AND (or NAND) gating, OR (or NOR) gating, and signal inversion (NOT gate). An additional function usually performed, though not logical in nature but nevertheless a practical necessity, is signal amplification. Other logical blocks, such as NOR, NAND, and flip-flops, are easily obtained using these three fundamental functional blocks. Several different circuit configurations can be used for these functional blocks.

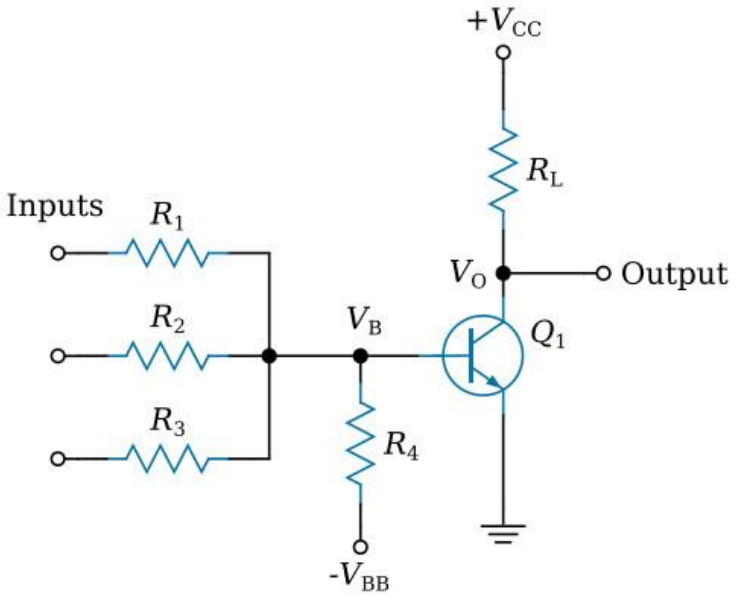
Resistor-Transistor Logic (RTL)

Resistor-transistor logic (RTL) is constructed from resistors and transistors. The RTL circuit is one of the basic logic circuits in digital logic families. It is a bipolar saturated device. The RTL logic is popular because of its simplicity. The RTL circuit consists of resistors at inputs and transistors at the output side. Transistors are used as the switching device. The emitter of the transistor is connected to the ground. The collector terminals are tied together and given to the supply through the resistor RC. The collector resistor is known as a passive pull-up resistor.

Resistor-Transistor Logic (RTL)

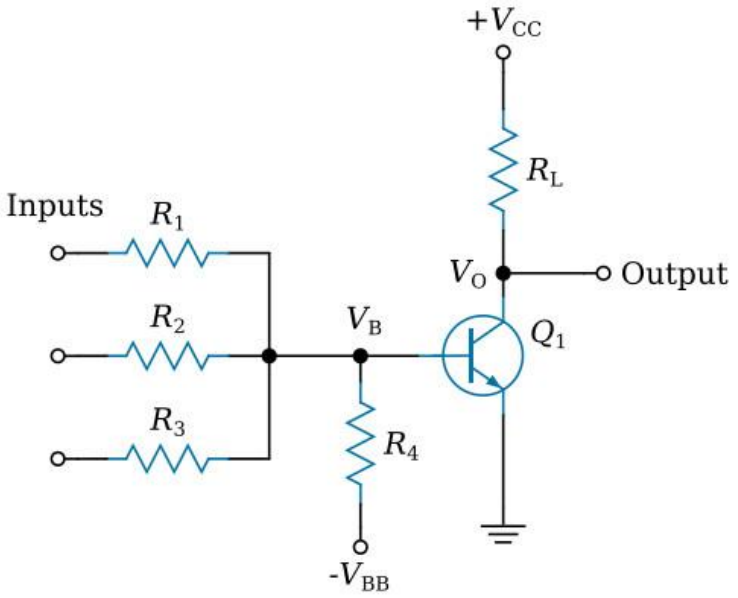
One-Transistor RTL Gate

The figure shows a simple 3-input RTL circuit which is a NOR gate. The circuit has each input combined through a coupling resistor (R_1, R_2, or R_3) and fed to the base of Q_1. The coupling resistors provide isolation that is less effective than that provided by transistors or diodes. This isolation makes the RTL sensitive to the value of the coupling resistors and the number of inputs (fan-in).



Resistor-Transistor Logic (RTL)

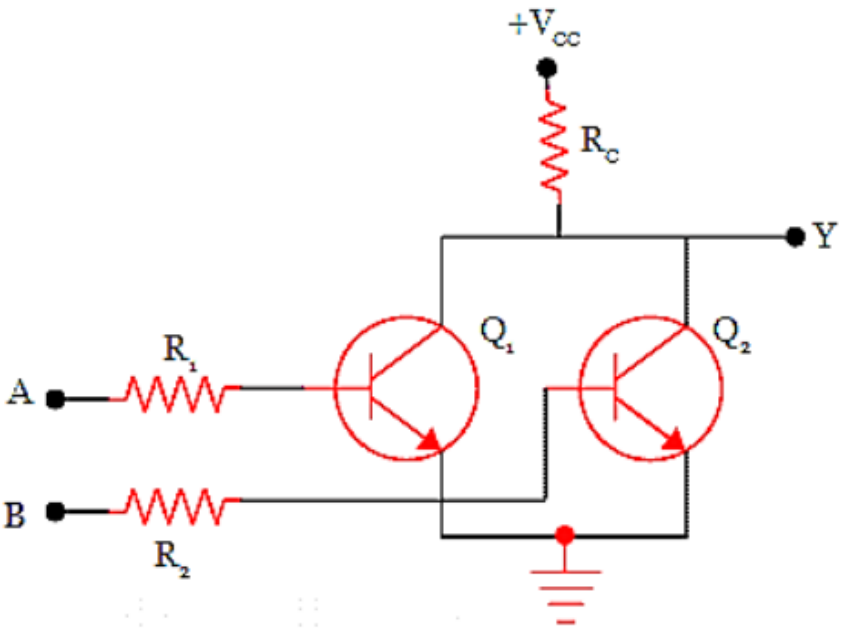
One-Transistor RTL Gate



The operation of the circuit is quite simple. When all three inputs are zero, the voltage V_B at the base of the transistor Q_1 is slightly more negative than ground since the base is tied to a negative voltage, $-V_{BB}$ through resistor R_4. Q_1 is cut off and the output voltage V_0 tends to fall to the supply voltage $+V_{CC}$. If any of the three inputs are positive, the current flow through its corresponding resistor pulls the voltage V_B to some positive value. This drives Q_1 into saturation. Here, the output voltage V_0 is determined by the saturation voltage $V_{CE(SAT)}$ of Q_1.

Resistor-Transistor Logic (RTL)

Two-Transistor RTL Gate



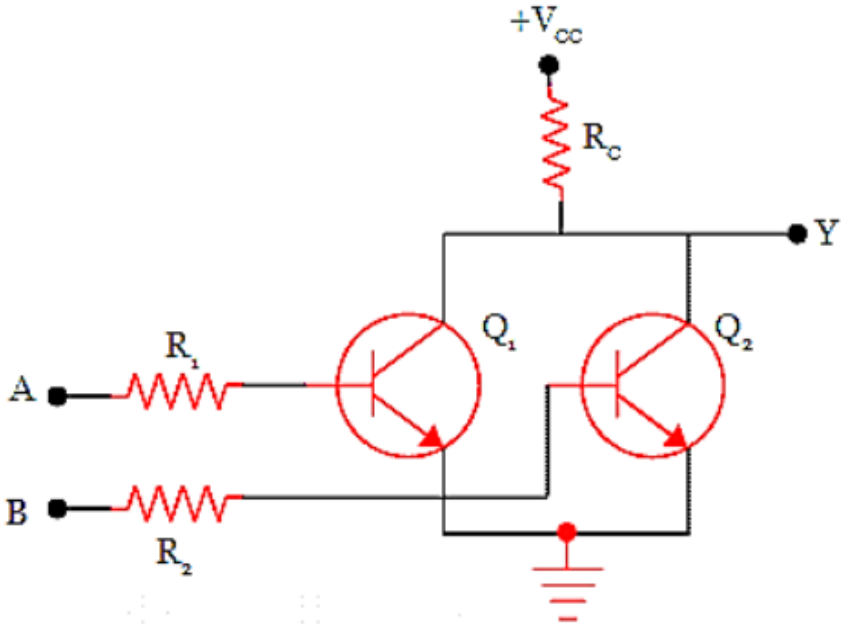
When both the inputs A and B are at 0V or logic 0, it is not enough to turn on the gates of both the transistor. So the transistors will not conduct. Due to this, the voltage +VCC will appear at the output Y. Hence the output is logic 1 or logic HIGH at terminal Y. When any one of the inputs, either A or B is given HIGH voltage or logic 1, then the transistor with HIGH gate input will be turned on. This will mak a path for the supply voltage to go to the ground through the resistor RC and transistor. Thus there will be 0 v at the output terminal Y. When both the inputs are HIGH, it will drive both the transistor to turn on. It will make a path for the supply voltage to flow to the ground through resistor RC and transistor. Therefore, there will be 0 v at the output terminal Y.

Resistor-Transistor Logic (RTL)

Two-Transistor RTL Gate

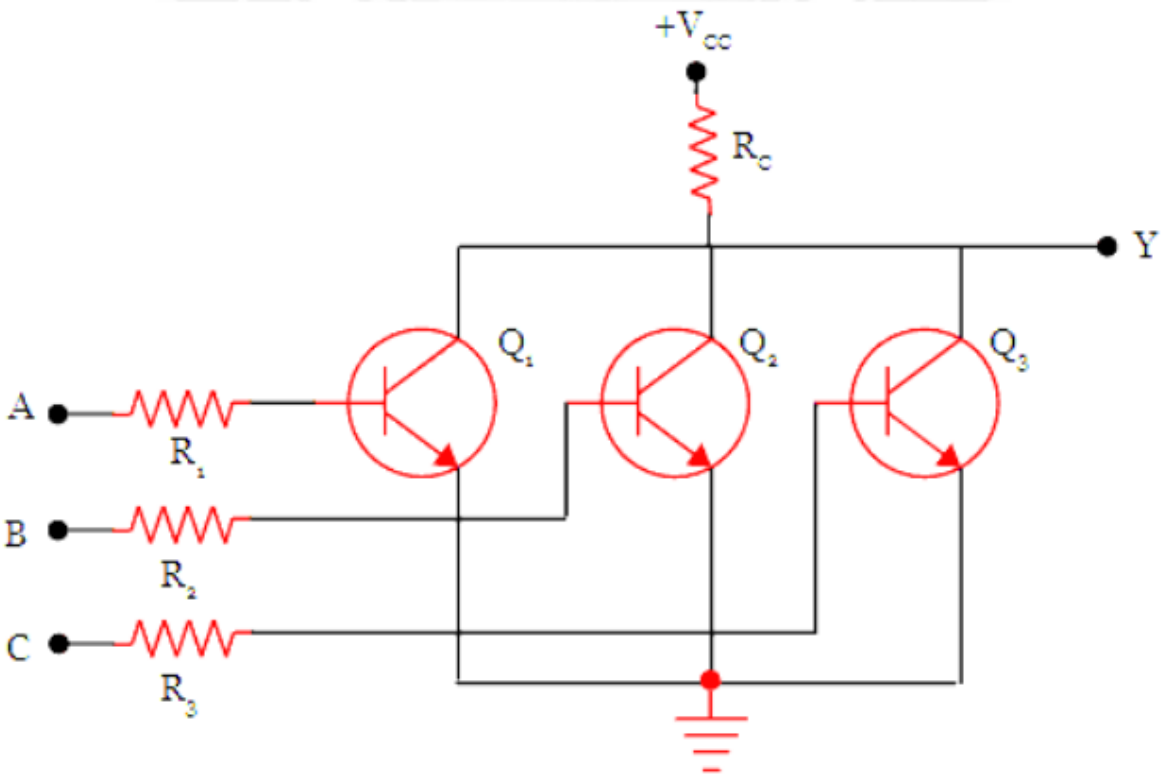
Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table – Nor Gate



Resistor-Transistor Logic (RTL)

Three-Transistor RTL Gate



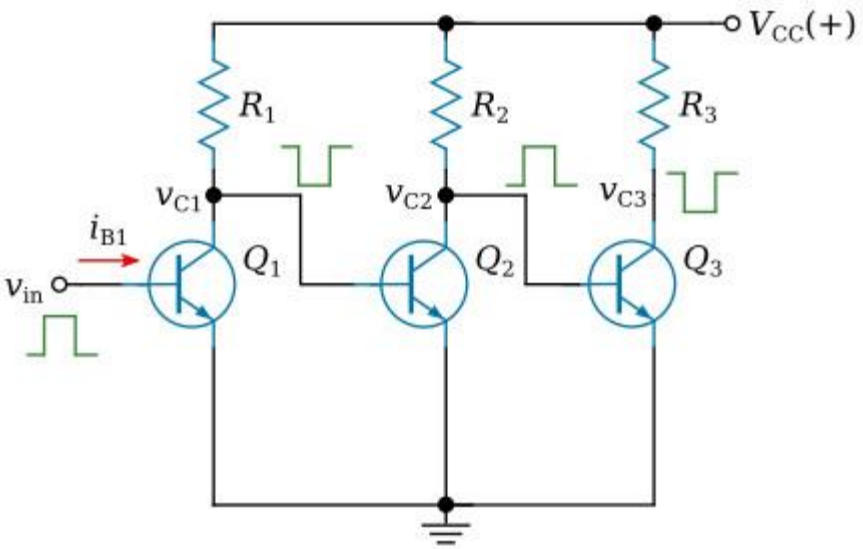
Resistor-Transistor Logic (RTL)

Limitations:

When the transistor is switched on, the power dissipation increases as the current flows through base and collector. Also, the RTL gate has poor noise margin, poor fan-out and the propagation delay is more

Direct-Coupled Transistor Logic (DCTL)

DCTL Inverters



The figure shows three DCTL inverters in cascade. In this circuit the collector resistors R_1, R_2, and R_3 serve as constant current sources.

They supply current to their respective transistors' collectors, when they are on or to the base of the next transistor when they are off.

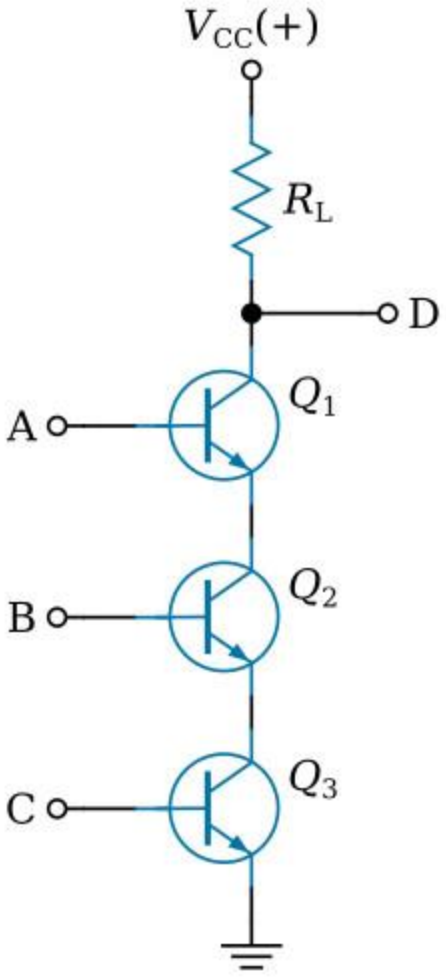
Direct-Coupled Transistor Logic (DCTL)

DCTL Series Gating

The figure below shows three transistors connected in series to form a NAND gate for positive input signals A, B, and C. If any of the three transistors is off, the output voltage at D will be the supply voltage (V_{CC}) in the unloaded condition. Under loaded conditions, the voltage at D will depend on the resistor R_L and the $V_{BE(ON)}$ of the next stage transistor. When all three transistors are on, the potential at D will be closer to ground than in the previous case and will be the sum of the $V_{CE(SAT)}$ of Q_1, Q_2, and Q_3 in series. Consequently, the principal disadvantage of this configuration is the necessity to insure that the next stage transistor will be off when all three transistors are on. The sum of the three $V_{CE(SAT)}$ in series must be less than $V_{BE(ON)}$ of the next stage transistor. One means of accomplishing this is to supply more base drive to Q_1, Q_2, and Q_3, thereby drawing them further into saturation and lowering the saturation resistance.

Direct-Coupled Transistor Logic (DCTL)

DCTL Series Gating



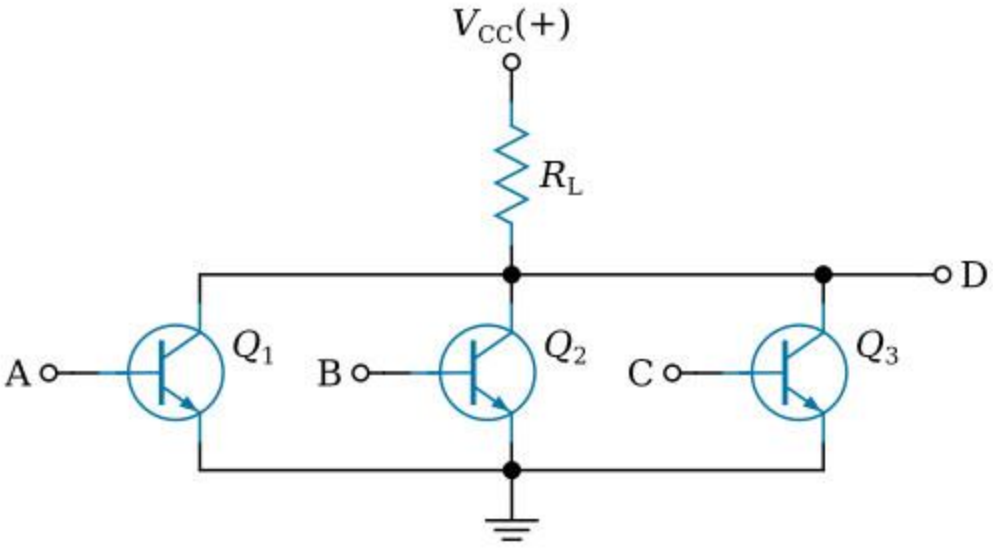
Direct-Coupled Transistor Logic (DCTL)

DCTL Parallel Gating

The figure below shows a parallel DCTL gate, which is really the previously considered "inverter" stage with three transistors having individual inputs instead of a single transistor. Obviously, this configuration is a NOR circuit. If any input is high on any of the three transistors, its collector will draw current through the load resistor, causing the output to go low.

Direct-Coupled Transistor Logic (DCTL)

DCTL Parallel Gating



Integrated Injection Logic (IIL, I^2L or I2L)

Integrated injection logic (IIL, I^2L, or I2L) is a class of digital circuits built with multiple collector bipolar junction transistors (BJT). When introduced it had speed comparable to TTL yet was almost as low power as CMOS, making it ideal for use in VLSI (and larger) integrated circuits.

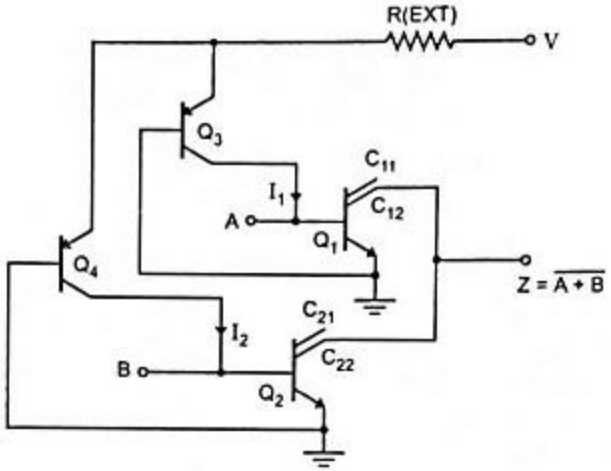


Fig. 47.7 *IIL Logic NOR Gate*

Integrated Injection Logic (IIL, I^2L or I2L)

When supply voltage V is connected to emitters of Q_3 and Q_4, current is supplied to base of Q_1 and Q_2. The working of the Integrated Injection Logic (IIL or I^2L) gate is explained below.

Case I : Both A and B LOW : A low at A will bypass the injected current from Q_3 and make Q_1 off. The input source acts as a sink for the current I_1. Similarly Q_2 will be off because input B is also low. Voltage at Z will be high.

Case II : Either A or B HIGH or Both HIGH :

Current I_1 or I_2 or both are diverted to BE junctions of transistors Q_1 and Q_2 and they are turned on. The voltage at Z will be low being saturated voltage of 0.2 V. Thus a NOR output is obtained.

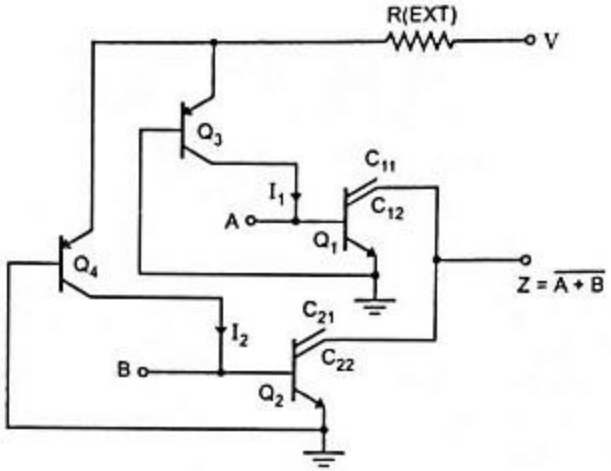


Fig. 47.7 *IIL Logic NOR Gate*

Schottky-Diode Non-Saturating Logic (Schottky-Clamped Logic for TTL)

Schottky Diodes in Logic Gates

The Schottky diode has many uses in digital circuits and are extensively used in Schottky transistor–transistor logic (TTL) digital logic gates and circuits due to their higher frequency response, decreased switching times and lower power consumption. Where high speed switching is required, Schottky based TTL is the obvious choice. There are different versions of Schottky TTL all with differing speeds and power consumption.

Schottky-Diode Non-Saturating Logic (Schottky-Clamped Logic for TTL)

- The three main TTL logic series which use the Schottky diode in its construction are given as:
- Schottky Diode Clamped TTL (S series) – Schottky "S" series TTL (74SXX) is an improved version of the original diode-transistor DTL, and transistor-transistor 74 series TTL logic gates and circuits. Schottky diodes are placed across the base-collector junction of the switching transistors to prevent them from saturating and creating propagation delays allowing for faster operation.

Schottky-Diode Non-Saturating Logic (Schottky-Clamped Logic for TTL)

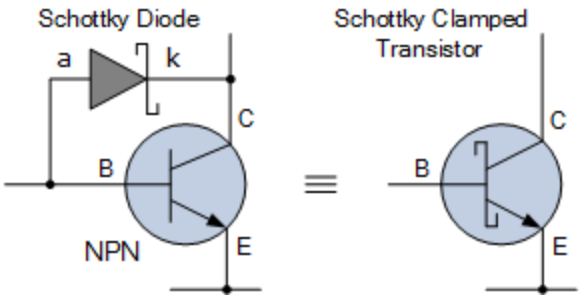
- Low-Power Schottky (LS series) – The transistor switching speed, stability and power dissipation of the 74LSXX series TTL is better than the previous 74SXX series. As well as a higher switching speed, the low-power Schottky TTL family consumes less power making the 74LSXX TTL series a good choice for many applications.

Schottky-Diode Non-Saturating Logic (Schottky-Clamped Logic for TTL)

- Advanced Low-Power Schottky (ALS series) – Additional improvements in the materials used to fabricate the ms-junctions of the diodes means that the 74LSXX series has reduced propagation delay time and much lower power dissipation compared to the 74ALSXX and the 74LS series. However, being a newer technology and inherently more complex design internally than standard TTL, the ALS series is slightly more expensive.

Schottky-Diode Non-Saturating Logic (Schottky-Clamped Logic for TTL)

As shown, a Schottky clamped transistor is basically a standard bipolar junction transistor with a Schottky diode connected in parallel across its base-collector junction.



When the transistor conducts normally in the active region of its characteristics curves, the base–collector junction is reverse biased and so the diode is reverse biased allowing the transistor to operate as a normal npn transistor.

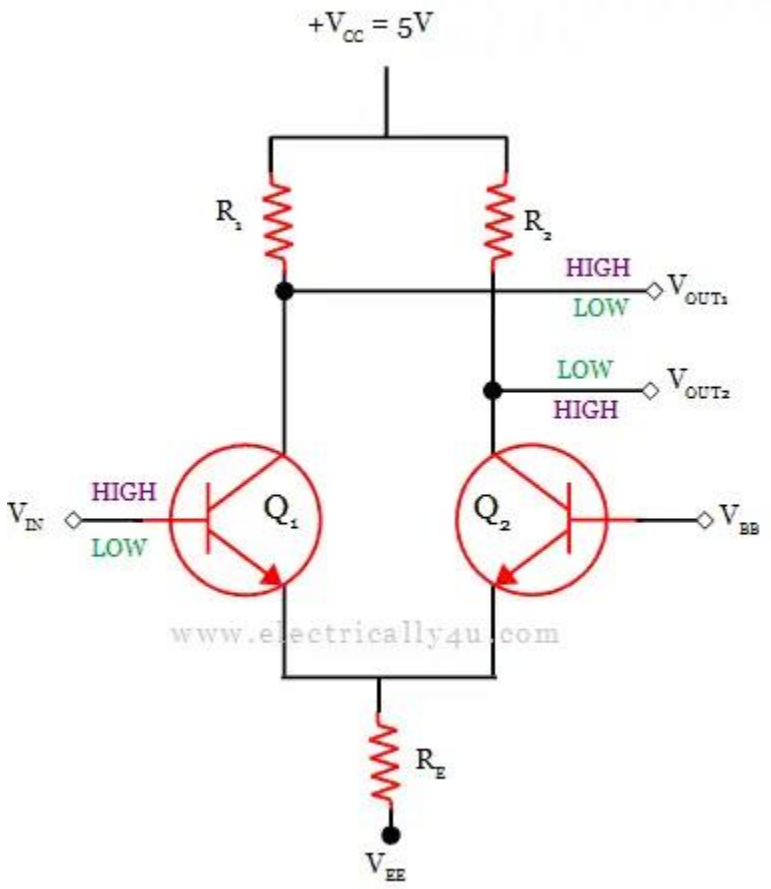
Emitter-Coupled Logic (ECL)

In electronics, **emitter-coupled logic** (**ECL**) is a high-speed integrated circuit bipolar transistor logic family. ECL uses an overdriven bipolar junction transistor (BJT) differential amplifier with single-ended input and limited emitter current to avoid the saturated (fully on) region of operation and its slow turn-off behaviour. As the current is steered between two legs of an emitter-coupled pair, ECL is sometimes called current-steering logic (CSL), current-mode logic (CML) or current-switch emitter-follower (CSEF) logic.

Emitter-Coupled Logic (ECL)

Inverter circuit of emitter-coupled logic

The circuit shown represents the emitter-coupled logic circuit of an inverter. It has two NPN transistors connected in differential single -ended input mode. Both the emitters are connected together with common resistance R_E. It is a current limiting resistance, used to prevent the transistor from entering into saturation.

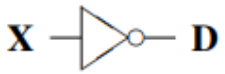


MOSFET Logic

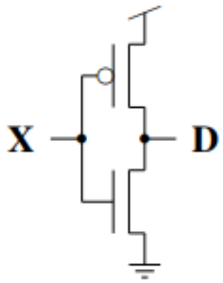
Inverter

X	D
0	1
1	0

(a)



(b)



(c)

$D = \overline{X}$

(d)

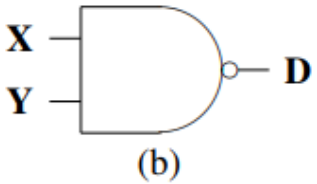
Inverter. (a) Truth table. (b) Symbol. (c) Schematic. (d) Boolean expression

MOSFET Logic

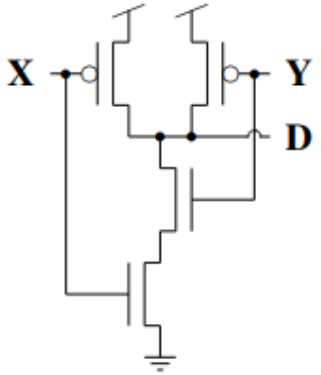
NAND gates

Y	X	D
0	0	1
0	1	1
1	0	1
1	1	0

(a)



(b)



(c)

$$D = \overline{X \cdot Y}$$

(d)

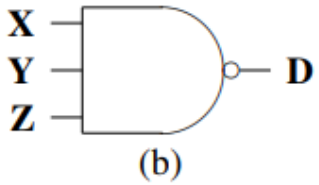
Two input NAND. (a) Truth table. (b) Symbol. (c) Schematic. (d) Boolean expression

MOSFET Logic

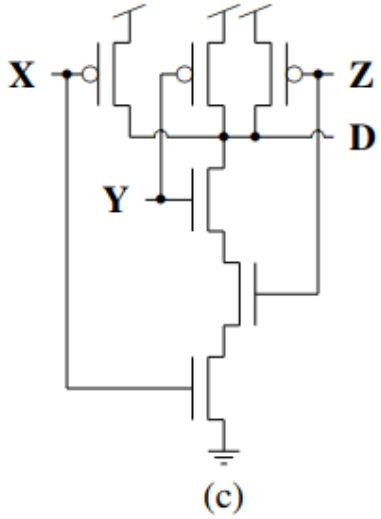
NAND gates

Z	Y	X	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a)



(b)



(c)

$$D = \overline{X \cdot Y \cdot Z}$$

(d)

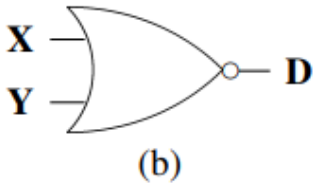
Three input NAND. (a) Truth table. (b) Symbol. (c) Schematic. (d) Boolean expression

MOSFET Logic

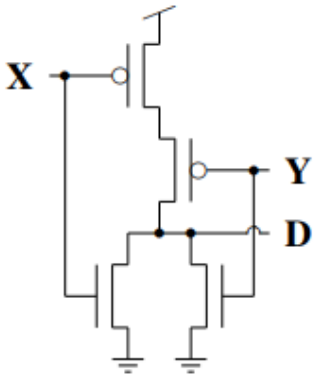
NOR gates

Y	X	D
0	0	1
0	1	0
1	0	0
1	1	0

(a)



(b)



(c)

$$D = \overline{X + Y}$$

(d)

Two input NOR. (a) Truth table. (b) Symbol. (c) Schematic. (d) Boolean expression

LOGIC Family

DIGITAL INTEGRATED CIRCUITS

Digital Integrated circuits are produced using several different circuit configurations and production technologies. Each such approach is called a specific logic family. A logic family is a collection of different integrated circuit chips that have similar input, output, and internal circuit characteristics, but they perform different logic gate functions such as AND, OR, NOT, etc. The idea is that different logic gate functions, when fabricated in the form of an integrated circuit with the same approach, or which belongs to the same logic family, will have identical electrical characteristics (electrically compatible with each other). These families may vary by speed, power consumption, cost, voltage and current levels.

LOGIC Family

The characteristics which are bound to be identical and used to compare performance are:

- Supply voltage range
- Speed of response
- Dissipation of power
- Input and output logic levels
- Current sinking capability
- Current sourcing capability
- Flexibility
- Noise immunity
- Fan-out

LOGIC Family