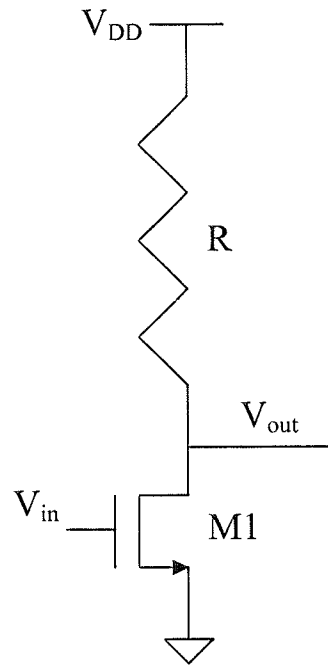


Question 1:



In the figure above, transistor M1 has the following parameters: $k_N = \frac{\mu_N \epsilon_{ox}}{t_{ox}} = 4\text{mA/V}^2$,

$V_{tn} = 1\text{V}$ and $V_{DD} = 5\text{V}$. V_{tn} represents the transistor threshold voltage, t_{ox} is the gate oxide thickness of SiO_2 , ϵ_{ox} is the permittivity of SiO_2 , and μ_n is the mobility of electrons.

(a) If W/L is the width-to-length ratio of M1 and R is the resistance of the resistive

load, then find the ratio $\frac{1/R}{W/L}$ so that V_{oL} of the inverter is equal to 1V. Please

clearly state all assumptions. (V_{oL} represents the output low voltage of the inverter.) (30 points)

(b) What is V_{oH} of the inverter? Please explain your results. (Note: V_{oH} is the output high voltage for the inverter) (10 points)

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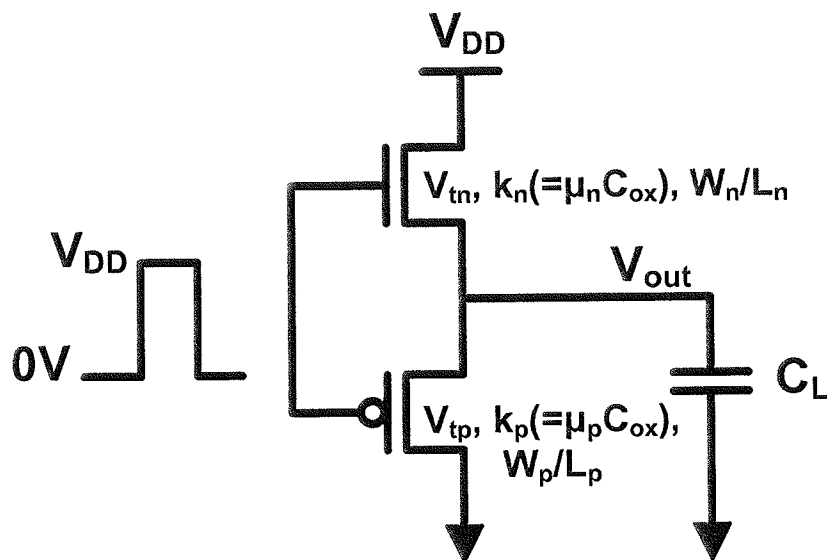
Question 2:

Consider an inverter of minimum size (input capacitance of C_i) driving a load C_l , which is x times as large as C_i ($C_l = x.C_i$). The size of the PMOS transistor is a times larger than the NMOS transistor. You decide to introduce another inverter (u times larger than the first) between the minimum sized inverter and the load C_l . What should u be to minimize the delay? When does it make sense to introduce this inverter? Clearly state all assumptions. (30 points)

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Question 3:

Consider the following circuit driving a load capacitance of C_L . The transistors have a threshold voltage of $|V_t| = |V_{tn}| = |V_{tp}|$. If there is a low to high input transition as shown in the figure, determine the energy dissipation. Assume that $V_{out} = 0$ to start with. (30 points)



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