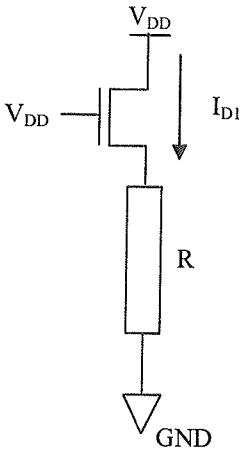
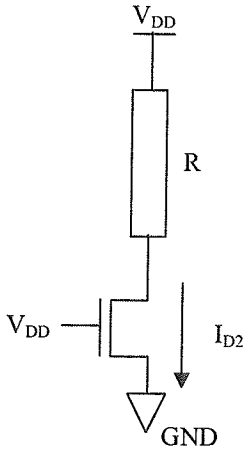
Question 1 (50 points total). Consider the following two circuit configurations. Both circuits are in fact identical except that the V_{DD} and GND terminals are swapped. R is a non-zero resistive load. Assume long channel devices and ignore channel length modulation.

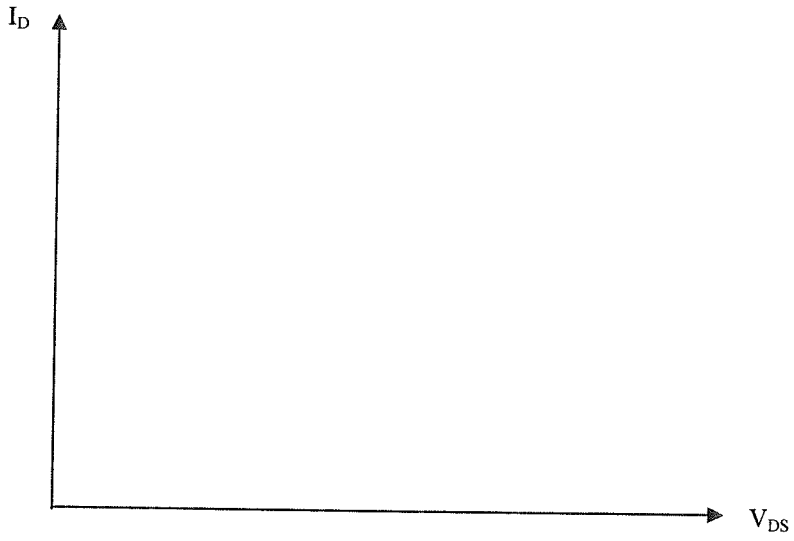


Circuit A



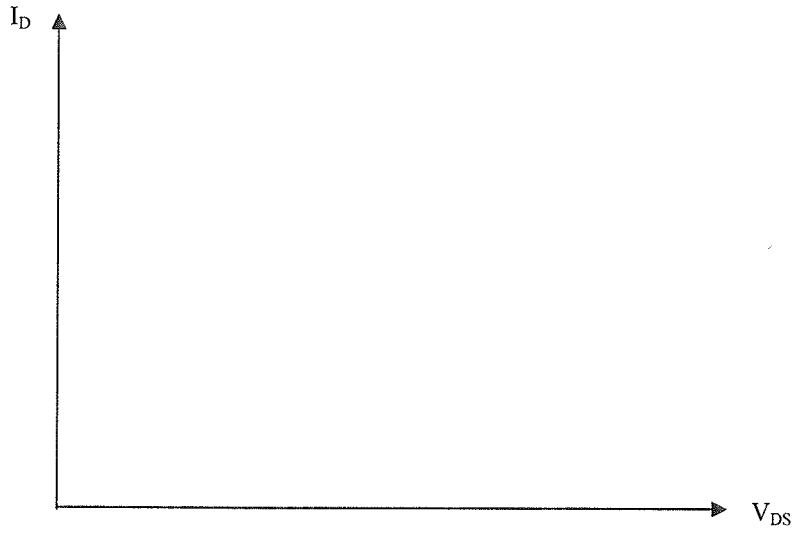
Circuit B

(a) (15 points) Sketch, not necessary to scale, the IV-curve for the transistor in circuit A. The x-axis is V_{DS}, and the y-axis is current I_D. Show also the IV-curve of the resistor in the plot to determine I_{D1}.



Write in Exam Book Only

(b) (15 points) Sketch, not necessary to scale, the IV-curve for the transistor in circuit B. The x-axis is V_{DS} and the y-axis is current I_D. Show also the IV-curve of the resistor in the plot to determine I_{D2}.



(c) (20 points) Which current, I_{D1} or I_{D2}, is larger? Justify your answer.

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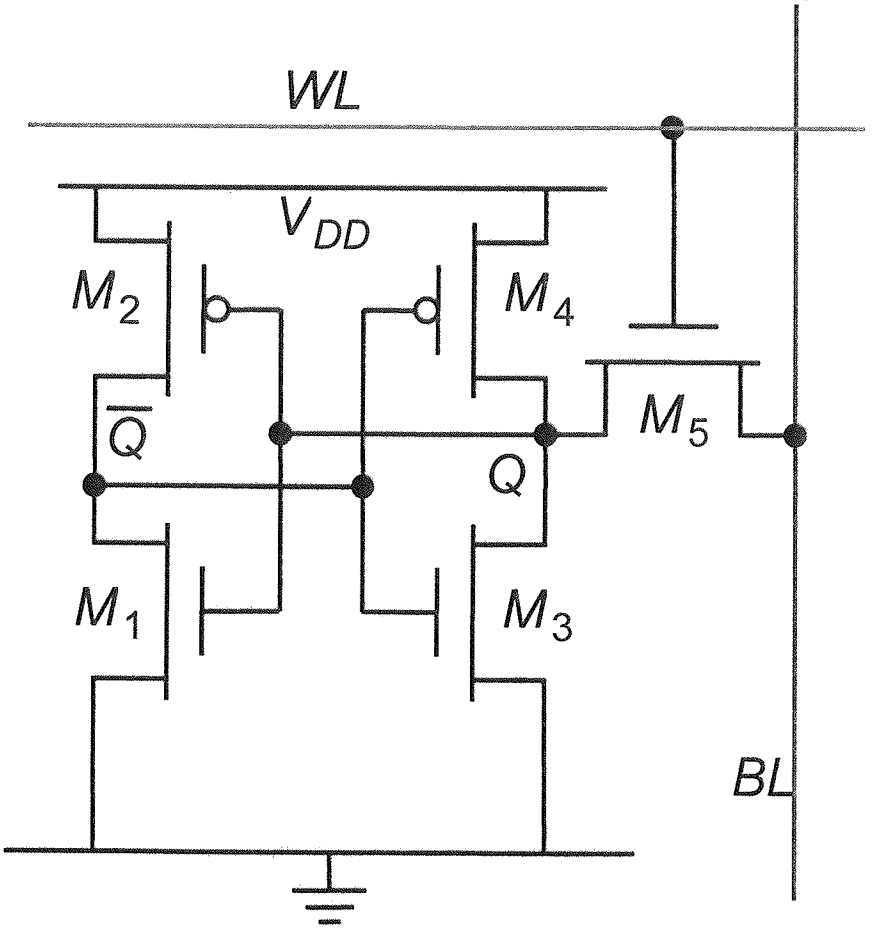
Question 2. (50 points) Consider the following 5-Transistor SRAM cell design. Answer the following questions based on your understanding of ratioed logic. Use V_T as the threshold voltage (for NMOS and PMOS) and V_M as the switching threshold of inverters.



(a) (15 points) Suppose V_Q is currently V_{DD}. Now, BL is pulled down to ground and WL is enabled. Discuss *qualitatively* the required sizing of the transistors to write 0 into Q (or making $V_Q = 0V$) . (You should identify the transistors forming the ratioed logic and state how the appropriate sizing of the ratioed logic could be determined, e.g., "transistors M1 and M5 form a ratioed logic and should be sized such that V_Q is less than $V_{T,M3}$ when V_{WL} is high." Do not attempt to solve equations.)

(b) (15 points) Suppose V_Q is currently 0V. Now, BL is pulled up to V_{DD} and WL is enabled. Discuss *qualitatively* the required sizing of transistors to write 1 into Q (or making $V_Q = V_{DD}$).

(c) (20 points) Assume that you have performed the appropriate sizing of transistors so that 0 and 1 can be written into Q correctly. Suppose WL is disabled and the voltage at node Q is either V_{DD} or 0V. Suppose BL is now pre-charged to V_{DD} before we enable WL to perform a read operation. Is it possible to perform a read safely? In other words, can the transistors $M_{1..5}$ work together to successfully pull BL to the voltage V_Q? Justify your answer. If your answer is negative, propose a solution to overcome the problem without adding transistors.