

# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

## PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
$C_n$	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
$\bar{P}$ ('LS381A 'S381 ONLY)	14	ACTIVE-LOW CARRY PROPAGATE OUTPUT
$\bar{G}$ ('LS381A 'S381 ONLY)	13	ACTIVE-LOW CARRY GENERATE OUTPUT
$C_n + 4$ ('LS382A ONLY)	14	RIPPLE-CARRY OUTPUT
OVR ('LS382A ONLY)	13	OVERFLOW OUTPUT
V <sub>CC</sub>	20	SUPPLY VOLTAGE
GND	10	GROUND

- Fully Parallel 4-Bit ALUs in 20-Pin Package for 0.300-Inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- 'LS381A and 'S381 Feature  $\bar{G}$  and  $\bar{P}$  Outputs for Look-Ahead Carry Cascading
- 'LS382A Features Ripple Carry ( $C_n + 4$ ) and Overflow (OVR) Outputs
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
  - A Minus B
  - B Minus A
  - A Plus B
  - and Five Other Functions

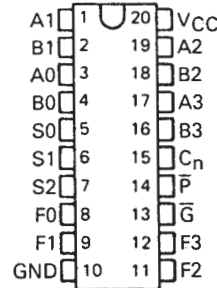
## description

The 'LS381A, 'S381 and 'LS382A are low-power Schottky and Schottky TTL arithmetic logic units (ALUs)/function generators that perform eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, or OR function of the two Boolean variables is provided without the use of external circuitry. Also, the outputs can be cleared (low) or preset (high) as desired. The 'LS381A and 'S381 provide two cascade outputs ( $\bar{P}$  and  $\bar{G}$ ) for expansion utilizing SN54S182/SN74S182 look-ahead carry generators. The 'LS382 provides a  $C_n + 4$  output to ripple the carry to the  $C_n$  input of the next stage. The 'LS382A detects and indicates two's complement overflow condition via the OVR output. The overflow output is logically equivalent to  $C_n + 3 \oplus C_n + 4$ . When the 'LS382A is cascaded to handle word lengths longer than four bits in length, only the most significant overflow (OVR) output is used.

The SN54' family is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74' family is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

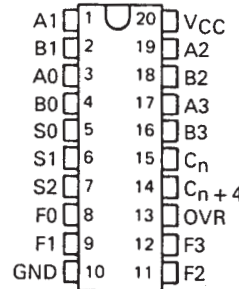
SN54LS381A, SN54S381  
... J OR W PACKAGE  
SN74LS381A, SN74S381  
... DW OR N PACKAGE

(TOP VIEW)



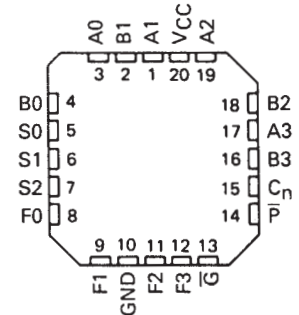
SN54LS382A ...  
J OR W PACKAGE  
SN74LS382A ...  
DW OR N PACKAGE

(TOP VIEW)



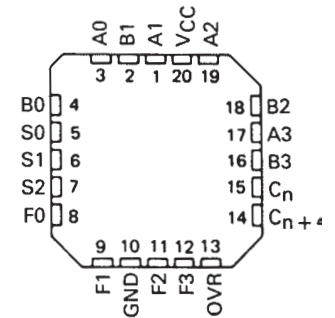
SN54LS381A, SN54S381  
... FK PACKAGE

(TOP VIEW)



SN54LS382A ... FK PACKAGE

(TOP VIEW)



## FUNCTION TABLE

SELECTION	ARITHMETIC/LOGIC		
S2 S1 S0	OPERATION		
L L L	CLEAR		
L L H	B MINUS A		
L H L	A MINUS B		
L H H	A PLUS B		
H L L	$A \oplus B$		
H L H	$A + B$		
H H L	AB		
H H H	PRESET		

H = high level, L = low level

# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

## function table

Certain differences exist in the  $\overline{G}$ ,  $\overline{P}$  ('LS381A, 'S381) and OVR,  $C_{n+4}$  ('LS382A) function table compared with similar parts from other technologies and other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B), where these outputs perform valuable cascade functions. There are slight differences in the other modes (CLEAR,  $A + B$ ,  $A \oplus B$ , AB, and PRESET), where these outputs are strictly "don't care".

This function table is a condensed version and assumes for  $A_n$  that A0, A1, A2, and A3 inputs all agree and for  $B_n$  that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these  $\overline{G}$ ,  $\overline{P}$  ('LS381A, 'S381) and OVR,  $C_{n+4}$  ('LS382A) outputs in all modes of operation to facilitate incoming inspection.

FUNCTION TABLE

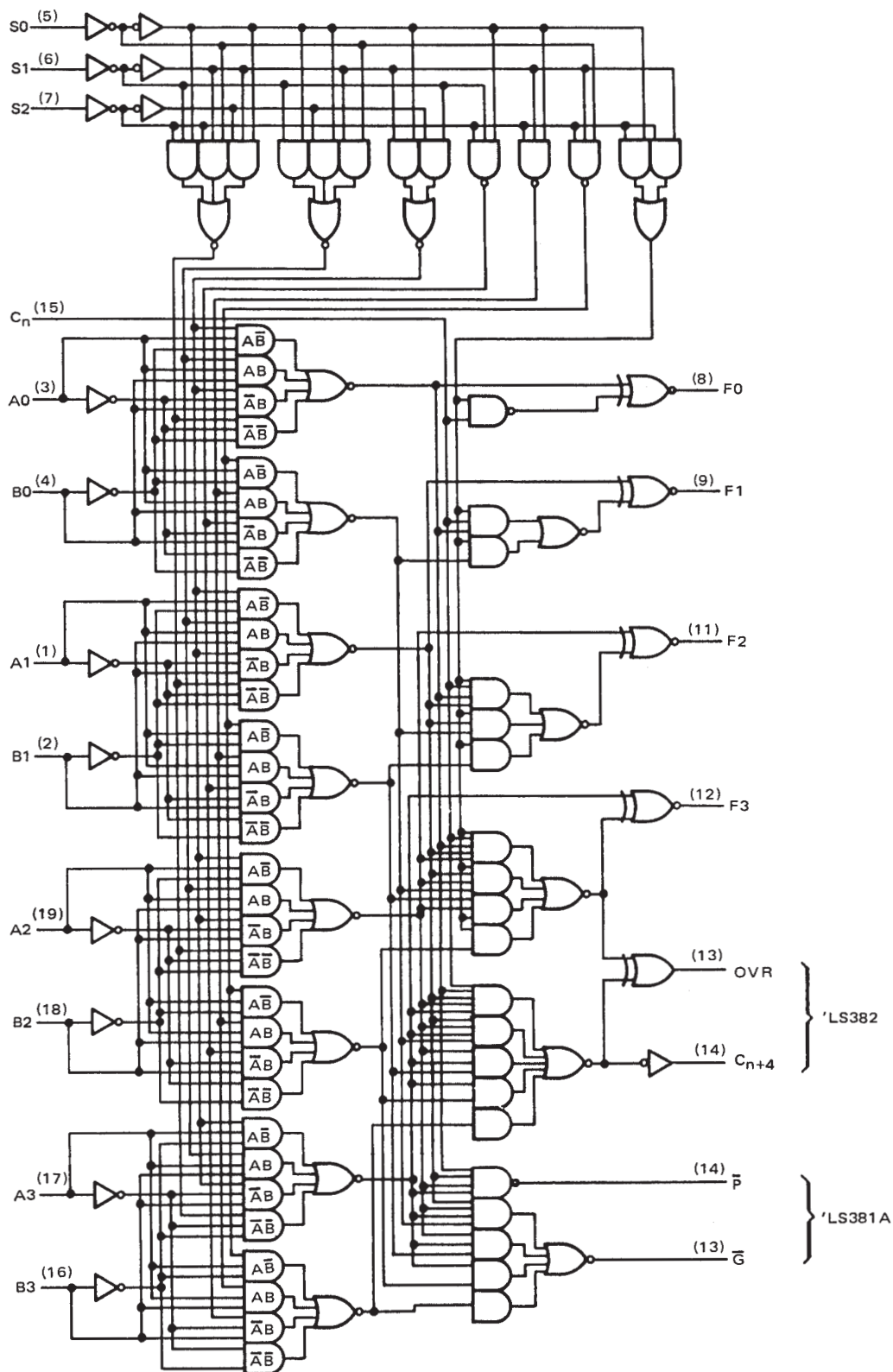
ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				('LS381A, 'S381)		('LS382A)	
	S2	S1	S0	$C_n$	$A_n$	$B_n$	F3	F2	F1	F0	$\overline{G}$	$\overline{P}$	OVR	$C_{n+4}$
CLEAR	L	L	L	X	X	X	L	L	L	L	H	H	L	L
B MINUS A	L	L	H	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	H	H	H	L	L	H	L	H
				L	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	H	H	H	H	L	H	L	H
				H	H	L	L	L	L	H	H	H	L	L
				H	H	H	L	L	L	L	H	L	L	H
A MINUS B	L	H	L	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	L	L	L	L	H	H	L	L
				L	H	L	H	H	H	L	L	H	L	H
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	L	L	L	H	H	H	L	L
				H	H	L	H	H	H	H	L	H	L	H
				H	H	H	L	L	L	L	H	L	L	H
A PLUS B	L	H	H	L	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				L	H	L	H	H	H	H	H	L	L	L
				L	H	H	H	H	H	L	L	H	L	H
				H	L	L	L	L	L	H	H	H	L	L
				H	L	H	L	L	L	L	H	L	L	H
				H	H	L	L	L	L	L	H	L	L	H
				H	H	H	H	H	H	H	L	H	L	H
$A \oplus B$	H	L	L	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
A + B	H	L	H	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				L	H	L	H	H	H	H	H	L	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	L	L
AB	H	H	L	X	L	L	L	L	L	L	H	H	L	L
				X	L	H	L	L	L	L	H	H	L	L
				L	H	L	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
PRESET	H	H	H	L	X	X	H	H	H	H	H	L	L	L
				H	X	X	H	H	H	H	H	L	H	H

# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

logic diagram (positive logic)

'LS381A, 'LS382A



Pin numbers shown are for DW, J, N, and W packages.

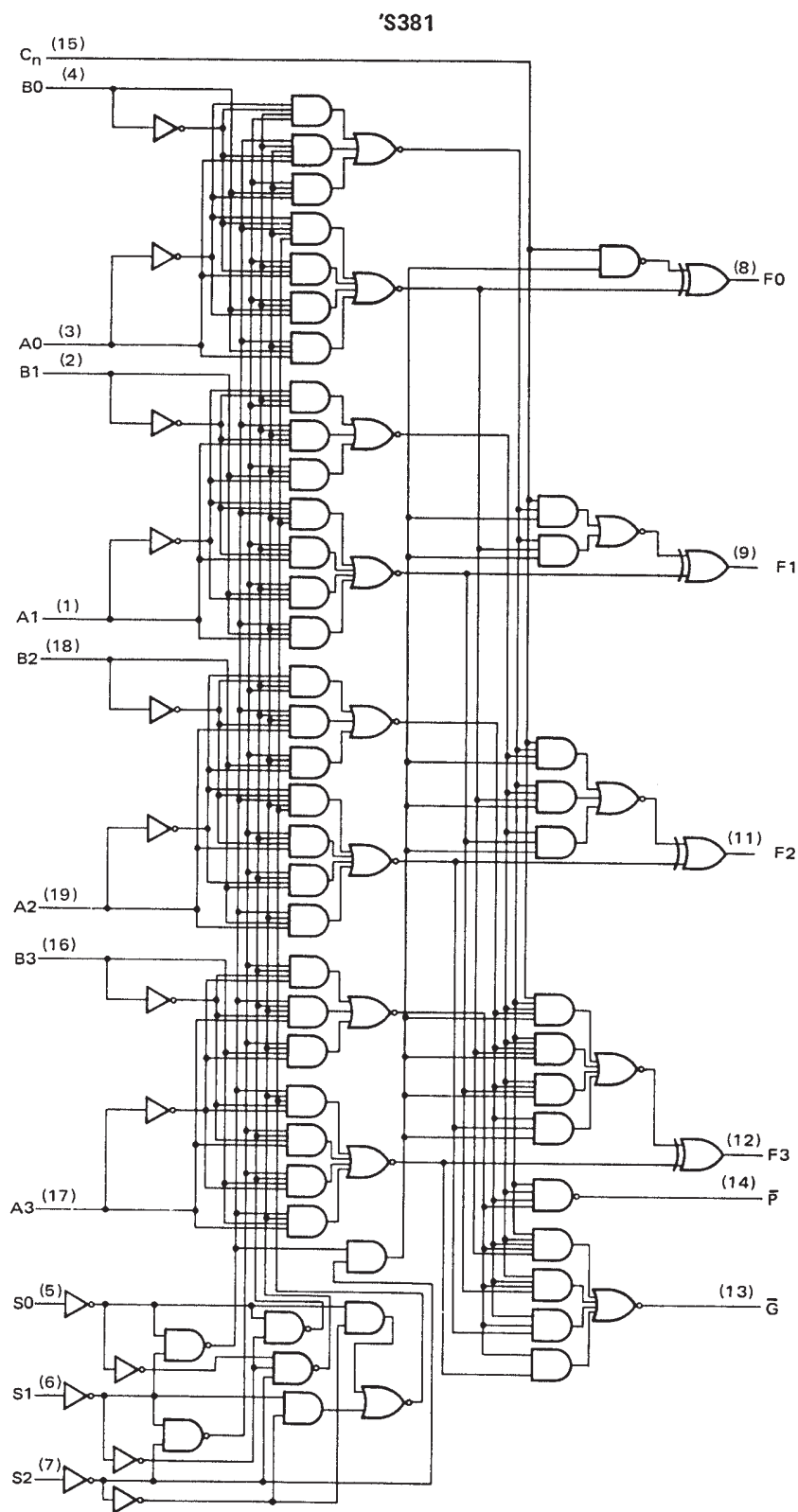


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

## logic diagram and schematics of inputs and outputs



Pin numbers shown are for DW, J, N, and W packages.

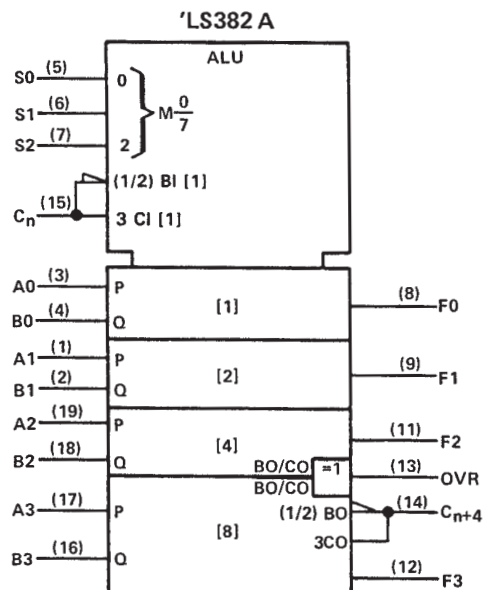
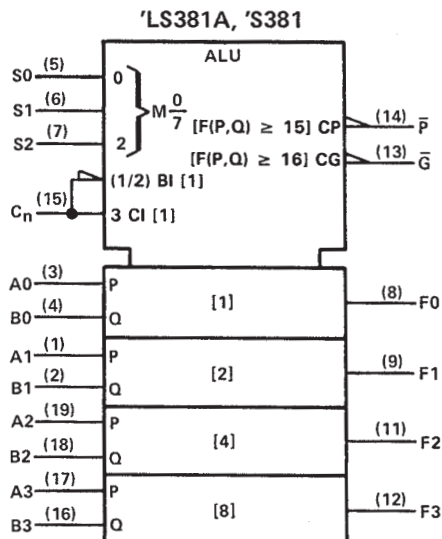


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

## logic symbols†

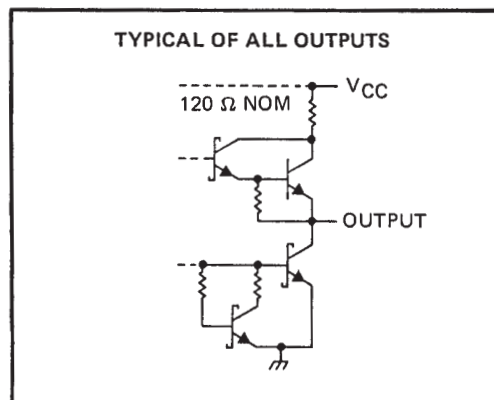
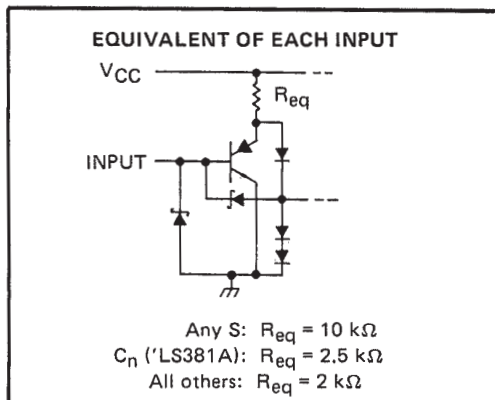


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

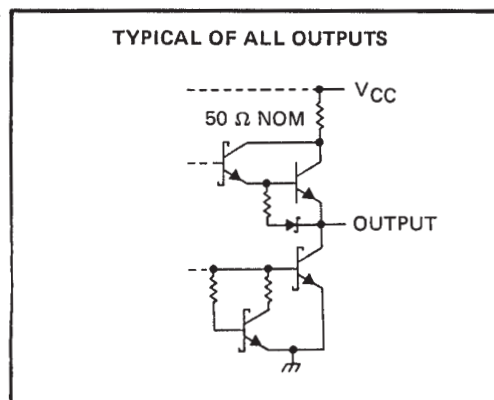
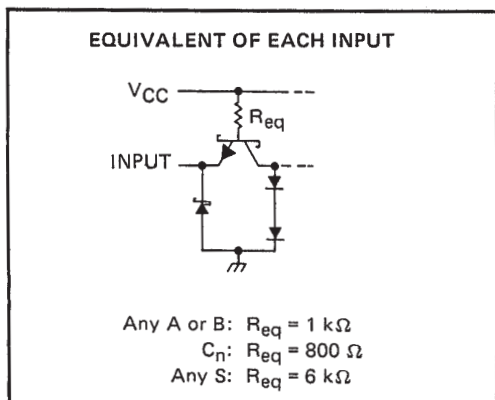
Pin numbers shown are for DW, J, N, and W packages.

## schematics of inputs and outputs

**'LS381, 'LS382A**



**'S381**





# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (See Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS381A, SN54LS382A	–55°C to 125°C
SN74LS381A, SN74LS382A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

## recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V
I <sub>OH</sub>	High-level output current		− 0.4			− 0.4			mA
I <sub>OL</sub>	Low-level output current	$\overline{G}$ output of 'LS381A	16			16			mA
		All other outputs	4			8			
T <sub>A</sub>	Operating free-air temperature		− 55      125			0      70			°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'		SN74LS'		UNIT
				MIN	TYP‡	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = – 18 mA		– 1.5		– 1.5		V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = – 0.4 mA		2.5	3.4	2.7	3.4	V
V <sub>OL</sub>	G̅ ('LS381A)	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 16 mA	0.47	0.7	0.47	0.7	V
	I <sub>OL</sub> = 4 mA		0.25	0.4	0.25	0.4		
	Other outputs		I <sub>OL</sub> = 8 mA			0.35	0.5	
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1		0.1		mA
I <sub>IH</sub>	Any S	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20		20		μA
	Any A or B			100		100		
	C <sub>n</sub> ('LS381A)			80		80		
	C <sub>n</sub> ('LS382A)			100		100		
I <sub>IL</sub>	Any S	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		– 0.2		– 0.2		mA
	Any A or B			– 1		– 1		
	C <sub>n</sub> ('LS381A)			– 0.8		– 0.8		
	C <sub>n</sub> ('LS382A)			– 0.8		– 0.8		
I <sub>OS</sub> §		V <sub>CC</sub> = MAX		– 20	– 100	– 20	– 100	mA
I <sub>CC</sub>		V <sub>CC</sub> = MAX, All inputs grounded, outputs open		35 65		35 65		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.



# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS381A			'LS382			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	C <sub>n</sub>	Any F	R <sub>L</sub> = 2 kΩ,      C <sub>L</sub> = 15 pF	18	27		18	27	ns	
t <sub>PHL</sub>				14	21		14	21		
t <sub>PLH</sub>	Any A or B	$\overline{G}$		20	30				ns	
t <sub>PHL</sub>				21	33					
t <sub>PLH</sub>	Any A or B	$\overline{P}$		21	33				ns	
t <sub>PHL</sub>				23	33					
t <sub>PLH</sub>	A <sub>i</sub> or B <sub>i</sub>	F <sub>i</sub>		20	30		20	30	ns	
t <sub>PHL</sub>				15	23		15	23		
t <sub>PLH</sub>	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	F <sub>i</sub>		35	53		35	53	ns	
t <sub>PHL</sub>				34	51		34	51		
t <sub>PLH</sub>	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	$\overline{G}$ or $\overline{P}$		31	47				ns	
t <sub>PHL</sub>				32	48					
t <sub>PLH</sub>	Any A or B	C <sub>n+4</sub>					28	42	ns	
t <sub>PHL</sub>							26	39		
t <sub>PLH</sub>	Any A or B	OVR					23	35	ns	
t <sub>PHL</sub>							27	41		
t <sub>PLH</sub>	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	C <sub>n+4</sub> or OVR					38	57	ns	
t <sub>PHL</sub>							36	54		
t <sub>PLH</sub>	C <sub>n</sub>	OVR					10	15	ns	
t <sub>PHL</sub>							13	23		
t <sub>PLH</sub>	C <sub>n</sub>	C <sub>n+4</sub>					13	21	ns	
t <sub>PHL</sub>							11	20		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN54LS381A, SN54S381, SN74LS381A, SN54LS382A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDLS168 – JANUARY 1981 – REVISED MARCH 1988

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S381	–55°C to 125°C
SN74S381	0°C to 70°C
Storage free-air temperature	–65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with its respective B input; for example A0 with B0, etc.

## recommended operating conditions

	SN54S381			SN74S381			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			–1			–1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage			2			V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				–1.2	V
$V_{OH}$	High-level output voltage	SN54S381 $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$		2.4	3.4		V
		SN74S381		2.7	3.4		
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
$I_{IH}$	High-level input current	Any S input				50	$\mu\text{A}$
		$C_n$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			250	
		All others				200	
$I_{IL}$	Low-level input current	Any S input				–2	mA
		$C_n$	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			–8	
		All others				–6	
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$		–40		–100	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$			105	160	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	C <sub>n</sub>	Any F	C <sub>L</sub> = 15 pF,    R <sub>L</sub> = 280 Ω, See Note 3		10	17	ns
tPHL					10	17	
tPLH	Any A or B	$\overline{G}$			12	20	ns
tPHL					12	20	
tPLH	Any A or B	$\overline{P}$			11	18	ns
tPHL					11	18	
tPLH	A <sub>i</sub> or B <sub>i</sub>	F <sub>i</sub>			18	27	ns
tPHL					16	25	
tPLH	Any S	Any			18	30	ns
tPHL					18	30	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.