CSCE2303 - Computer Organization and Assembly Language Programming

Memory Hierarchy Simulator

Names & IDs

Jana Elfeky, 900215017

Andrew Antoine, 900211633

Abdelrahman Ihab, 900213468

Program Description: The implemented caching system simulator is designed to mimic a one-level direct-mapped cache with support for both read and write operations. It simulates two write policies: write-through and write-back. The simulator reads memory access sequences from an input file, processes each access, updates the cache state accordingly, and outputs detailed statistics on cache performance. Its features are:

1. Direct Mapping: Each memory address maps to a specific cache line based on its index.
2. Write Policies:

   Write-Through (WT): Updates both the cache and the main memory simultaneously on a write hit or miss.

   Write-Back (WB): Updates only the cache on a write hit and marks the cache line as dirty. The main memory is updated only when the dirty line is evicted.
3. Statistics Collection: Tracks and reports total accesses, reads, writes, hits, misses, hit ratio, miss ratio, and average memory access time (AMAT).
4. Configurable Parameters: Allows user-defined cache size, line size, cache access cycles, and write policies for cache hits and misses.

Design Decisions and Assumptions:

1. Fixed Memory Access Time: Assumes a fixed memory access time of 150 cycles for calculating AMAT.
2. File Handling: Reads memory access sequences from a file named access_sequence.txt located in the same directory as the executable.
3. Input Validation: Minimal validation of user inputs. The program expects correctly formatted inputs for cache parameters and policies.
4. Cache Initialization: Initializes cache lines as invalid with default tag and dirty flag values.

Bugs/Issues: There weren't any major bugs/issues encountered while working on the simulator.

User Guide:

Input Parameters

The program will prompt you to enter the following parameters:

1. Cache Size (bytes): Total size of the cache in bytes.
2. Line Size (bytes): Size of each cache line in bytes.
3. Cache Access Cycles: Number of cycles for accessing the cache.
4. Hit Write Policy (WT/WB): Write policy on cache hits (WT for Write-Through, WB for Write-Back).
5. Miss Write Policy (WT/WB): Write policy on cache misses (WT for Write-Through, WB for Write-Back).

Full Simulation Example

Example Access Sequence File: “access_sequence.txt”

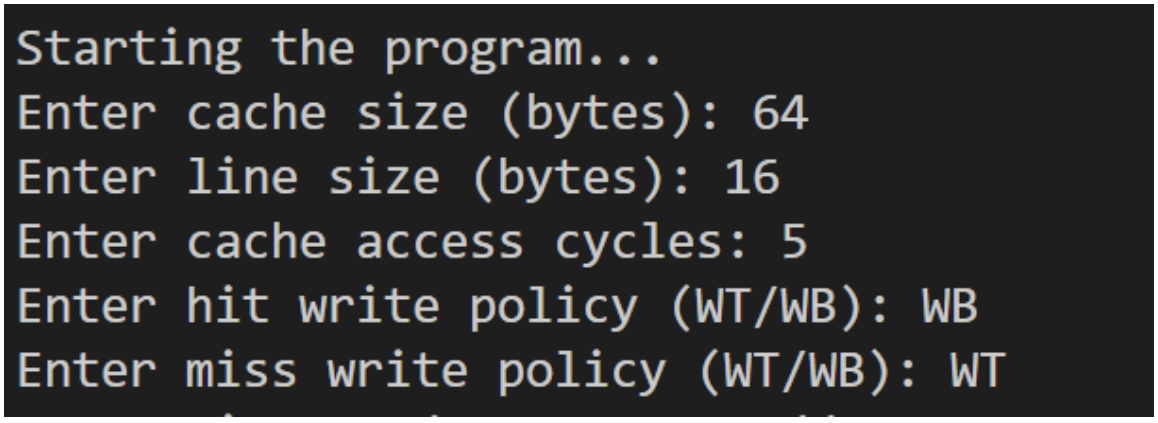
The file should contain a single line with comma-separated entries in the format address:accessType, where accessType is either R for read or W for write.

Example content:

16:R,32:W,48:R,64:W,16:R,80:W,32:R

Example Execution:

1. Provide Input:



2. Simulation Output:

```
Processing read access at address: 16
Cache State:
Line 0: Valid = 0, Tag = 0, Flag = 0
Line 1: Valid = 1, Tag = 1, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 1
Reads: 1, Writes: 0
Hits: 0, Misses: 1
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 32
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 0, Tag = 0, Flag = 0
Line 1: Valid = 1, Tag = 1, Flag = 0
Line 2: Valid = 1, Tag = 2, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 2
Reads: 1, Writes: 1
Hits: 0, Misses: 2
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 48
Cache State:
Line 0: Valid = 0, Tag = 0, Flag = 0
Line 1: Valid = 1, Tag = 1, Flag = 0
Line 2: Valid = 1, Tag = 2, Flag = 0
Line 3: Valid = 1, Tag = 3, Flag = 0
Total Accesses: 3
Reads: 2, Writes: 1
Hits: 0, Misses: 3
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 64
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 1, Tag = 1, Flag = 0
Line 2: Valid = 1, Tag = 2, Flag = 0
Line 3: Valid = 1, Tag = 3, Flag = 0
Total Accesses: 4
Reads: 2, Writes: 2
Hits: 0, Misses: 4
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 16
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 1, Tag = 1, Flag = 0
Line 2: Valid = 1, Tag = 2, Flag = 0
Line 3: Valid = 1, Tag = 3, Flag = 0
Total Accesses: 5
Reads: 3, Writes: 2
Hits: 1, Misses: 4
Hit Ratio: 0.2, Miss Ratio: 0.8
Average Memory Access Time: 125 cycles

Processing write access at address: 80
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 1, Tag = 5, Flag = 0
Line 2: Valid = 1, Tag = 2, Flag = 0
Line 3: Valid = 1, Tag = 3, Flag = 0
Total Accesses: 6
Reads: 3, Writes: 3
Hits: 1, Misses: 5
Hit Ratio: 0.166667, Miss Ratio: 0.833333
Average Memory Access Time: 130 cycles
```

```
Processing read access at address: 32
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 1, Tag = 5, Flag = 0
Line 2: Valid = 1, Tag = 2, Flag = 0
Line 3: Valid = 1, Tag = 3, Flag = 0
Total Accesses: 7
Reads: 4, Writes: 3
Hits: 2, Misses: 5
Hit Ratio: 0.285714, Miss Ratio: 0.714286
Average Memory Access Time: 112.143 cycles

Program completed successfully.
```

List of Sequences Used to Test:

Sequence 1:
1024:R,2048:W,1024:R,3000:W,2048:R,1088:W,2048:R,2112:W,3000:R,3072:W,3000:R,3072:W,2048:R,1024:W,1088:R,4096:W,2048:R,2112:W,4096:R,1024:W

Sequence 1 Output:

```
Starting the program...
Enter cache size (bytes): 64
Enter line size (bytes): 16
Enter cache access cycles: 5
Enter hit write policy (WT/WB): WB
Enter miss write policy (WT/WB): WT
Processing read access at address: 1024
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 1
Reads: 1, Writes: 0
Hits: 0, Misses: 1
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 2048
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 2
Reads: 1, Writes: 1
Hits: 0, Misses: 2
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 1024
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 3
Reads: 2, Writes: 1
Hits: 0, Misses: 3
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing write access at address: 3000
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 4
Reads: 2, Writes: 2
Hits: 0, Misses: 4
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 2048
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 5
Reads: 3, Writes: 2
Hits: 0, Misses: 5
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 1088
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 68, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 6
Reads: 3, Writes: 3
Hits: 0, Misses: 6
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 2048
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 7
Reads: 4, Writes: 3
Hits: 0, Misses: 7
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 2112
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 132, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 8
Reads: 4, Writes: 4
Hits: 0, Misses: 8
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 3000
Cache State:
Line 0: Valid = 1, Tag = 132, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 9
Reads: 5, Writes: 4
Hits: 1, Misses: 8
Hit Ratio: 0.111111, Miss Ratio: 0.888889
Average Memory Access Time: 138.333 cycles
```

```
Processing write access at address: 3072
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 192, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 10
Reads: 5, Writes: 5
Hits: 1, Misses: 9
Hit Ratio: 0.1, Miss Ratio: 0.9
Average Memory Access Time: 140 cycles

Processing read access at address: 3000
Cache State:
Line 0: Valid = 1, Tag = 192, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 11
Reads: 6, Writes: 5
Hits: 2, Misses: 9
Hit Ratio: 0.181818, Miss Ratio: 0.818182
Average Memory Access Time: 127.727 cycles

Processing write access at address: 3072
Cache State:
Line 0: Valid = 1, Tag = 192, Flag = 1
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 12
Reads: 6, Writes: 6
Hits: 3, Misses: 9
Hit Ratio: 0.25, Miss Ratio: 0.75
Average Memory Access Time: 117.5 cycles
```

```
Processing read access at address: 2048
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 13
Reads: 7, Writes: 6
Hits: 3, Misses: 10
Hit Ratio: 0.230769, Miss Ratio: 0.769231
Average Memory Access Time: 120.385 cycles

Processing write access at address: 1024
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 14
Reads: 7, Writes: 7
Hits: 3, Misses: 11
Hit Ratio: 0.214286, Miss Ratio: 0.785714
Average Memory Access Time: 122.857 cycles

Processing read access at address: 1088
Cache State:
Line 0: Valid = 1, Tag = 68, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 15
Reads: 8, Writes: 7
Hits: 3, Misses: 12
Hit Ratio: 0.2, Miss Ratio: 0.8
Average Memory Access Time: 125 cycles
```

```
Processing write access at address: 4096
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 256, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 16
Reads: 8, Writes: 8
Hits: 3, Misses: 13
Hit Ratio: 0.1875, Miss Ratio: 0.8125
Average Memory Access Time: 126.875 cycles

Processing read access at address: 2048
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 17
Reads: 9, Writes: 8
Hits: 3, Misses: 14
Hit Ratio: 0.176471, Miss Ratio: 0.823529
Average Memory Access Time: 128.529 cycles

Processing write access at address: 2112
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 132, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 18
Reads: 9, Writes: 9
Hits: 3, Misses: 15
Hit Ratio: 0.166667, Miss Ratio: 0.833333
Average Memory Access Time: 130 cycles
```

```
Processing read access at address: 4096
Cache State:
Line 0: Valid = 1, Tag = 256, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 19
Reads: 10, Writes: 9
Hits: 3, Misses: 16
Hit Ratio: 0.157895, Miss Ratio: 0.842105
Average Memory Access Time: 131.316 cycles

Processing write access at address: 1024
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 1, Tag = 187, Flag = 0
Total Accesses: 20
Reads: 10, Writes: 10
Hits: 3, Misses: 17
Hit Ratio: 0.15, Miss Ratio: 0.85
Average Memory Access Time: 132.5 cycles

Program completed successfully.
```

Sequence 2:
64:R,128:W,256:R,512:W,64:R,128:R,512:W,1024:W,64:W,128:R,512:W,1024:W,2048:R,256:R,
128:W,64:R,256:W,512:R,1024:R,2048:W

Sequence 2 Output:

```
Starting the program...
Enter cache size (bytes): 64
Enter line size (bytes): 16
Enter cache access cycles: 5
Enter hit write policy (WT/WB): WB
Enter miss write policy (WT/WB): WT
Processing read access at address: 64
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 1
Reads: 1, Writes: 0
Hits: 0, Misses: 1
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 128
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 8, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 2
Reads: 1, Writes: 1
Hits: 0, Misses: 2
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 256
Cache State:
Line 0: Valid = 1, Tag = 16, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 3
Reads: 2, Writes: 1
Hits: 0, Misses: 3
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing write access at address: 512
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 32, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 4
Reads: 2, Writes: 2
Hits: 0, Misses: 4
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 64
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 5
Reads: 3, Writes: 2
Hits: 0, Misses: 5
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 128
Cache State:
Line 0: Valid = 1, Tag = 8, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 6
Reads: 4, Writes: 2
Hits: 0, Misses: 6
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing write access at address: 512
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 32, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 7
Reads: 4, Writes: 3
Hits: 0, Misses: 7
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 1024
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 8
Reads: 4, Writes: 4
Hits: 0, Misses: 8
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 64
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 9
Reads: 4, Writes: 5
Hits: 0, Misses: 9
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 128
Cache State:
Line 0: Valid = 1, Tag = 8, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 10
Reads: 5, Writes: 5
Hits: 0, Misses: 10
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 512
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 32, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 11
Reads: 5, Writes: 6
Hits: 0, Misses: 11
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 1024
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 12
Reads: 5, Writes: 7
Hits: 0, Misses: 12
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 2048
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 13
Reads: 6, Writes: 7
Hits: 0, Misses: 13
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 256
Cache State:
Line 0: Valid = 1, Tag = 16, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 14
Reads: 7, Writes: 7
Hits: 0, Misses: 14
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 128
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 8, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 15
Reads: 7, Writes: 8
Hits: 0, Misses: 15
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 64
Cache State:
Line 0: Valid = 1, Tag = 4, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 16
Reads: 8, Writes: 8
Hits: 0, Misses: 16
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 256
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 16, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 17
Reads: 8, Writes: 9
Hits: 0, Misses: 17
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing read access at address: 512
Cache State:
Line 0: Valid = 1, Tag = 32, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 18
Reads: 9, Writes: 9
Hits: 0, Misses: 18
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles
```

```
Processing read access at address: 1024
Cache State:
Line 0: Valid = 1, Tag = 64, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 19
Reads: 10, Writes: 9
Hits: 0, Misses: 19
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Processing write access at address: 2048
Write-through on miss: Writing to memory.
Cache State:
Line 0: Valid = 1, Tag = 128, Flag = 0
Line 1: Valid = 0, Tag = 0, Flag = 0
Line 2: Valid = 0, Tag = 0, Flag = 0
Line 3: Valid = 0, Tag = 0, Flag = 0
Total Accesses: 20
Reads: 10, Writes: 10
Hits: 0, Misses: 20
Hit Ratio: 0, Miss Ratio: 1
Average Memory Access Time: 155 cycles

Program completed successfully.
```

Our Experience: Building the caching system simulator was a rewarding learning experience. While the complexity wasn't overwhelming, it demanded meticulous attention to detail to ensure accurate and functional results. Collaboration on the implementation proved fruitful, allowing for efficient task division and using each other's expertise. This project provided an important bridge between theoretical concepts and practical application. It solidified our understanding of memory hierarchy principles, including cache mechanisms and direct mapping, while also introducing us to write policies. Through this hands-on experience, we gained a deeper appreciation for translating theoretical knowledge into a tangible real-world scenario.