Birla Institute of Technology & Science, Pilani
Work Integrated Learning Programmes Division
First Semester 2023-2024
M.Tech (Data Science and Engineering)
Mid-Semester Exam (EC-2 Regular)

Course No.	: DSECLZG516
Course Title	: Computer Organization and Software Systems
Nature of Exam	: Open Book
Weightage	: 30%
Duration	:
Date of Exam	:

No. of Pages = 3
No. of Questions = 6

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

Q1: Answer the following questions. [2+3 = 5 Marks]

(a) Define the key stages of the instruction cycle. Briefly describe the activities that take place during each stage.

(b) Application Development team recently developed a Python program consisting of 8,000 instructions in the main function, 1,500 instructions in function G(), and 700 instructions in function H(). The program is executed on a system with a clock frequency of 4.2 GHz, and the architecture maintains an average cycles per instruction (CPI) of 12.

i. Compute the CPU time required for the complete execution of the program.

ii. To achieve a CPU execution time of 25 microseconds, determine the necessary CPI.

Q2: Answer the following questions. [3+ 1 =5 MARKS]

(a) You are designing a data storage and retrieval system that utilizes a data + code scheme for error detection. The encoded data k is represented as: 1101 0101 1101. Your task is to identify if there is an error in the encoded data. If so, determine which bit is affected and the correct data.

(b) Why glass platter is preferred over aluminum in magnetic disc memory? Justify with proper reasons.

Q3: Answer the following questions [5MARKS]

Consider a computer with the following specifications.

- Byte addressable Main Memory with 4MB capacity
- Direct Mapped cache with 1024 lines and line size of 32 bytes
- Clock rate is 1 GHz

(a) Compute the total number of bits needed for representing main memory address?

(b) What is the total capacity of direct mapped cache?

(c) Calculate number of blocks in main memory?

(d) Specify the number of bits needed for tag, line and word offset?

(e) If the Cache access takes 3 ns and main memory access takes 20 ns, and for a particular code the hit ratio is 95%. what is the Average Memory Access Time?

Q4: Answer the following question. [5 MARKS]

The computer data scientists contemplating the preference of using LFU and LRU Replacement Algorithm. The fully associative cache is having 4 lines and the address generated by the CPU corresponds to following block numbers:

4 2 8 5 2 4 1 3 8 1.

Help these Data scientists to choose the better of the two replacement algorithms. Justify your selection with proper table.

Q5: Answer the following questions. **[2.5 + 1 + 1.5 = 5 MARKS]**

(a) A Power PC needs to be designed using Harvard architecture having 32 instructions, source and destination operands referring to 64 Registers and a displacement of value 1003 H. For example, ADD R1, R2, 1003 H where ADD is the Opcode, R1 is source as well as destination Register, R2 is the base Register, 1003H is the displacement that gets added to the base register to generate effective address of the data. Represent the instruction format specifying the various fields and bits required by them.

(b) PC Relative addressing exploits the concept of Spatial reference. State True or False and provide justification.

(c) An address field in an instruction contains a decimal value 10. Find out the corresponding operand located for Indirect Addressing Mode. Support your answer with proper diagram.

Q6: Answer the following questions. **[4 + 1 = 5 MARKS]**

(a) Consider a reservation table for a pipeline with four stages: S0, S1, S2, and S3.

Stages/Time	0	1	2	3
S0	X			X
S1		X		
S2		X	X	
S3	X			

i. Draw the complete pipeline diagram.

ii. Draw time-space diagram showing 3 Tasks (T1, T2, and T3) execution.

iii. How much time that is needed to complete 3 tasks?

(b) Which addressing mode is suitable for array element access?