Question **10**

Not yet answered

Marked out of 0.50

Flag question

Consider main memory contains 4K blocks of 128 bytes each, then the size of tag field in case of Associative mapping is

- a. 13 Bits
- b. 4 Bits
- c. 19 Bits
- d. 12 Bits

Clear my choice

Ans: d

Question **9**

Answer saved

Marked out of 0.50

Flag question

Which of the following options states the correct storage-device hierarchy in terms of decreasing access time?

- a. register, main memory, magnetic disk, magnetic tape
- b. magnetic tape, magnetic disk, cache, main memory
- c. magnetic tape, magnetic disk, main memory, register
- d. magnetic disk, optical disk, main memory, register

Clear my choice

Ans: c

Time left 0:19:48

Question **8**

Answer saved

Marked out of 0.50

Flag question

Instruction execution happens in two cycles: fetch cycle and execute cycle. Which of the following are performed during the Execute Cycle?

- a. Data transfer between CPU and main memory
- b. All Options are correct.
- c. Data transfer between CPU and I/O Module
- d. Some arithmetic operations

Clear my choice

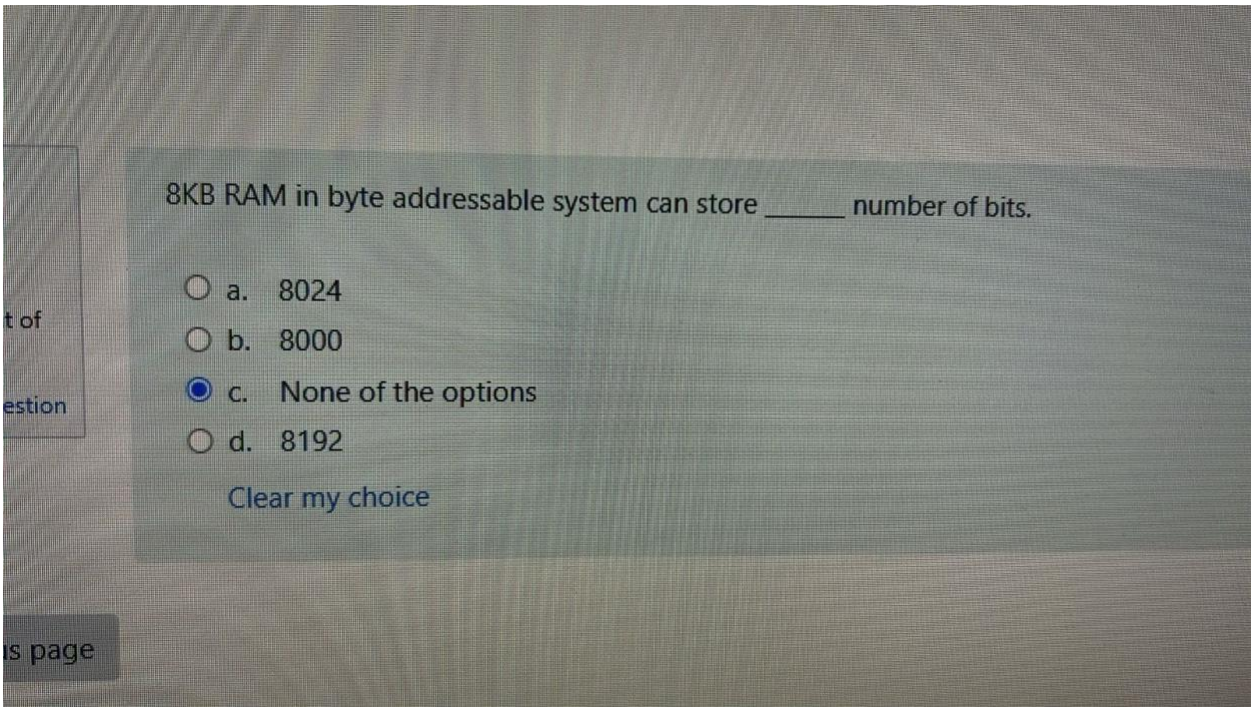
Ans: b

Time left 0:26:59

A computer has a 512 KB, 8-way set associative cache with block size of 64 bytes. The processor sends 32 bit addresses to the cache controller. The number of lines in cache i

- a. None of the options
- b. 128
- c. 512
- d. 8192

Ans: d

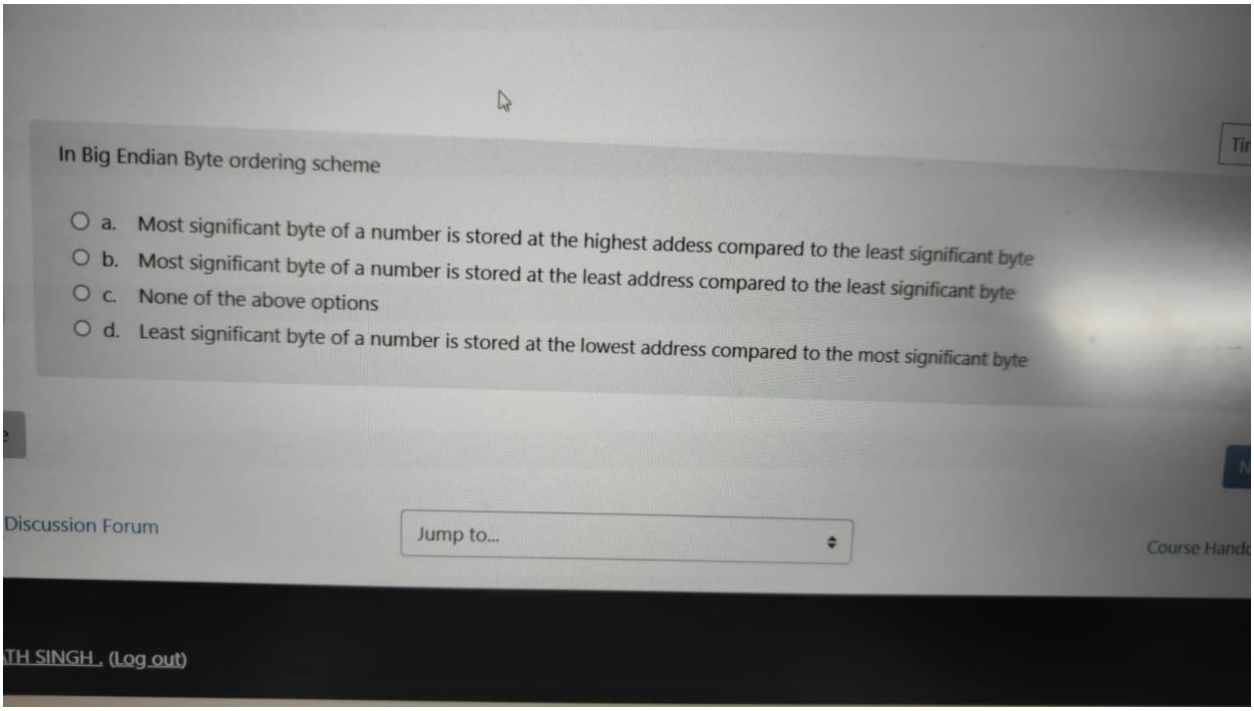


Ans: c

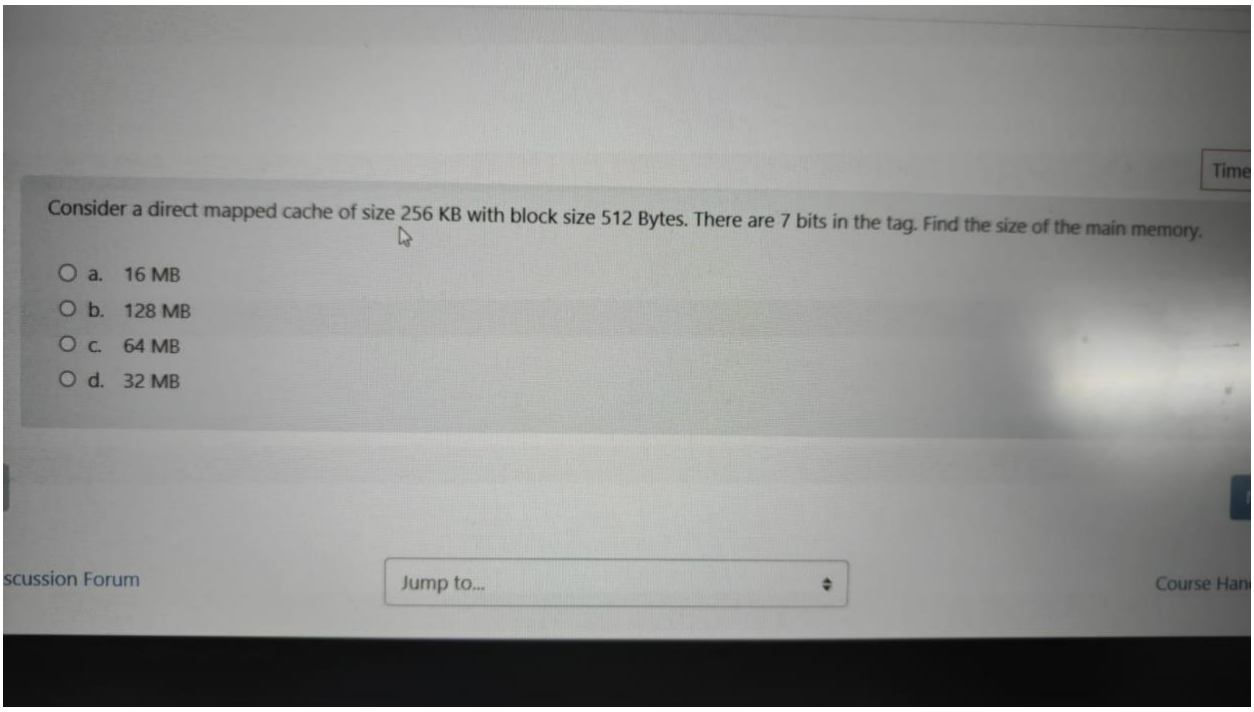
Consider a decimal number 67. _____is the corresponding unpacked BCD number

a. 0110 0010
b. 0000 0110 0000 0111
c. 0010 0110
d. 0010 0000 0110 0000

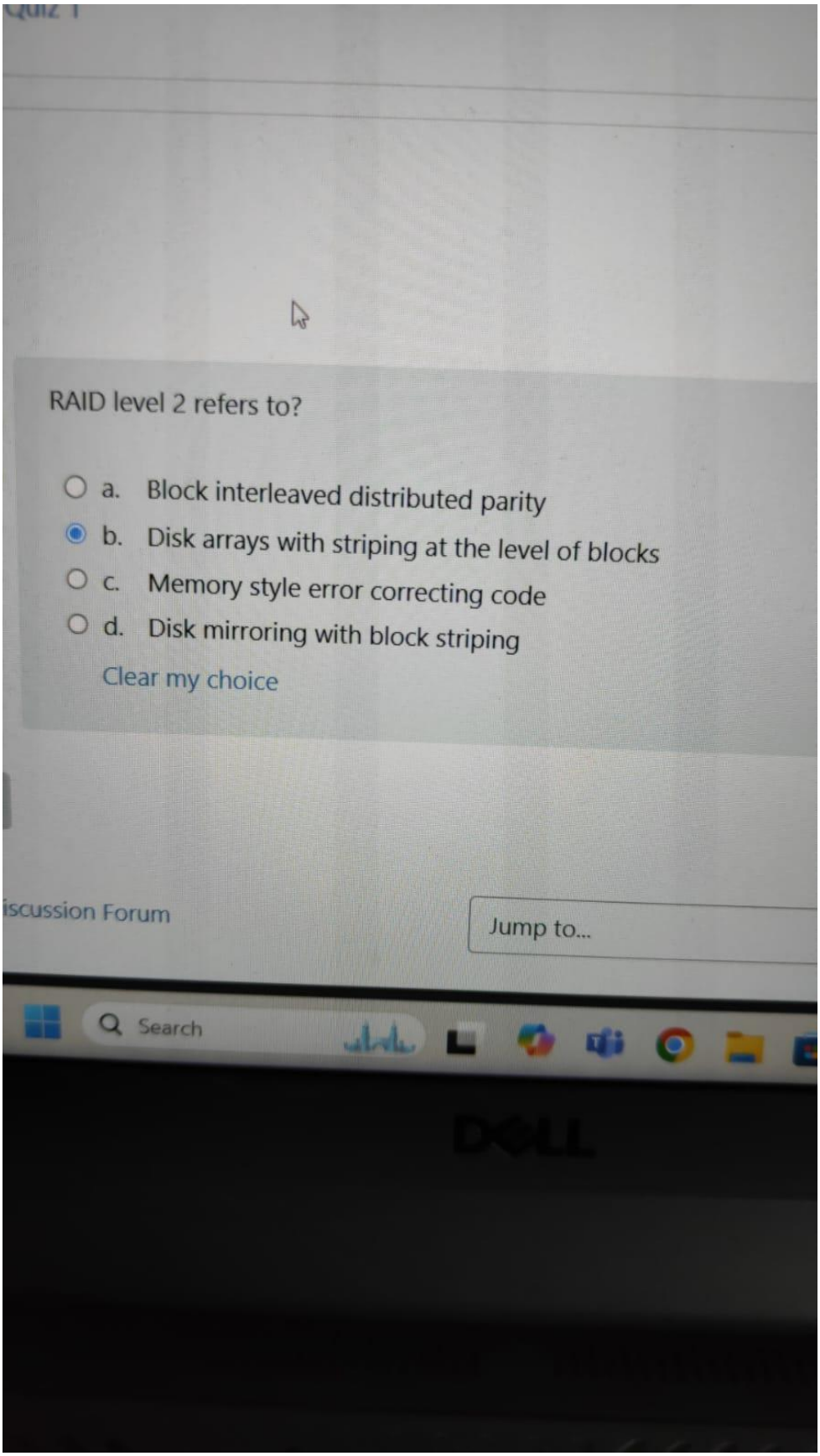
Ans: b


In Big Endian Byte ordering scheme
a. Most significant byte of a number is stored at the highest addess compared to the least significant byte
b. Most significant byte of a number is stored at the least address compared to the least significant byte
c. None of the above options
d. Least significant byte of a number is stored at the lowest address compared to the most significant byte
Discussion Forum
Jump to...
TH SINGH . (Log out)

Ans: b


Consider a direct mapped cache of size 256 KB with block size 512 Bytes. There are 7 bits in the tag. Find the size of the main memory.
a. 16 MB
b. 128 MB
c. 64 MB
d. 32 MB
scussion Forum
Jump to...

Ans: d


RAID level 2 refers to?
a. Block interleaved distributed parity
b. Disk arrays with striping at the level of blocks
c. Memory style error correcting code
d. Disk mirroring with block striping
Clear my choice
iscussion Forum
Jump to...
Search
DELL

Ans: c

___ addressing mode is most suitable to change the normal sequence of execution of instructions.

Question 1Answer

a.

Indirect

b.

PC Immediate

c.

Index with Offset

d.

PC Relative

Ans: c

Consider a word addressable memory of size 8K x 8bits. Total number of bits that can be stored in this memory is

Question 3Answer

a.

8192

b.

65536

c.

8190

d.

65531

Ans: b

Consider a system with a CPU word length of 32 bits, byte-addressable main memory of size 4GB, and a block size of 32 words. The system also contains 512 lines direct-mapped cache. What is the overall size of the cache, including the Tag?

Question 2Answer

a.

16K

b.

24K

c.

64 KB

d.

65 KB

Ans: d

A system has a main memory with 16 megabytes of addressable locations and a 32 kilobyte direct mapped cache with 8 bytes per block. The minimum addressable unit is a byte. Calculate the number of bits for Line Field [or Slot]

Question 1Answer

a.

12

b.

10

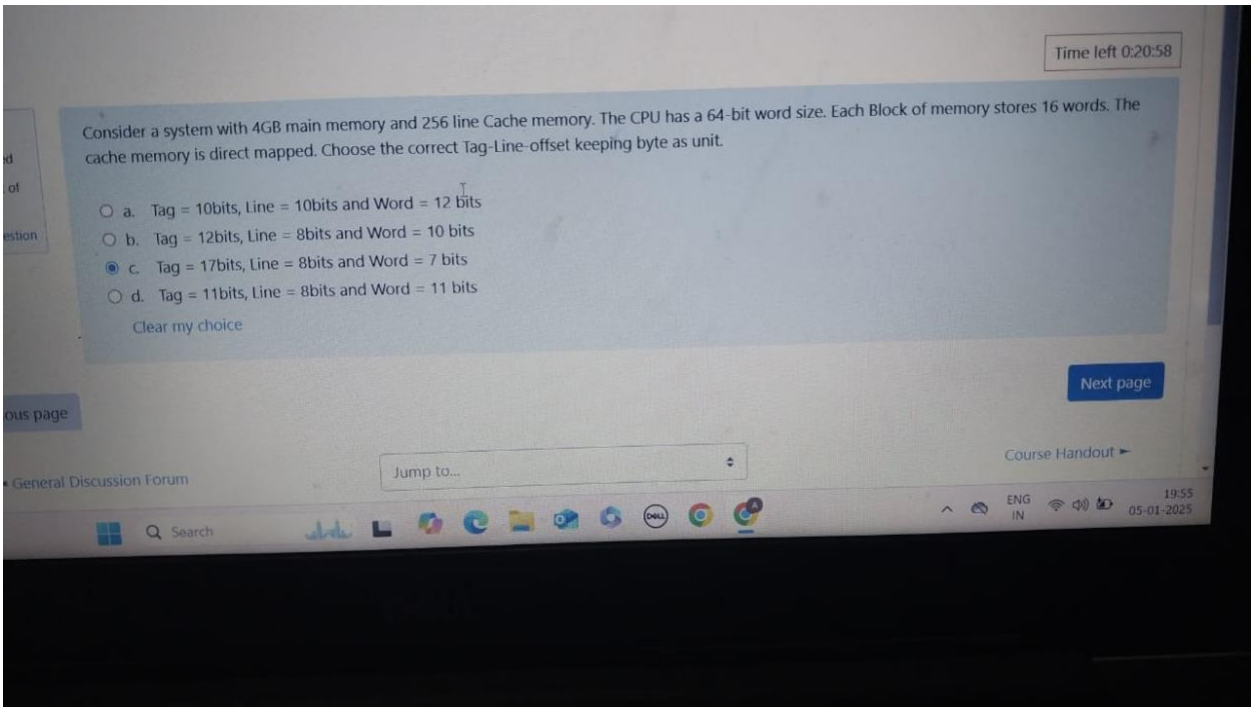
c.

13

d.

11

Ans: a



Ans: d

Which of the following is true about processes in an operating system?

Question 4Answer

a.

They can directly access hardware without the OS.

b.

They are active instances of programs.

c.

They share the same address space.

d.

They execute independently of the operating system.

Ans: b

What does MIPS stand for in performance assessment?

Question 5Answer

a.

Modular Instruction Parallel System

b.

Million Instructions Per Second

c.

Multiple Instruction Processing System

d.

Memory Integrated Processing Speed

Ans: b

Consider a system with a CPU word length of 2 bytes, byte-addressable main memory of size 4GB, and a block size of 32 words. The system also contains 512 lines direct-mapped cache. What is the overall size of the cache, including the Tag?

Question 6Answer

a.

44472 bytes

b.

41472 bytes

c.

16K bytes

d.

64K bytes

Ans: d

In Immediate addressing mode, the operand value is present in the

Question 7Answer

a.

Instruction

b.

Register

c.

IO device

d.

Memory

Ans: a

Which type of memory comes at the top of the memory hierarchy and which at the bottom?

Question 9Answer

a.

Registers and Remote Secondary Storage

b.

Cache and Disks

c.

Registers and Disks

d.

Cache and Tape

Ans: a

8KB RAM in byte addressable system can store ___ number of bits.

Question 10Answer

a.

None of the options

b.

8000

c.

8192

d.

8024

Ans: a

___ addressing mode is most suitable to change the normal sequence of execution of instructions.

Question 2Answer

a.

PC Relative

b.

Index with Offset

c.

Indirect

d.

PC Immediate

Ans: b

The total size of a direct-mapped cache with 64 lines with a line size of 16 bytes is ___,

Question 1Answer

a.

1 KB

b.

64 KB

c.

4 KB

d.

16 KB

Ans: a

Which component is responsible for generating executable file?

Question 5Answer

a.

Loader

b.

Debugger

c.

Linker

d.

Compiler

Ans: d

In fully associative mapping, any memory block maps to

Question 6Answer

a.

any cache line

b.

specific cache line always

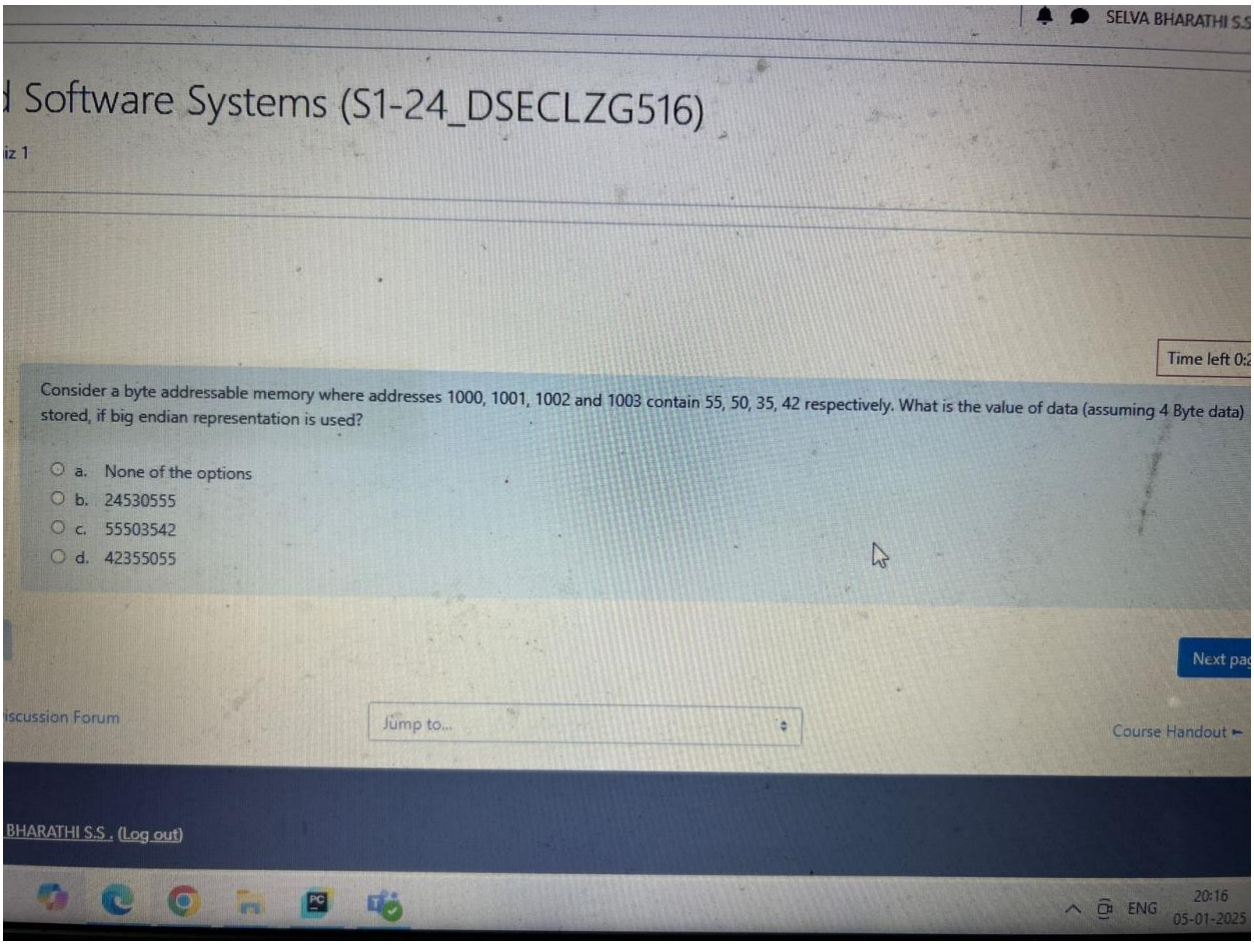
c.

any two cache lines in a set

d.

None of these

Ans: a



Ans: c

In ____ addressing mode, the operand is directly specified in the instruction.

Question 2Answer

a.

Definite

b.

Direct

c.

Relative

d.

Immediate

Ans: d

In Big Endian Byte ordering scheme

Question 5Answer

a.

Least significant byte of a number is stored at the lowest address compared to the most significant byte

b.

Most significant byte of a number is stored at the least address compared to the least significant byte

c.

None of the above options

d.

Most significant byte of a number is stored at the highest addess compared to the least significant byte

Ans: a

The efficient way of reducing the speed mismatch between memory access and CPU operation is by means of

Question 4Answer

a.

Increasing the size of the main memory

b.

Reducing the size of the main memory

c.

Cache Memory

d.

Decreasing the size of the hard disk

Ans: c

Which of the following options states the correct storage-device hierarchy in terms of decreasing access time?

Question 7Answer

a.

magnetic tape, magnetic disk, cache, main memory

b.

register, main memory, magnetic disk, magnetic tape

c.

magnetic disk, optical disk, main memory, register

d.

magnetic tape, magnetic disk, main memory, register

Ans: d

Consider a word addressable memory of size 4K x 8 bits. Total number of bits that can be stored in this memory is

Question 10Answer

a.

33768

b.

4096

c.

32768

d.

4095

Ans: c

A computer has a 512 KB, 8-way set associative cache with block size of 64 bytes. The processor sends 32 bit addresses to the cache controller. The number of sets in cache is

Question 8Answer

a.

None of the options

b.

1024

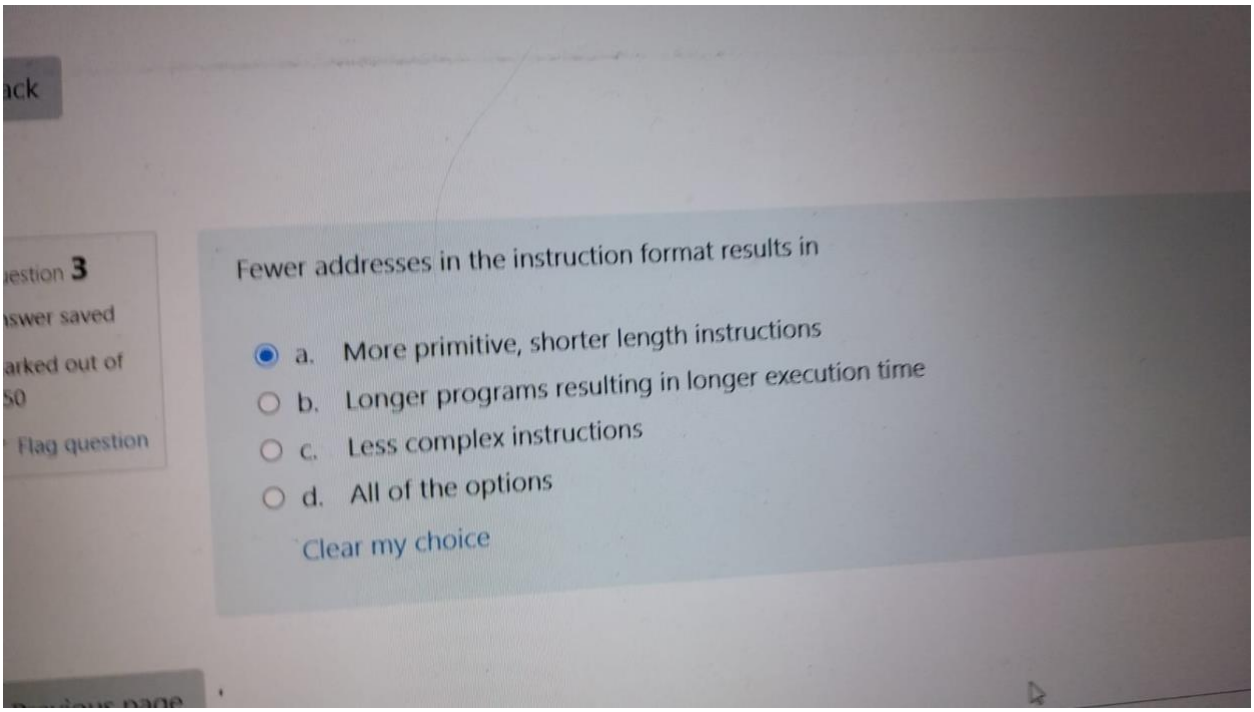
c.

512

d.

128

Ans: b



Ans: d

Which of the following in the memory hierarchy, lower in terms of storage capacity?

Question 5Answer

a.

Cache memory

b.

Secondary memory

c.

RAM

d.

Registers

Ans: d

The presence of interrupt signal raised by the external device is examined by the processor ____

Question 8Answer

a.

during the fetch cycle

b.

at the end of the execution cycle

c.

during the data fetch

d.

during the data storage

Ans: b

In ____ addressing mode, the address of the operand is specified in the instruction format.

Question 9Answer

a.

Immediate

b.

Definite

c.

Relative

d.

Direct

Ans: d

Instruction execution happens in two cycles: fetch cycle and execute cycle. Which activity does not take place during the execution cycle?

Question 10Answer

a.

Data transfer between CPU and I/O module

b.

Processor interprets instruction and performs required actions

c.

Alteration of the sequence of operations

d.

ALU performs the arithmetic & logical operation

Ans: a

Consider a system with a CPU word length of 2 bytes, byte-addressable main memory of size 4GB, and a block size of 32 words. The system also contains 512 lines direct-mapped cache. What is the overall size of the cache, including the Tag?

Question 7Answer

a.

41472 bytes

b.

44472 bytes

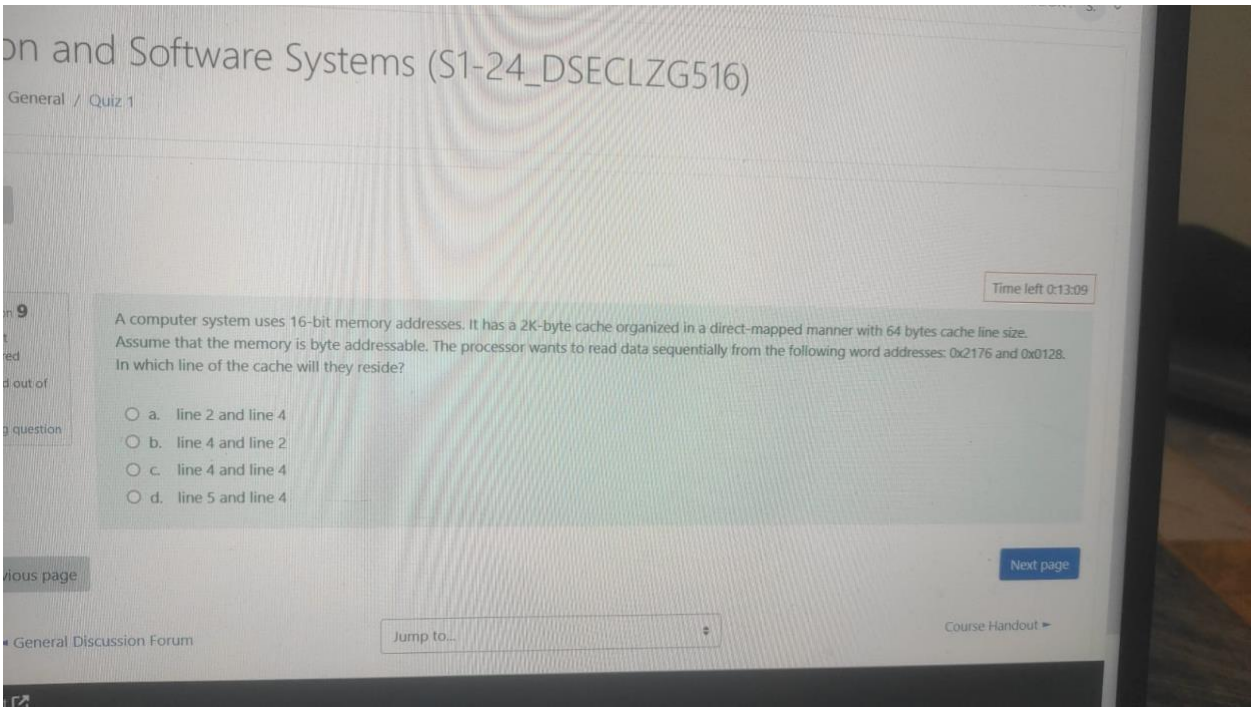
c.

64K bytes

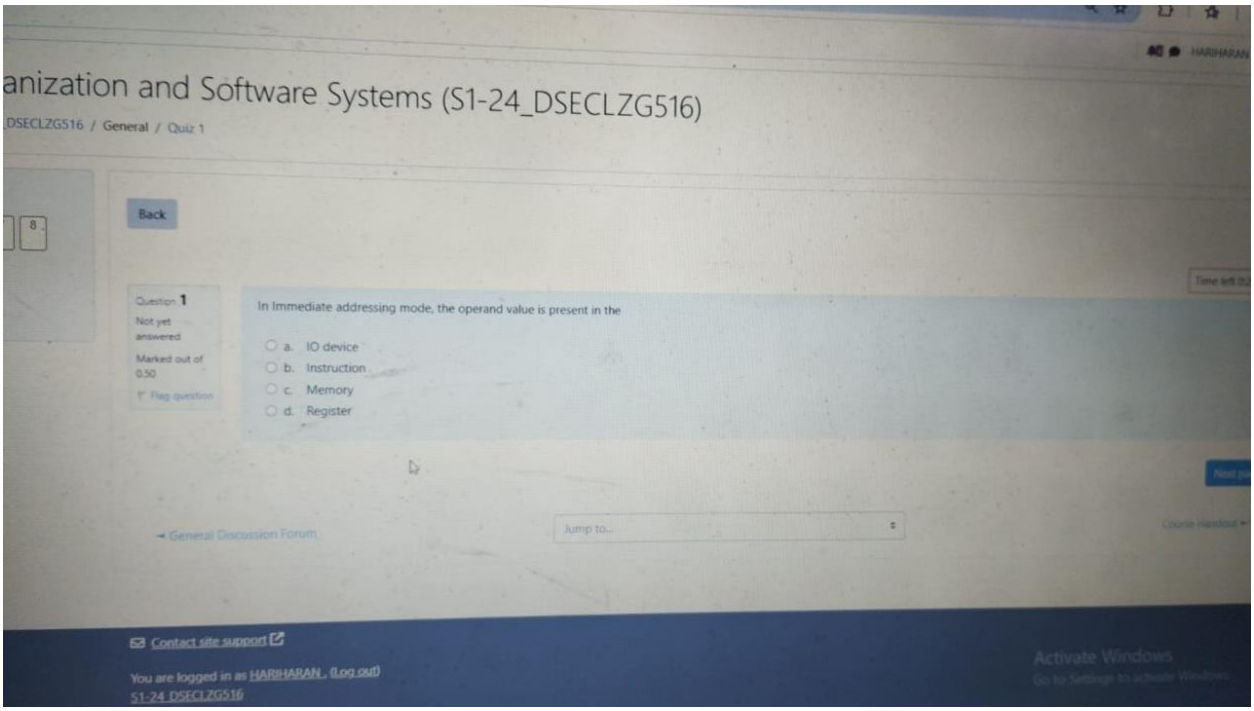
d.

16K bytes

Ans: a



Ans: d



Ans: b

Consider a direct mapped cache having 4 lines, Block 9 will be place in

Question 2Answer

a.

Line 2

b.

Line 0

c.

Line 3

d.

Line 1

Ans: d

Initially, the computer system had an off-chip cache with a 2ns hit time and a 98% hit rate. An on-chip cache with a 0.5 ns hit time and a 94% hit rate is used to improve the computer's performance. The main memory access time is 40 ns. Which cache type is better in terms of Average Memory Access Time (AMAT)?

Question 5Answer

a.

On-chip cache

b.

Both are bad

c.

Both are good

d.

Off-chip cache

Ans: d

A ____ is the smallest unit of information that can be read from or written to the disk

Question 6Answer

a.

Spindle

b.

Sector

c.

Platter

d.

Track

Ans: b

A 22 bit address generates address space of

Question 1Answer

a.

10 M bytes

b.

2 M bytes

c.

1 M bytes

d.

4 M bytes

Ans: d

When the CPU refers to memory and if the word is not found in cache but it is in main memory then it counts as __

Question 9Answer

a.

Pass

b.

Miss

c.

Slip

d.

Hit

Ans: b

Which of the following determines the high hit ratio of the cache memory

Question 2Answer

a.

Size of the ram

b.

Cache Access

c.

Size of the cache

d.

All Options are correct

Ans: d