Birla Institute of Technology & Science, Pilani
Work Integrated Learning Programmes Division
First Semester 2023-2024
M.Tech (Data Science and Engineering)
Compre Exam (EC-3 Regular)

Course No.	: DSECLZG516
Course Title	: Computer Organization and Software Systems
Nature of Exam	: Open Book
Weightage	: 40%
Duration	: 2 hour
Date of Exam	:

No. of Pages = 4
No. of Questions = 6

Note to Students:
1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

Q1: Answer the following questions. [3 + 3 = 6 Marks]

a) Consider two different implementations of machines A and B of the same instruction set. There are four classes of Instructions (I1, I2, I3 and I4) in the instruction set. Machine A has a clock rate of 6 Ghz and machine B has a clock rate of 3 Ghz. The CPI for each instruction class on machines A and B along with the compiler usage of instruction classes are given in the following table:

Instruction Class	CPI on Machine A	CPI on Machine B	Compiler Usage
I1	2	2	30%
I2	3	4	40%
I3	4	4	10%
I4	3	2	20%

Compute:
i) Average CPI of machine A and machine B? [1.5 M]
ii) Among the two machines, which one is faster over other by what value? [1.5 M]

b) Consider the following code for optimization:

```
1. Program Compre1
2. T1 = 10
3. M = 5
4. N = 5 * 2
5. for ( X= 0; X > 10; X++) {
6.        Y1 = T1 + 100 + 10 – 2
7.         Z1 = M * 2 + Y1
8.         if  (T1 = = 0){
9.            Z2 = M * 2 + Y1
10.       }
11. }
12. end
```

Obtain the time efficient code by applying optimization techniques. [3**M]**

Q2: Answer the following questions. **[6 + 1 = 7Marks]**

a) Consider a system with four processes P1, P2 P3 and P4 whose arrival time and CPU and I/0 bursts are given in the table (Note: CPU burst is indicated with a number which is underlined). Assume that the system uses round robin scheduling with time quantum 4 clock cycles. Draw Gantt chart, and fill in the table. Also, find out average turnaround time and waiting time.

Process	Arrival time	CPU-I/O Burst	Finish Time	Turnaround Time	Waiting Time
P1	0	4+3+6			
P2	2	6+1+6			
P3	4	6+2+5			
P4	10	5+2+4			
			Average		

b) What is disadvantage of having a very large time quantum value for round robin scheduling algorithm?

Q3: Answer the following questions **[2 + 4 + 1 = 7 Marks]**

a) The memory system of a certain computer consists of a cache access time of 5 microseconds and a main memory with an access time of 2 milliseconds. The hit ratio is 75%. What is the average access time of the memory system? [2M]

b) Consider the reservation table for 4 stage instruction pipeline processor. S0, S1 etc. indicate pipeline stages.

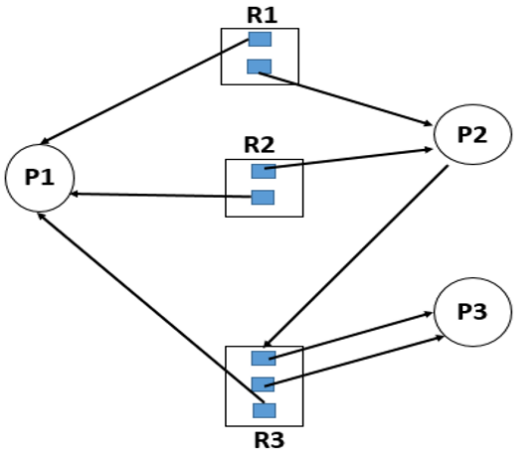
	0	1	2	3	4	5
S0	X					
S1		X			X	
S2			X			X
S3				X		

Answer the following questions:

i. Find out the following: [**2M**]
   a. Collision vector
   b. Simple cycle
   c. Greedy cycle
   d. Minimum Average Latency

ii. Calculate the minimum number of clock cycles required to execute 3 instructions (X, Y and Z) [2**M**]

c) Which process(es) is/are in a deadlock in the following resource allocation graph? Justify your answer. [1M]



Q4: Answer the following question. **[3 + 4 = 7 Marks]**

a) Identify the variables that support temporal and spatial locality of reference in the following code segment:

```
int sales(int price[8]){
        int i = 0;
        int avg=0, total = 0;

        while ( i < 8){
                total = total + price[i];
                i++;
        }
        avg = total/8;
        return total;
}
```

Provide justification for your choice. **Answer without justification will not be awarded any marks.** [3M]

b) The following pseudocode consists of 3 concurrent processes and 3 binary semaphores. The semaphores are initialized as S0 = 1, S1 = 0, S2 = 0.

Process P0	Process P1	Process P2

wait(S1);
signal (S0);
	while(true){
	wait(S0);
	print '0';
	signal(S1);
	signal (S2);
	}
		wait(S2);
		print '1'
		signal (S0);

Assuming that the processes are scheduled as follows:

P1, P2, P0, P0, P2, P0, P2, P0

i. How many times will process P0 will print '0'? [1M]

ii. How many times will process P2 will print '1'?[1M]

iii. What will be the values of S0, S1 and S2, at the end of execution of above sequence?[2M]

Q5: Answer the following questions. **[4 + 3 = 7 Marks]**

a) Consider a computer system with 40 bit logical address, page size of 4M and 8 bytes per page table entry.

i. How many pages are there in the logical address space? [1M]

ii. How many frames are there in the main memory? [1M]

iii. How many entries are there in page table? [1M]

iv. Assume that the user wants to load 16 MB program in to main memory. How much memory is used by the program including its page table? [1M]

b) Newly designed system uses Buddy System to allocate memory blocks. Initially memory has 1KB size. Following are the memory allocation details:

Time	Remarks
T0	A = alloc (252 Bytes)
T1	B = alloc (126 Bytes)
T2	C = alloc (256 Bytes)
T3	D = alloc (201 Bytes)
T4	Free (B)
T5	Free (C)

At the end of T5, there is a request for 128 Bytes, 256Bytes, 383 Bytes and 512 Bytes by processes E, F, G and H respectively (Note: Process E arrived first, then F and so on). What is the largest Chunk that can be allocated at T6? Justify your answer with memory allocation diagram. [3M]

Q6: Answer the following questions. **[2 + 1 + 3 = 6 Marks]**

a) Consider a distributed system with 32 processors and 32 memory modules which are interconnected using omega switching network with two input two output switch. Answer the following questions.

i. Number of stages in the network [0.5 mark]

ii. Number of switches in each stage [0.5 mark]

iii. Number of bits needed in the routing tag [1 mark]

b) Out of four classes of parallel systems under Flynn's classification, which class is best suited for applications such as railway reservation systems? [1M]

c) Having a large number of processor registers makes it possible to reduce the number of memory accesses needed to perform complex tasks. Devise a simple computational task to show the validity of this statement for a processor that has four registers compared to another that has only two registers.[3M]