Birla Institute of Technology & Science, Pilani
Work Integrated Learning Programmes Division
First Semester 2023-2024
M.Tech (Data Science and Engineering)
Mid-Semester Exam (EC-2 Makeup)

Course No. : DSECLZG516
Course Title : Computer Organization and Software Systems
Nature of Exam : Open Book
Weightage : 30%
Duration :
Date of Exam :

No. of Pages = 2
No. of Questions = 6

Note to Students:
1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

Q1: Answer the following questions. [2 + 3 = 5 Marks]

(a) Describe the main categories of interrupts. Provide situations where each interrupt type may be encountered.

(b) Imagine a benchmark program operating on a system with a clock rate of 30MHz. The program involves 75,000 executable instructions, each categorized by instruction type, and each type has a designated count of clock cycles for execution.

Instruction Type	Instruction Count	Cycles Per Instruction
Integer Arithmetic	35000	1
Data Transfer	20000	2
Floating Point	12000	2
Control Transfer	8000	2

Determine the effective CPI, MIPS and execution time for the program.

Q2: Answer the following questions. [2 + 3 = 5 MARKS]

a) The "INgate" company which manufactures Magnetic Disk Drives seeks your help in evaluating critical metrics using the following inputs:

Magnetic Disc pack has 16 surfaces, 256 tracks per surface and 512 sectors per track. There are 512 bytes per sector.

i. What is the capacity of disk pack?
ii. What is the number of bits required to address a sector?

b) Following is the code word generated using Hamming code.

0 1 1 0 1 0 1 0 1 0 1 0

This code word contains data and syndrome bits.

i. Identify the syndrome bits.
ii. What is the decimal equivalent of data?
iii. Is there any error in the data? If so, what is the correct data?

Q3: Answer the following questions [5MARKS]

Consider a memory system that uses a 32-bit address to address byte addressable main memory and a cache with 16 KB line size. Assume a four-way set-associative cache which stores tag of 6 bits along with data blocks in each cache line. Answer the following questions.

a) Calculate the total capacity of main memory in **GBytes.**
b) Calculate number of blocks in main memory.

c) Show the main memory address format with number of bits needed for each field.
d) Calculate number of lines per set and number of sets in cache.
e) Calculate total number of lines in cache.

Q4: Answer the following question. **[4 + 1 = 5 MARKS]**

a) Mr. Joel proposed a new cache replacement algorithm using two existing cache memory replacement algorithm LRU and FIFO. The new algorithm work in two phases. During first phase (clock number 0 to 4), it follows LRU and in second phase, that is (clock number 5 to 9), it follows FIFO. The algorithm is tested with the following main memory block sequence: 3 4 3 6 7 3 8 7 4 3. Find out the hit ratio of the new replacement algorithm. Assume that the cache uses associative mapping. Justify your answer.

	LFU					FIFO				
Time	0	1	2	3	4	5	6	7	8	9
Address	3	4	3	6	7	3	8	7	4	3
L_0										
L_1										
L_2										
L_3										
M/H										

b) Assume the content Register A is 10101101. Find out the content of the Register A for the following cases.
   i. Arithmetic left shift (one time)
   ii. Arithmetic right shift (one time)

Q5: Answer the following questions. **[1 + 4 = 5 MARKS]**

a) Register Indirect addressing results in very fast execution but limited memory space compared to register addressing mode. State True/False with proper justifications.
b) A RISC based processor is designed with 32 instructions and 13 bit addresses. Opcode field of the instruction has fixed number of bits.
   i. There are 60 two address instructions. How many one address instructions can be accommodated?
   ii. Draw the instruction format for one address instruction and two address instruction.
   iii. List 2 differences between 2 address instruction and 3 address instruction with an example.

Q6: Answer the following questions. **[3 + 2 = 5 MARKS]**

a) Consider a reservation table for a pipeline with four stages: S0, S1, S2, and S3.

Stages/Time	0	1	2	3
S0		X		X
S1			X	
S2		X		
S3	X			

   i. Draw the complete pipeline diagram.
   ii. Draw time-space diagram showing 3 Tasks (T1, T2, and T3) execution.

b) State whether the following statements are **True** or **False** with proper justification. Answers without proper justification will not be given any marks.
   a. RAID 0 is not a true member RAID family.
   b. During instruction fetch operation, the instruction is directly transferred to the instruction register from the Main Memory before it is decoded.