Experimental Techiques in Particle Physics

Radiation a Challenge for Electronics and Detectors

Lecture 10, 2021-01-12

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Fraunhofer INT

Radiation Fluence inside Detectors

Promising new physical results are related to some very rarely produced particles

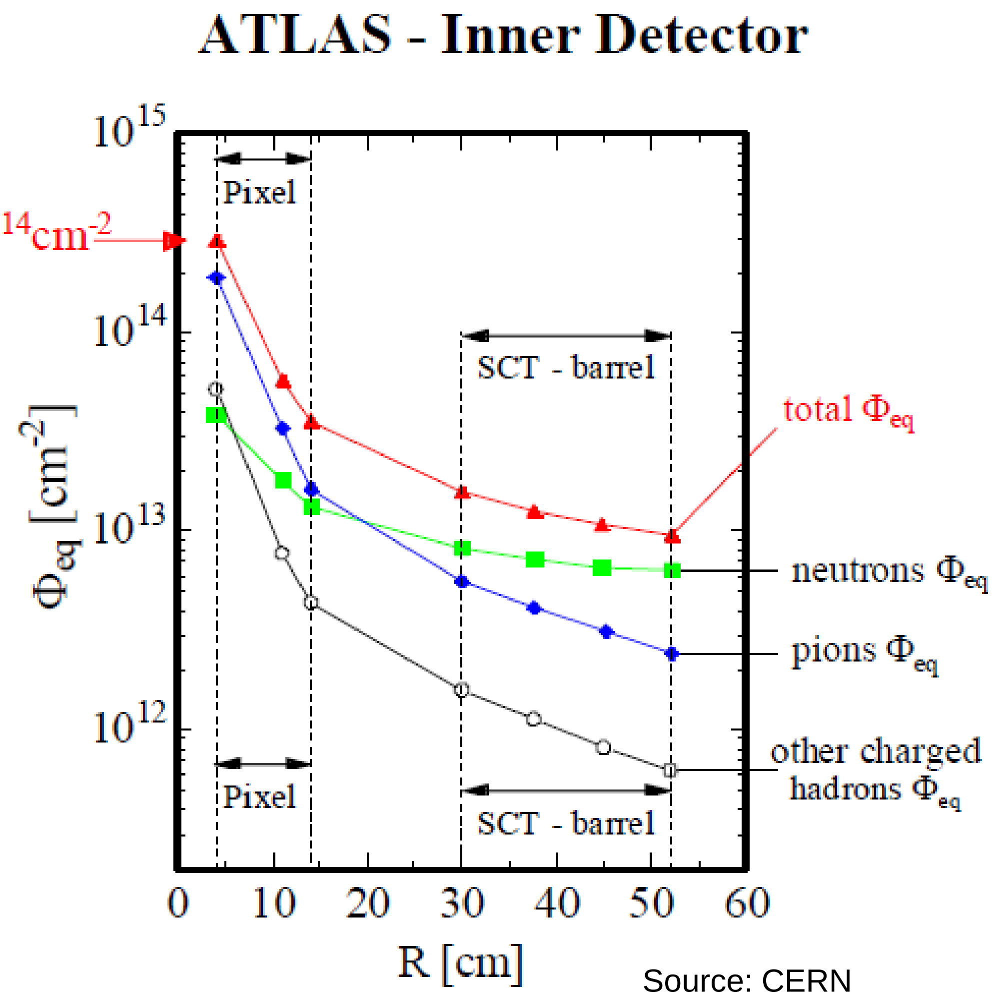
- High event rate (10^9/s at LHC), very good spatial resolution and fast signal read out required, can be fulfilled with silicon detectors, however:

Detectors and electronics will be harshly irradiated!

- ATLAS - Inner Detector:
  Φ_{eq} up to 3 x $10^{14}cm^{-2}$ per operational year
- 10 years of operation have to be guaranteed

What is the impact on silicon detectors?

How can we make silicon radiation harder?



Source: CERN

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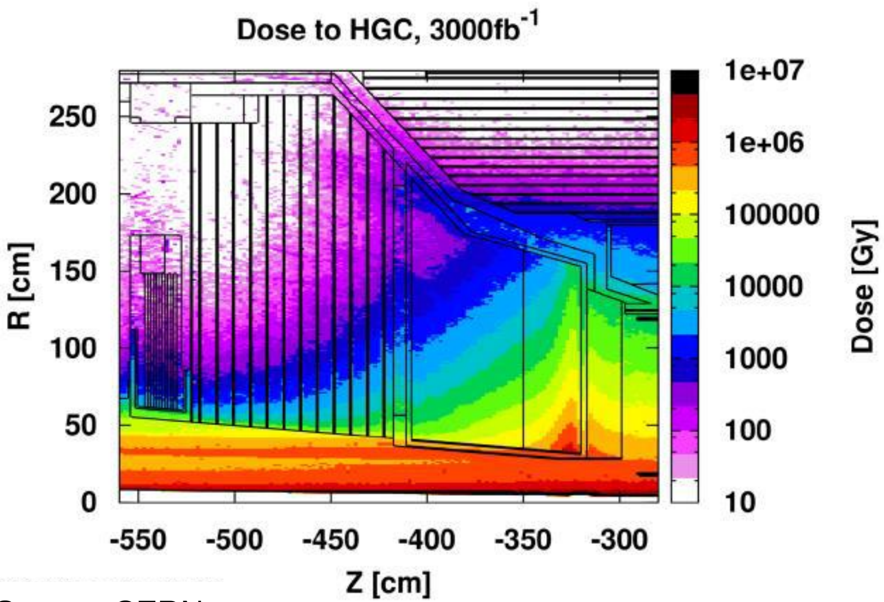
Radiation Fluence inside Detectors – Next Level

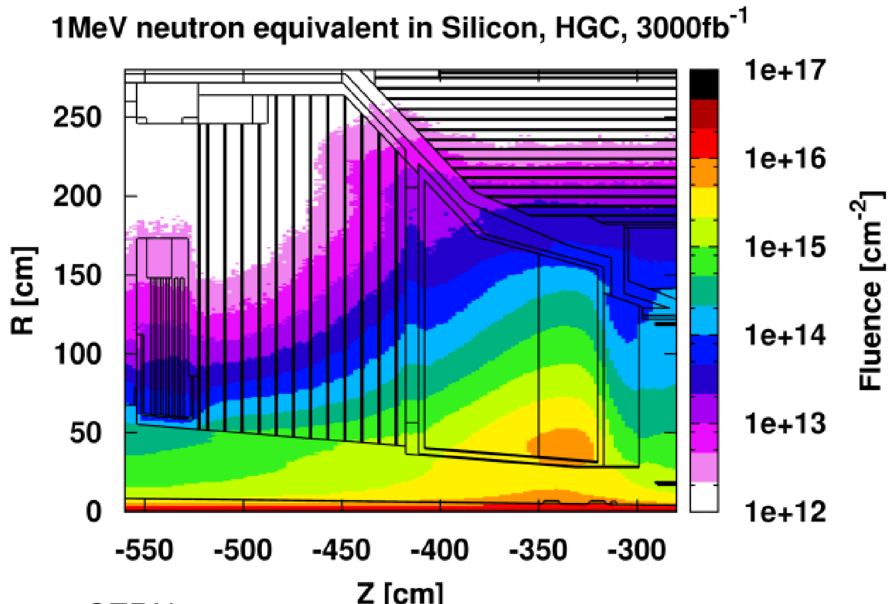
For the HL-LHC (High-Luminosity LHC) detector electronics,

- to operate between 2025 and 2035,
- at ionizing radiation levels of up to 10 MGy (1 GRad) in silicon and
- 10^{16} (1 MeV n_{eq})/cm^2 are expected,

thus requiring the use of radiation-hard by design electronics.



Source: CERN



Source: CERN

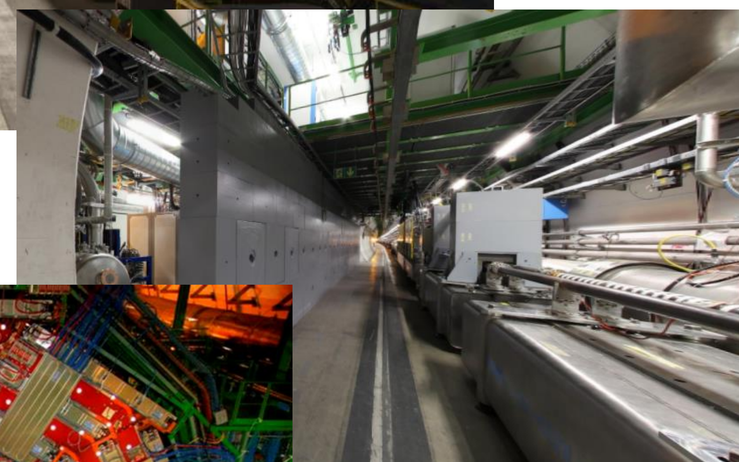
Critical Equipment near the Accelerator

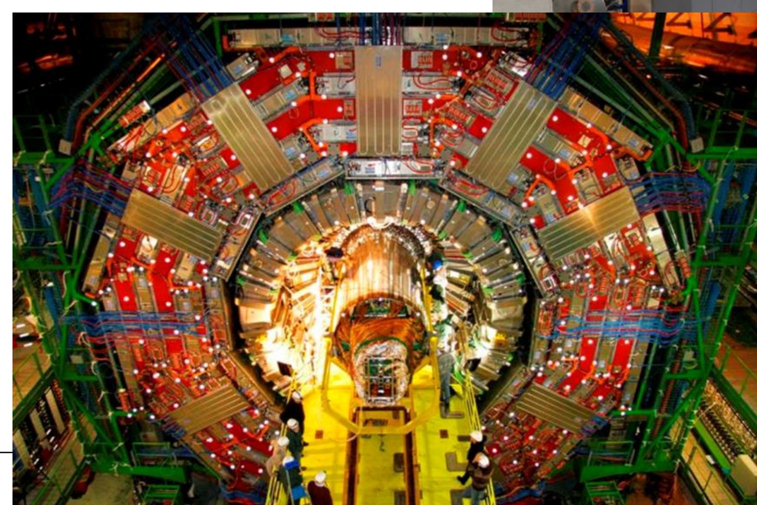
Main reason requiring operation of electronics near accelerators:

- Cable distance to accelerator elements (detectors, magnets, vacuum, cryogenics, RF, beam instrumentation…)
- Lack of radiation-safe areas around accelerator (underground machine)

Main drivers for use of commercial systems:

- Cost
- Performance
- Availability and timeline

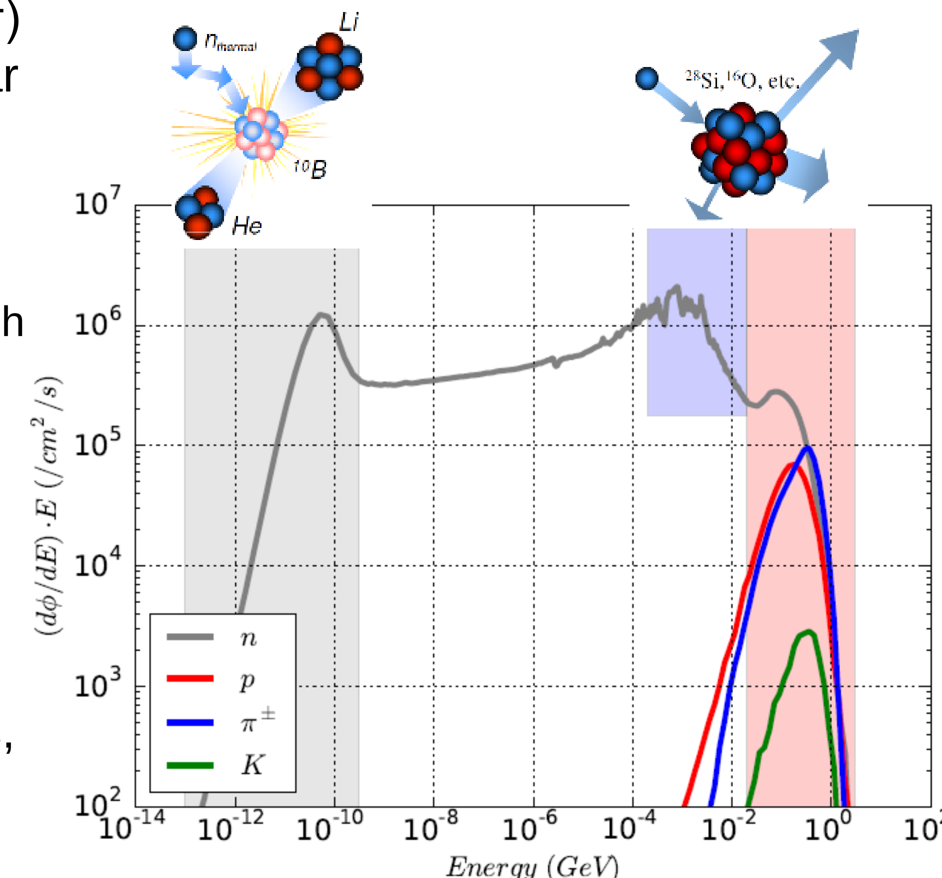




Source: CERN

Mixed Radiation Fields inside Shielded Alcoves

- Main SEE contributors: hadrons (n, p, π) indirectly through ionization after nuclear interactions
  - Two main energy intervals can be distinguished:
    - thermal neutrons (causing SEEs through 10B capture)
    - equivalent high-energy hadrons (HEH with energy > 20 MeV + intermediate energy neutron contribution)
  - so the sensitivities to HEH and thermal neutrons (if relevant) need to be qualified
- Main TID contributors: charged hadrons, electrons/positrons, photons
- Main DD contributors: neutrons



Source: CERN

So in areas (e.g. shielded alcoves) with typical annual fluences ranging from 10^5 to 10^9 HEH/cm^2 COTS based systems seems feasible.

Commercial-Grade vs Rad-Tolerant Grade FPGA

- Commercial-grade electronics are not specially manufactured to be operated in radiation environments and so they do not tolerate radiation.
- Some vendors offer dedicated radiation-tolerant FPGAs:
  - But the are 100 to 1000x more expensive
  - Because they are build typically for the space or military market where only small quantities are needed.
- However high-energy physics experiments typically use hundreds or thousands FPGAs.

Source: ALTERA

Source: XILINX

So HEP normally buy commercial-grade (COTS) FPGA..

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Radiation Effects on Commercial-Grade FPGA

FPGA Type	TID	SEU in Configuration	SET	Destructive Events (SEL, etc.)
SRAM		sensitive	sensitive	insensitive
Flash		insensitive	sensitive	insensitive
Antifuse		insensitive	sensitive	insensitive

SRAM-Based FPGA

- SRAM-based FPGA store logic cells configuration data in the static memory (organized as an array of latches).
- Since SRAM are volatile and can't keep data without power source, such FPGAs must be programmed (configured) upon start.
- There are two basic modes of programming:
  - *Master mode*, when FPGA reads configuration data from an external source, such as an external Flash memory chip.
  - *Slave mode*, when FPGA is configured by an external master device, such as a processor. This can be usually done via a dedicated configuration interface or via a boundary-scan (JTAG) interface.
- SRAM-based FPGAs include most chips of Xilinx Virtex and Spartan families and Altera Stratix and Cyclone.
- SRAM-based FPGAs have an internal flash memory blocks, thus eliminating the need to have an external non-volatile memory (ref. Xilinx Spartan-3AN family).

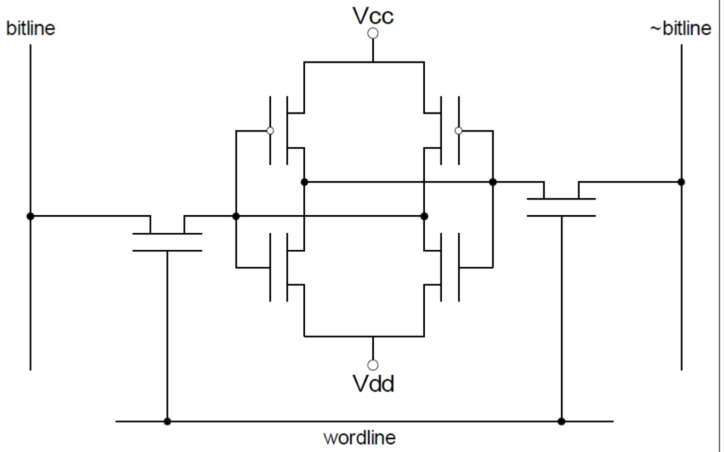

Fig. 1: SRAM memory cell

Source: XILINX

SRAM-Based FPGA: Pros and Cons

- Re-programmable
  - can add features after installation,
  - allows to try more complex logic or to react to external conditions
- Fastest FPGA technology
  - Newest silicon process (e.g. 16 nm XILINX UltraScale+)
  - LVDS ports with 1.6 Gbps or SERDES with 32 Gbps
- Best TID tolerance
  - More than 5 kGy(Si) with some part types much higher

- Consumes the most power
- Is sensitive to SEUs in the Configuration memory
- Needs scrubbing (increases power consumption further)

Flash-Based FPGA

- The true flash-based FPGAs shouldn't be confused with the previous type. The SRAM-based FPGAs with internal flash memory use flash only during startup to load data to the SRAM configuration cells.
- On the contrary, true flash-based FPGA uses flash as a primary resource for configuration storage, and doesn't require SRAM (a similar technology is used in CPLDs – complex programmable logic devices, but the FPGA architecture is very different from that of CPLD).
- This technology has an advantage of being less power consumptive.
- Flash-based FPGAs are also more tolerant to radiation effects.
- Flash-based FPGA families such as *Igloo* and *ProASIC3* are manufactured by ACTEL.
- As in the previous case, using flash-based FPGAs can be a solution to prevent unauthorized bitstream copying.

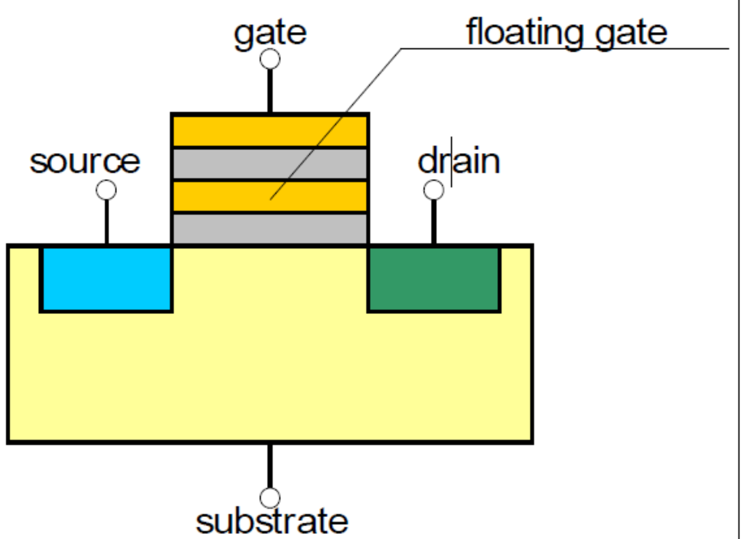

Fig. 2: A floating-gate transistor used in flash memory

Source: ACTEL

Flash-Based FPGA: Pros and Cons

- Re-programmable
  - can add features after installation,
  - allows to try more complex logic or to react to external conditions
- Reliability
  - No SEUs in Configuration memory
- Intermediate density and speed
  - LVDS port up to 1.25 Gbps and SERDES up to 12.7 Gbps

- Intermediate TID tolerance
  - Ca. 700 Gy(Si) on Igloo2 or SmartFusion2
- Ability to be reprogrammed fails at much lower TID levels
- Design tools not as mature as for SRAM-based FPGAs

Antifuse-Based FPGA

- Antifuse-based FPGAs are different from the previous ones in that they can be programmed only once.
- The *antifuse* is a device that doesn't conduct current initially, but can be "burned" to conduct current (the antifuse behavior is thus opposite to that of the fuse, hence the name).
- The antifuse-based FPGA can't be then reprogrammed since there is no way to return a burned antifuse into the initial state.
- Antifuse-based device families include *Axcelerator* produced by Actel.

Antifuse-Based FPGA: Pros and Cons

- Reliability
  - No SEUs in Configuration memory

- Limited availability
- Only programmable once
- Lowest speed, e.g. 700 Mbps LVDS ports
- Intermediate TID tolerance: ca. 800 Gy(Si)

Example of Use of FPGAs at CERN

Use cases at CERN

	Present	Plans for next generation
nanoFIP (accelerators)	ProASIC3. [1]	investigating Smartfusion2 and nanoXplore FPGA [2]
LHC SciFi , Cal, and Muons	Antifuse AX , ProASIC	Igloo2
LHCb RICH	Antifuse AX , ProASIC	Xilinx Kintex7 [4]
ALICE ITS [7]	no FPGAs	Xilinx ultraScale(+) , ProASIC3L (scrubber).
ALICE TOF	ProASIC	Igloo2
ALICE TPC	SmartFusion2	
ATLAS muon RPC	Xilinx	Xilinx
ATLAS TGC Muon	Antifuse AX	Plan A : Xilinx Kintex-7 Plan B : PolarFire
CMS RPC Muon	Xilinx SPARTAN3; Actel ProASIC+ as blind scrubber, every 10 minutes.	Plan A : Xilinx Kintex7 and SmartFusion2. Plan B : PolarFire
CMS DT Muon	no FPGAs	PolarFire
CMS HCAL [10]	ProASIC3L, igloo2	

Source: CERN

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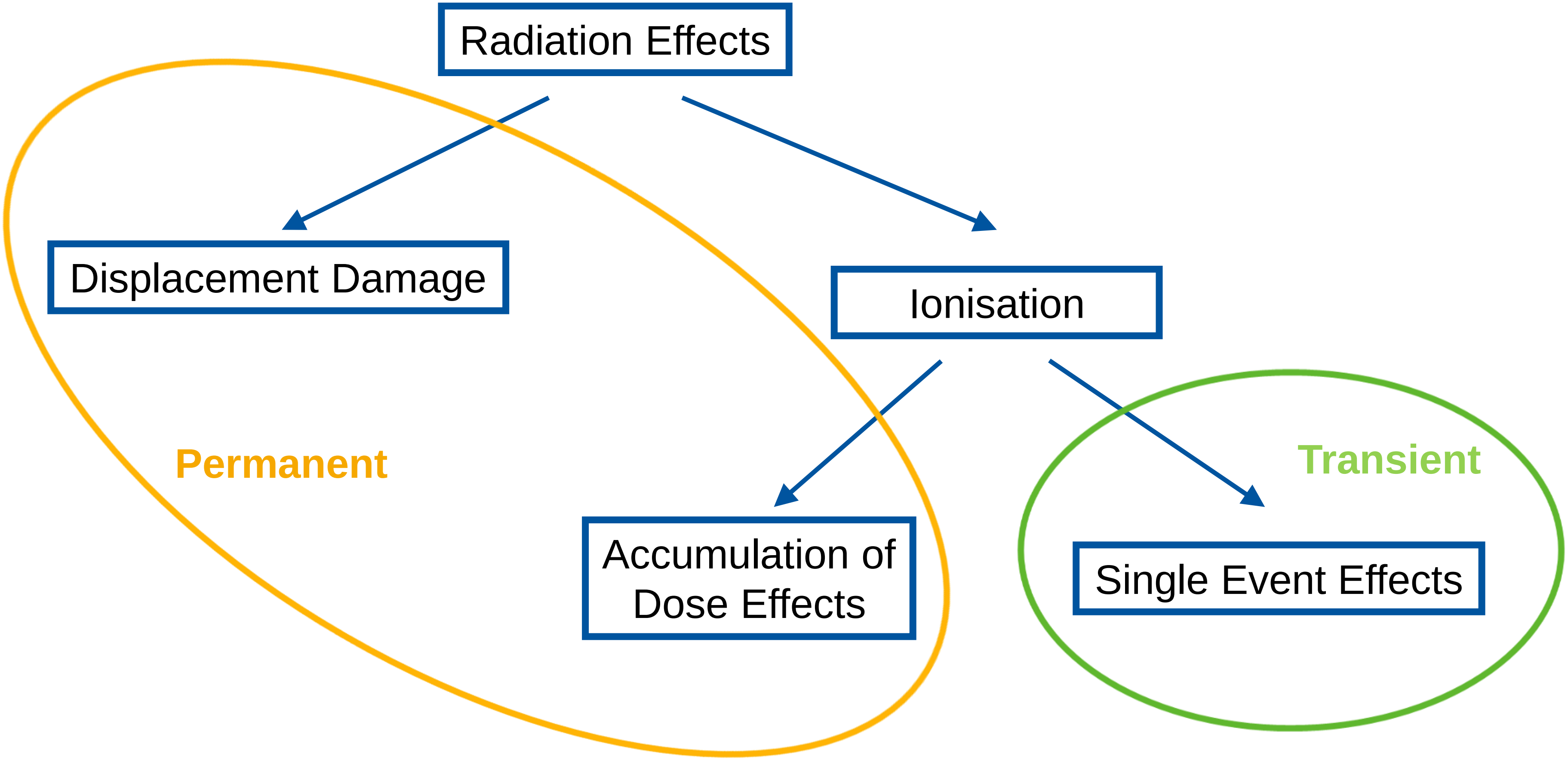
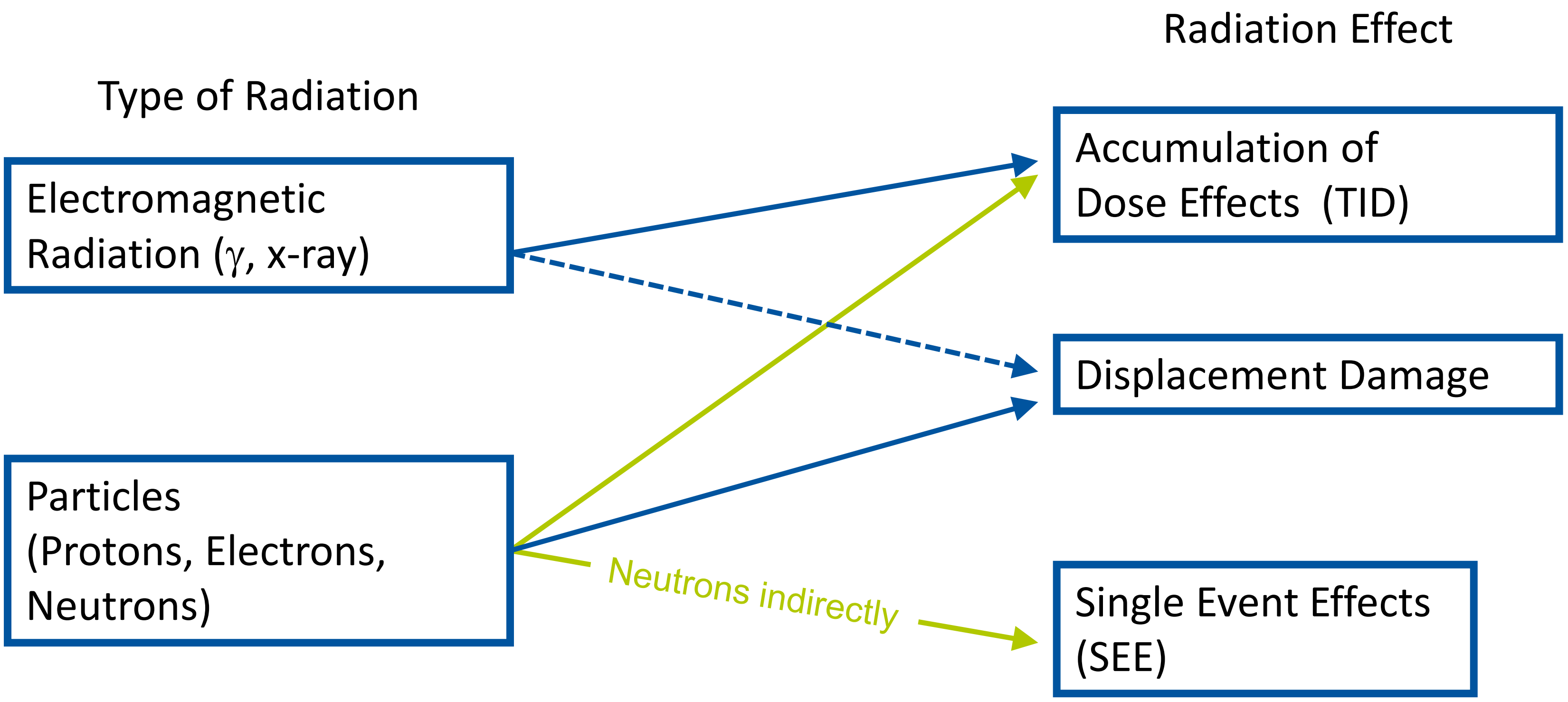
Classification of Radiation Effects

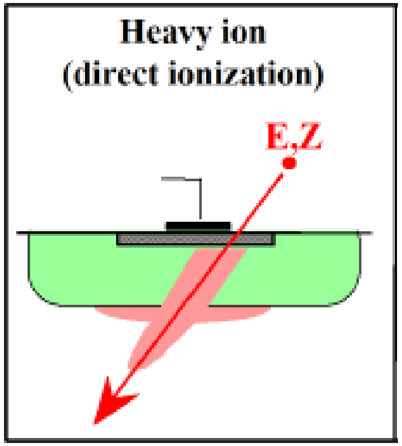


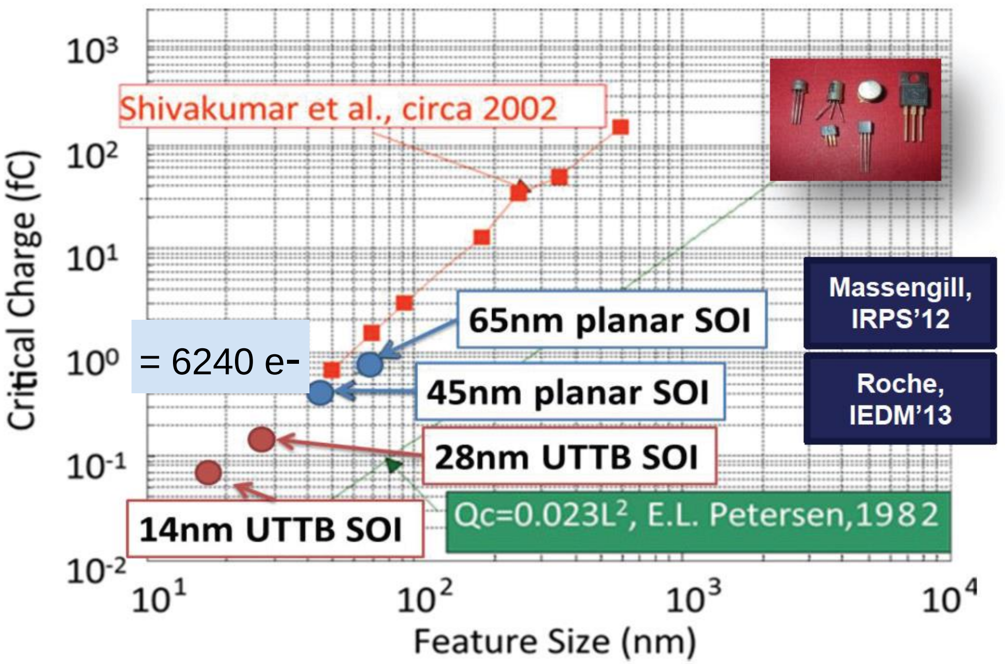
Radiation Effects of Different Types of Radiation

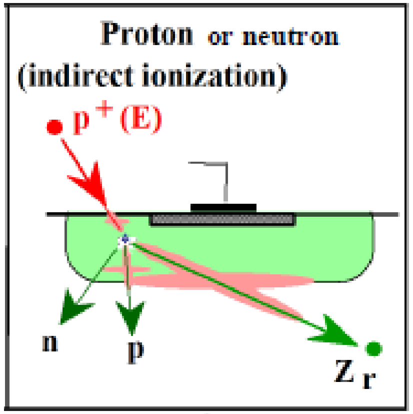


Mechanism for Inducing a Single-Event Effect

- Deposition of energy of primary particle in matter
- Creation of electron hole pairs
- Transport of charge carriers (drift and diffusion)
- Collection of carriers in sensitive areas of the devices (= depleted pn-junction)
- „Electrical answer“ of the system, if sufficient charge is collected (i.e. threshold = critical charge)







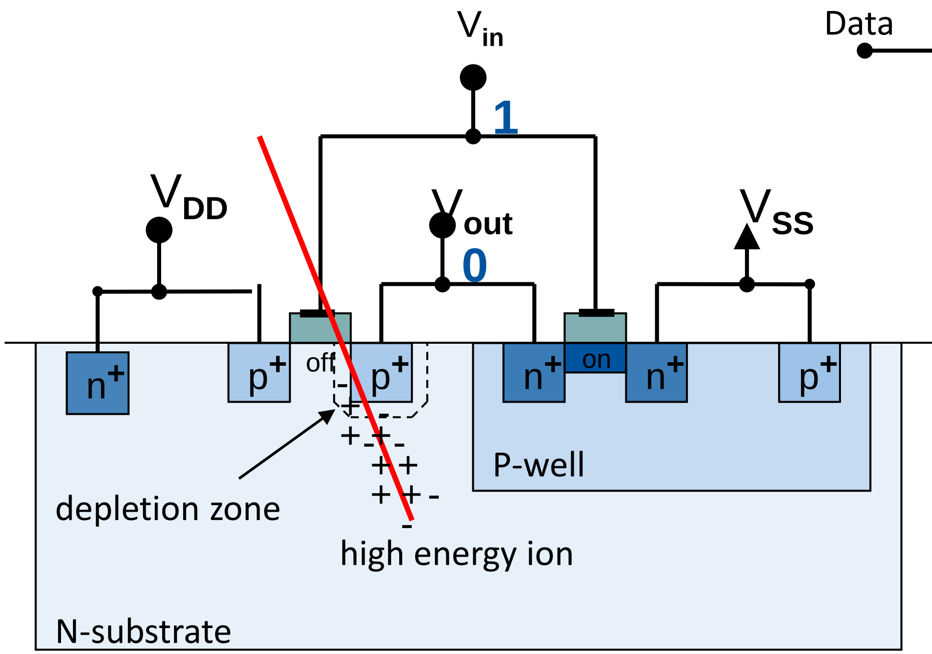
Source: R. Schrimpf, „Single-Event Effects in Emerging Device Technologies“, 2015 MRQW Proceedings

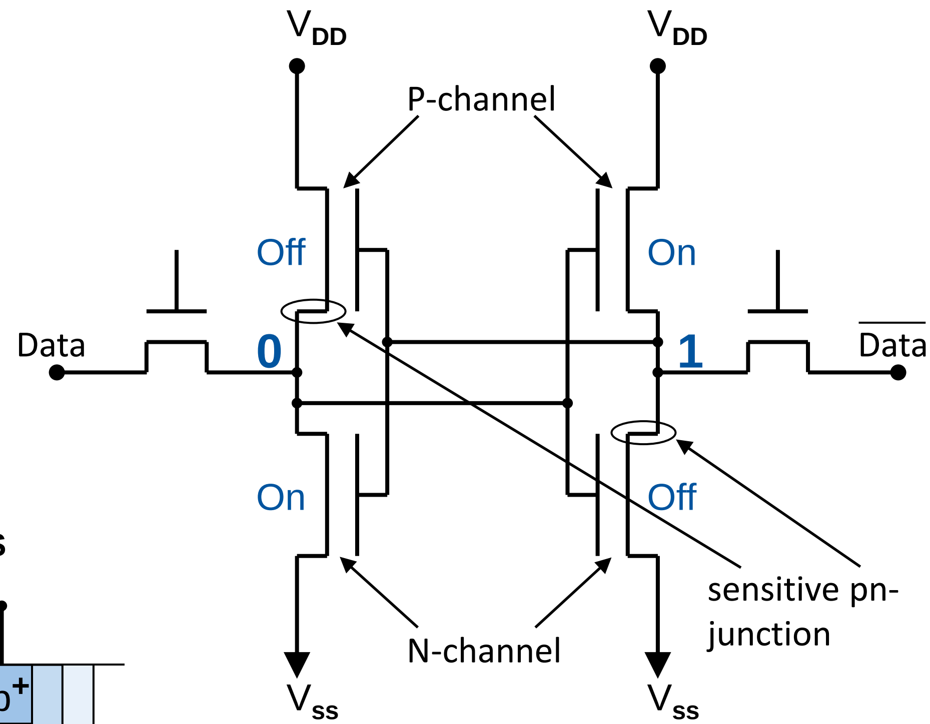
Single-Event …

Upset – SEU	Change of stored information	Memories, latches in digital systems
Multiple Bit/Cell Upset – MBU, MCU	Change of information in several logical or physical neighboring memory cells	Memories, latches in digital systems
Functional Interrupt – SEFI	Loss of normal functionality or operation	Complex devices with internal control logic
Transient – SET	Pulse of certain amplitude and length	Analogue und mixed-signal devices, photonics
Latchup – SEL	State of strongly increased current consumption	CMOS, BiCMOS
Gate Rupture – SEGR	Local disruption of the gate isolation	Power MOSFET
Burnout – SEB	Triggering of a permanent short circuit	BJT, Power MOSFET

Soft Error - SEU

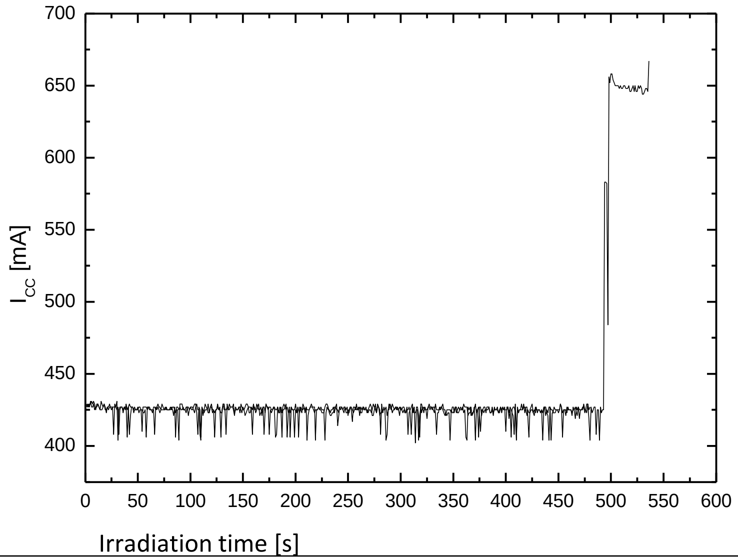
- Single-Event Upset („soft – error“)
  - Example 6-Transistor SRAM-Cell
  - CMOS technology

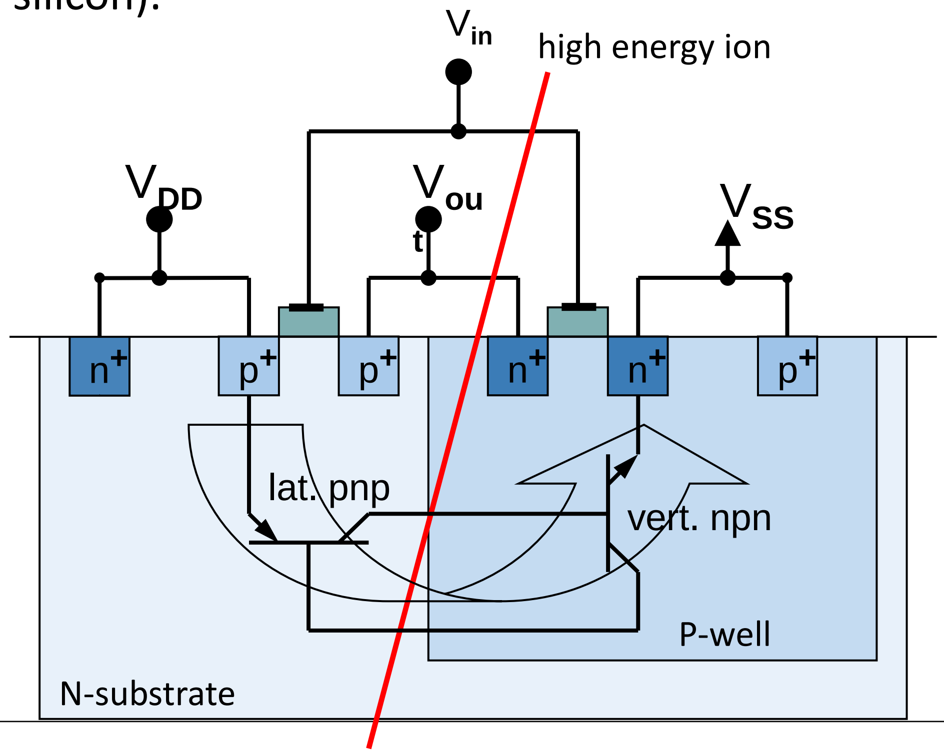




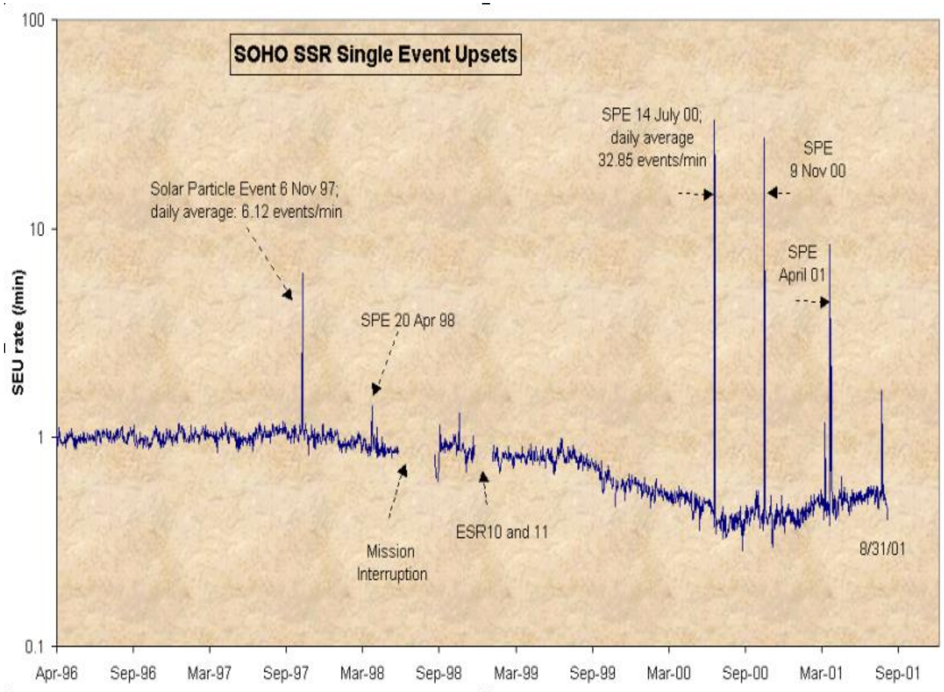
Destructive SEL

- Devices in CMOS technology are prone to Single-Event Latchup
  - Ignition of a parasitic thyristor (pnpn-structure).
  - Current consumption increases strongly.
  - If not cleared immediately, device will be destroyed through thermally (local melting of silicon).

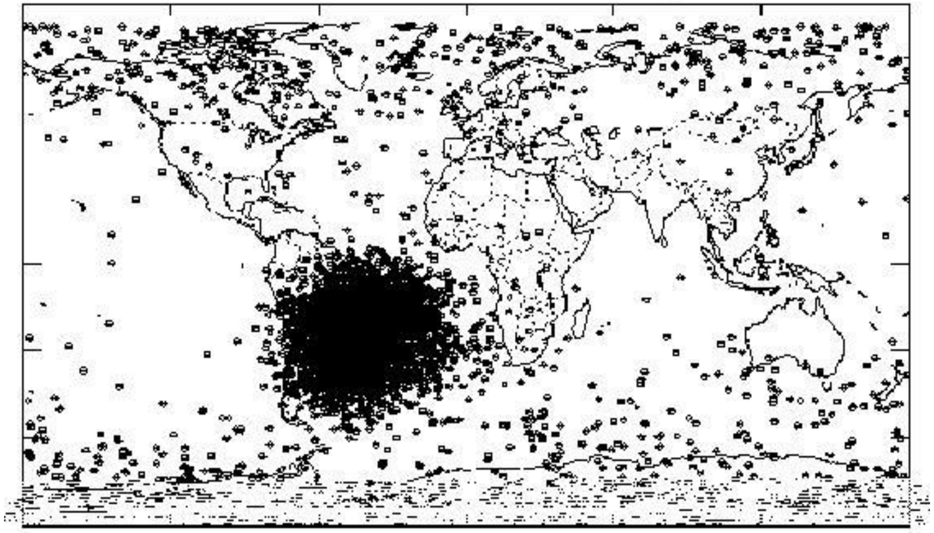




SEEs in Space

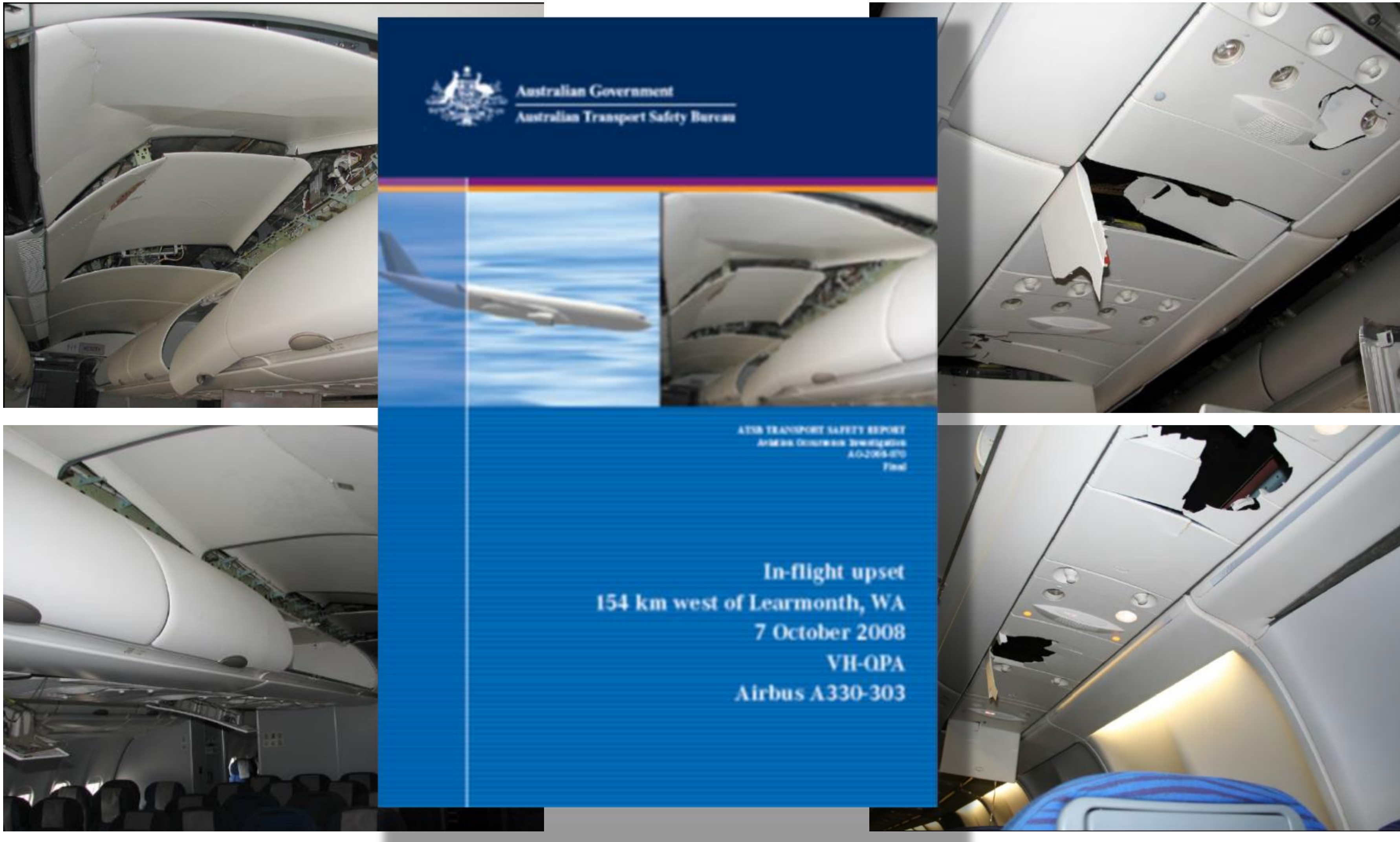


Source: NASA / ESA



Source: ESA

SEE in Airbus A330 Avionics - Qantas Flight 72



Source: ATSB

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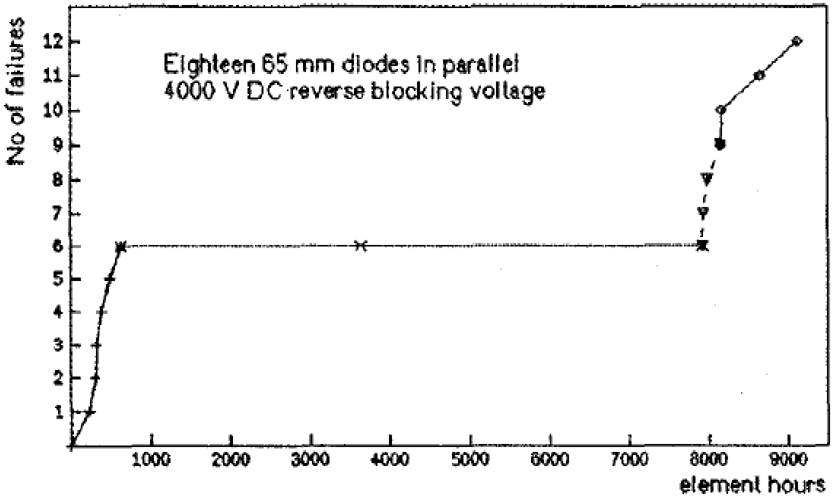
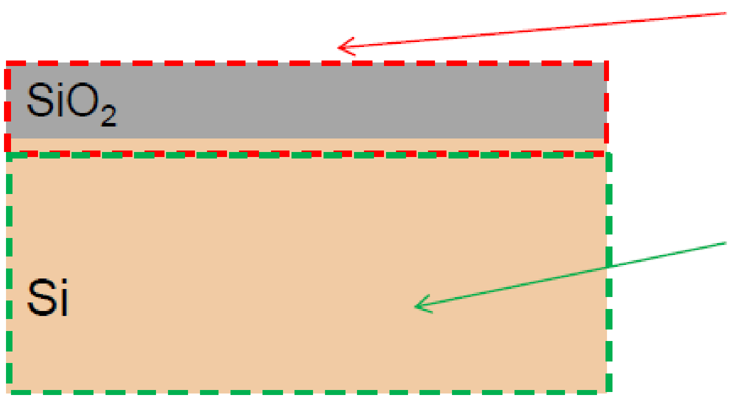
SEB in Power MOSFET Induced by Atmospheric Neutrons



Source: Proc. 6th Internat. Symp. Power Semiconductor Devices & IC's, Davos, Switzerland, May 3 1 - June 2 1994.

Total Dose and Displacement Damage Effects

- Ionization damage energy absorbed by ionization in insulating layers (SiO_2)
  - Charge carriers drift and diffuse to other regions
  - Charges can be trapped
  - => unintended concentration of charge, parasitic electric fields

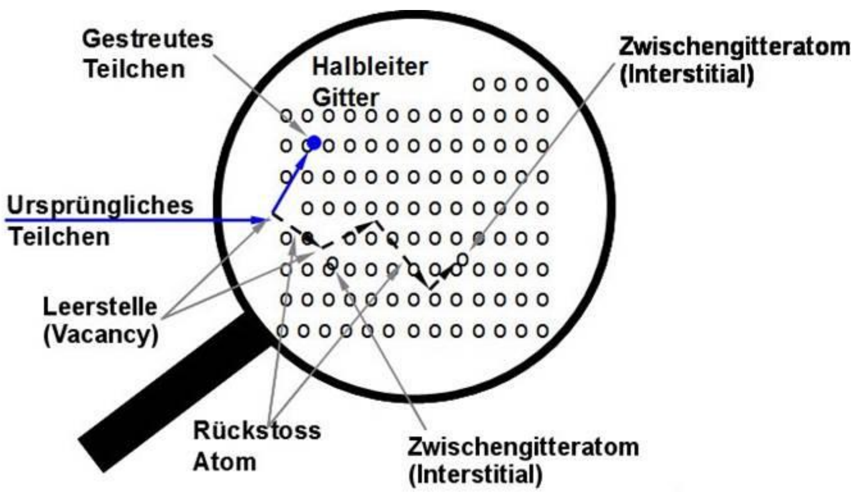


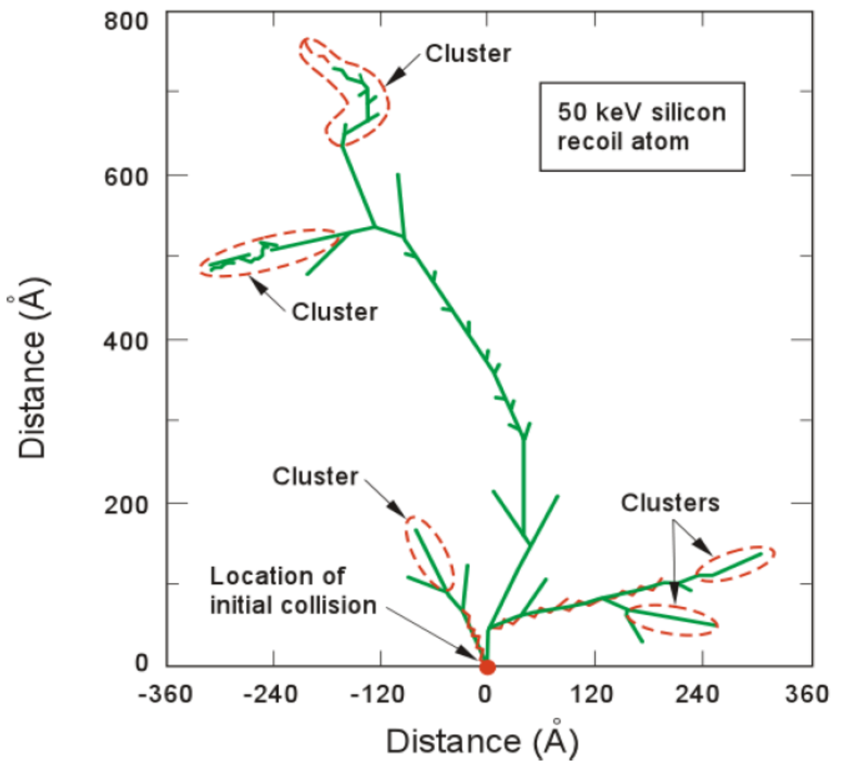
Region affected by ionizing energy loss (IEL) - surface damage

Region affected by non-ioizing energy loss (NIEL) – bulk damage

Displacement Damage (TNID) – Basics (I)

- Atoms will be knocked from their lattice positions by the impinging particle and leave behind vacancies (Frenkel pairs).
- If their energy is sufficient they can knock out more atoms.





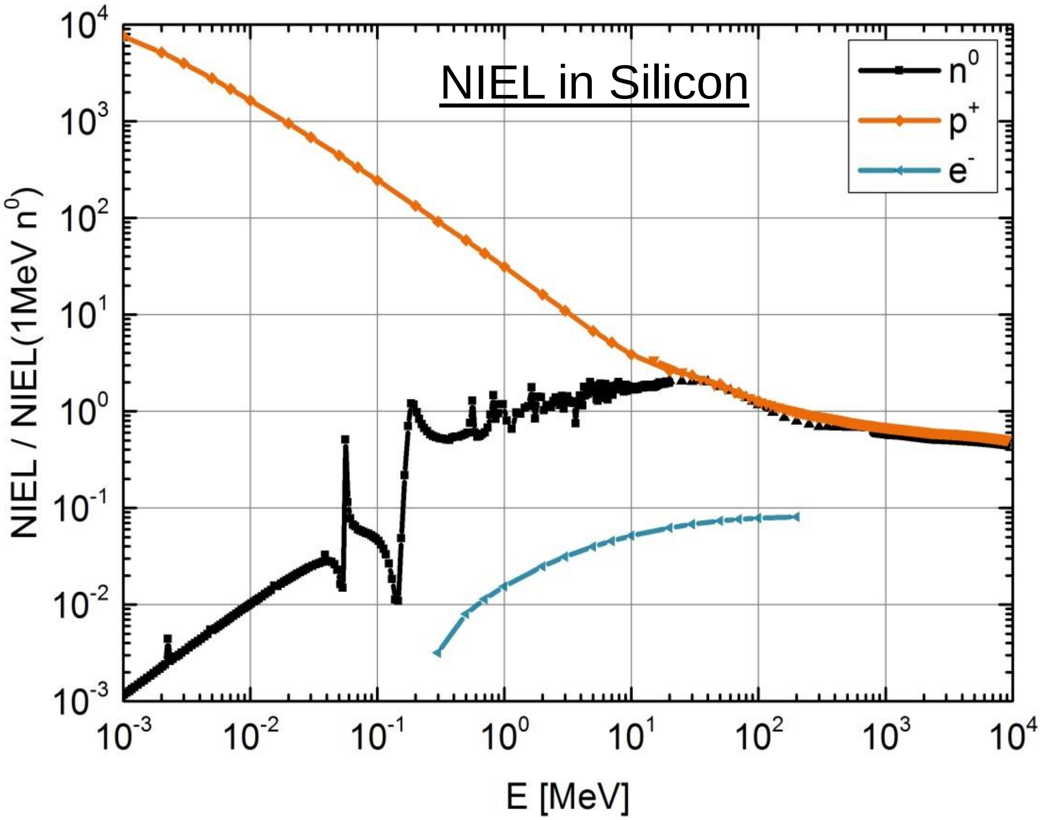
Source: IEEE TNS, Vol 19, p181,1972

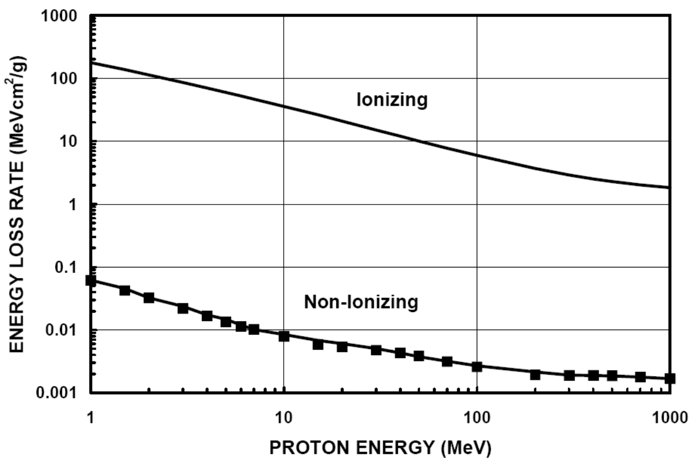
Displacement Damage (TNID) – Basics (II)

- PKA - Primary Knock on Atom
- 50 keV PKA (average recoil energy for PKA produced by 1 MeV neutrons)
- Displacement threshold in Silicon:
  - Single lattice atom (Frenkel pair):
    - $E_d \sim 25$ eV
  - Defect cluster
    - $E_C \sim 5$ keV
- Neutrons (elastic scattering)
  - $E_n > 185$ eV for single displacement
  - $E_n > 35$ keV for cluster
- Electrons
  - $E_e > 255$ keV for single displacement
  - $E_e > 8$ MeV for cluster
- ^{60}Co-gammas
  - Compton Electrons with max. $E\gamma \sim 1$ MeV (no cluster production)

Displacement Damage (TNID) - NIEL

- The non-ionizing energy loss (NIEL) is similar to the energy loss through ionisation
- $D_{neutron}$ (1 MeV)/cm^2 = 95 MeV mb/cm^2





Source: IEEE TNS, Vol. 41, p. 1974, 1994

Displacement Damage (TNID) - NIEL Hypothesis

- The NIEL hypothesis
  - The damage is introduced through stable defect centers
  - The number of defects is proportional to the NIEL
  - The microscopic character of the defects and their concentration is independent from the features of the primary particle
  - The change of basic electrical properties is proportional to the number of defects (Shockley Read Hall Theory)
- So one can test (simulate) of different particles types with different energy spectra with a single energy at a fixed energy

$$NIEL(E_{\mathrm{test}})\Phi(E_{\mathrm{test}}) = \int_{E_1}^{E_2} NIEL(E)\frac{\mathrm{d}\Phi(E)}{\mathrm{d}E}\mathrm{d}E$$

Equivalent 1 MeV neutron fluence

Differential
high energy hadron
spectrum

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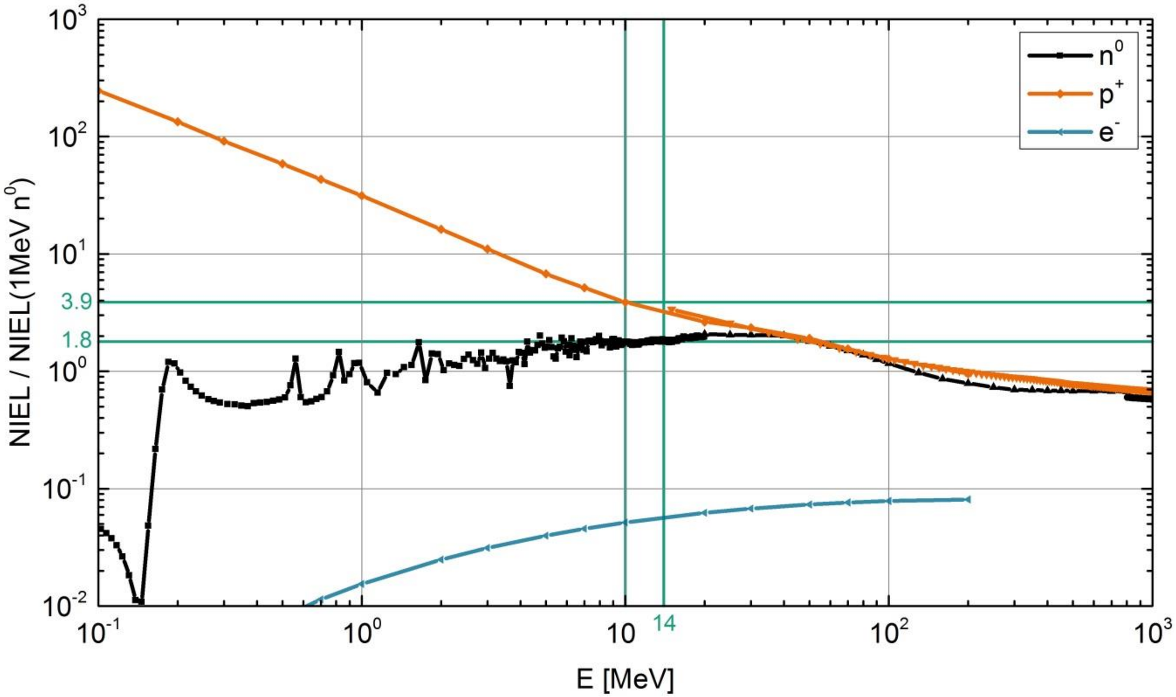
Displacement Damage (TNID) - NIEL Hypothesis - Example

NIEL in Silicon



	NIEL	Φ [cm^{-2}]	NIEL $\cdot$ Φ [cm^{-2}]
p^+(10 MeV)	3.87	$1.00 \cdot 10^{10}$	$3.871 \cdot 10^{10}$
n^0(14 MeV)	1.80	$2.15 \cdot 10^{10}$	$3.871 \cdot 10^{10}$

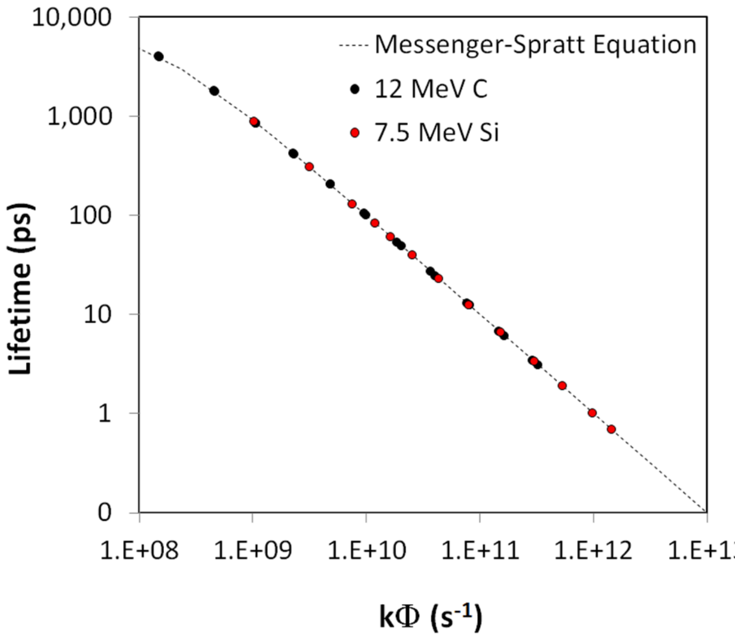
Displacement Damage (TNID) – Manifestation

- Formation of mid-gap states
  - facilitate transitions of electrons from VB to CB
  - increase of leakage current of a reverse-biased pn-junction
  - increase of noise $\propto \sqrt{I}$
  - Increased recombination in non-depleted regions, i.e. charge loss
- Formation of trapping centers (closer to band edge)
  - charge trapping + delayed release
  - loss of charge collection efficiency
- Formation of acceptor and donor-like levels
  - Change in doping characteristics: space-charge (“type”) inversion n $\rightarrow$p
  - change in depletion voltage
  - reverse annealing

Displacement Damage (TNID) - Minority carrier lifetime

- Minority carrier lifetime τ = average time it takes for a minority carrier to recombine
  - In n-type Si holes are minority carriers
  - And in p-type Si electrons
- τ strongly depends on concentration of recombination centers
- Effect of change of minority carrier lifetime
  - Reduces detector sensitivity
  - Reduces amplification of bipolar transistors
  - Reduces charge transfer efficiency (CTE) in CCDs
  - Reduces light output of LEDs
  - Increases threshold current of laser diodes
  - Reduces current transfer ratio (CTR) in opto-couplers

$$\frac{1}{\tau} = \frac{1}{\tau_o} + K\phi$$



Source: SAND2017-2945J

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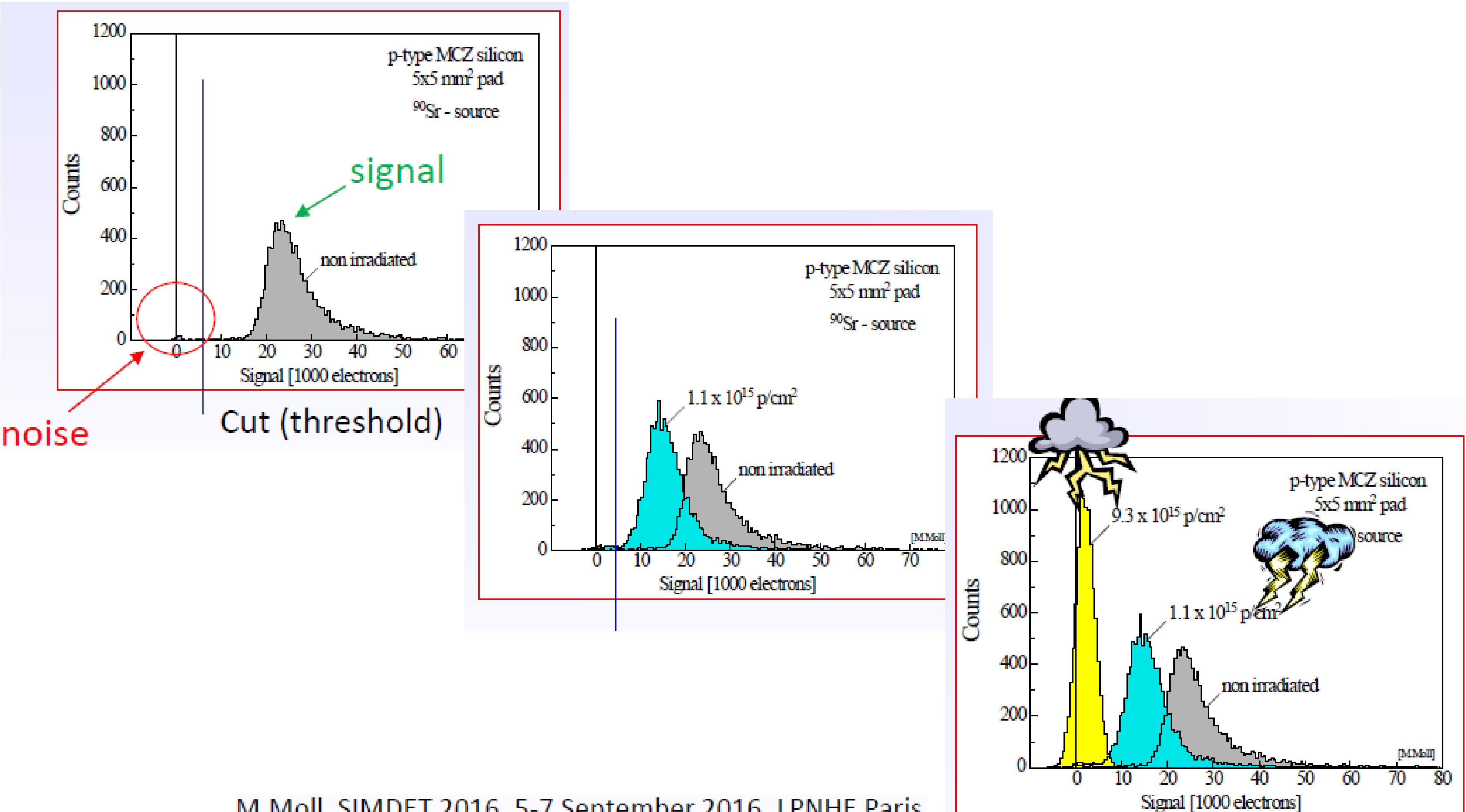
Displacement Damage (TNID) – Charge Trapping



M.Moll, SIMDET 2016, 5-7 September 2016, LPNHE Paris

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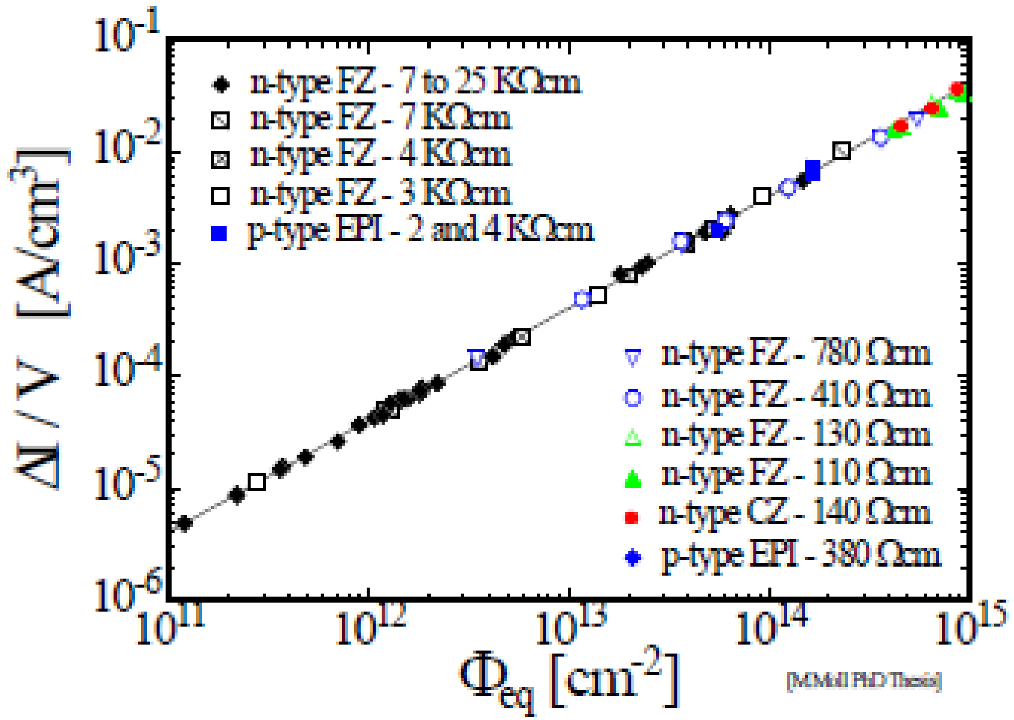
Displacement Damage (TNID) – Leakage Current

- Uniform distribution of active defects
- $I_d = I_0 + \alpha \cdot \Phi \cdot A_d$
- Partial annealing after initial irradiation



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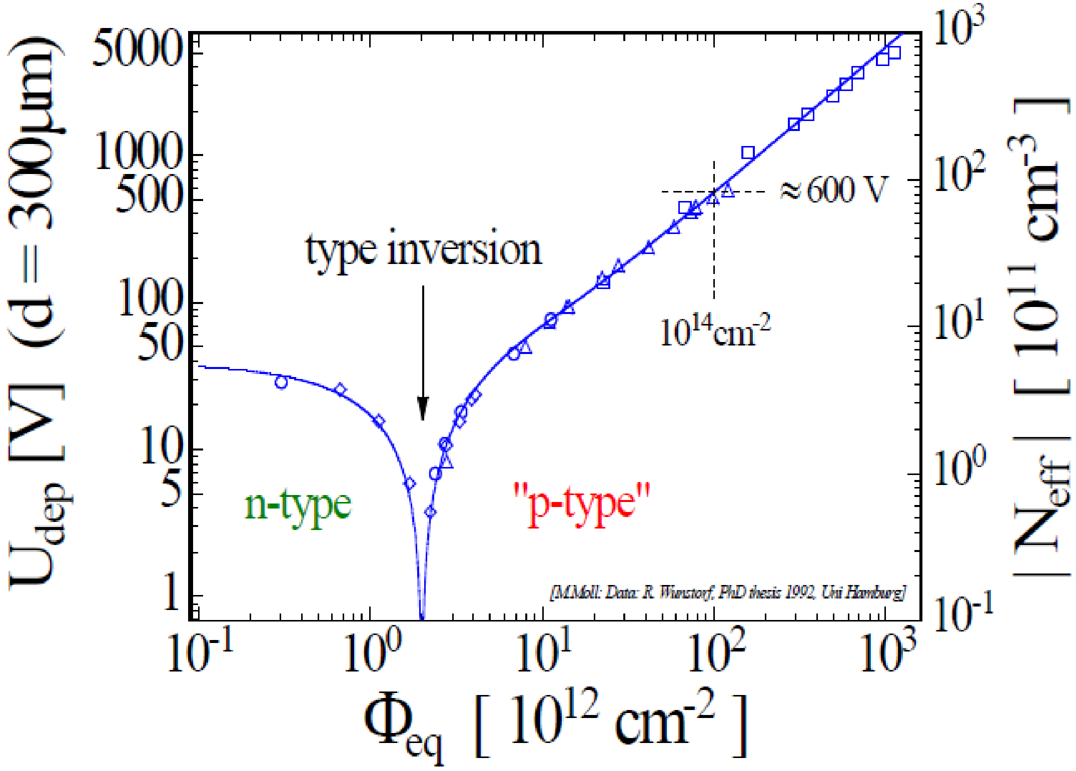
Displacement Damage (TNID) – Depletion Voltage

- Effective doping changes with fluence Φ
    - I. Traps remove donors
    - II. Traps create acceptors

- This can lead to a type inversion, e.g. from n- to p-type

- $U_{dep} \propto |N_{eff}| d^2$



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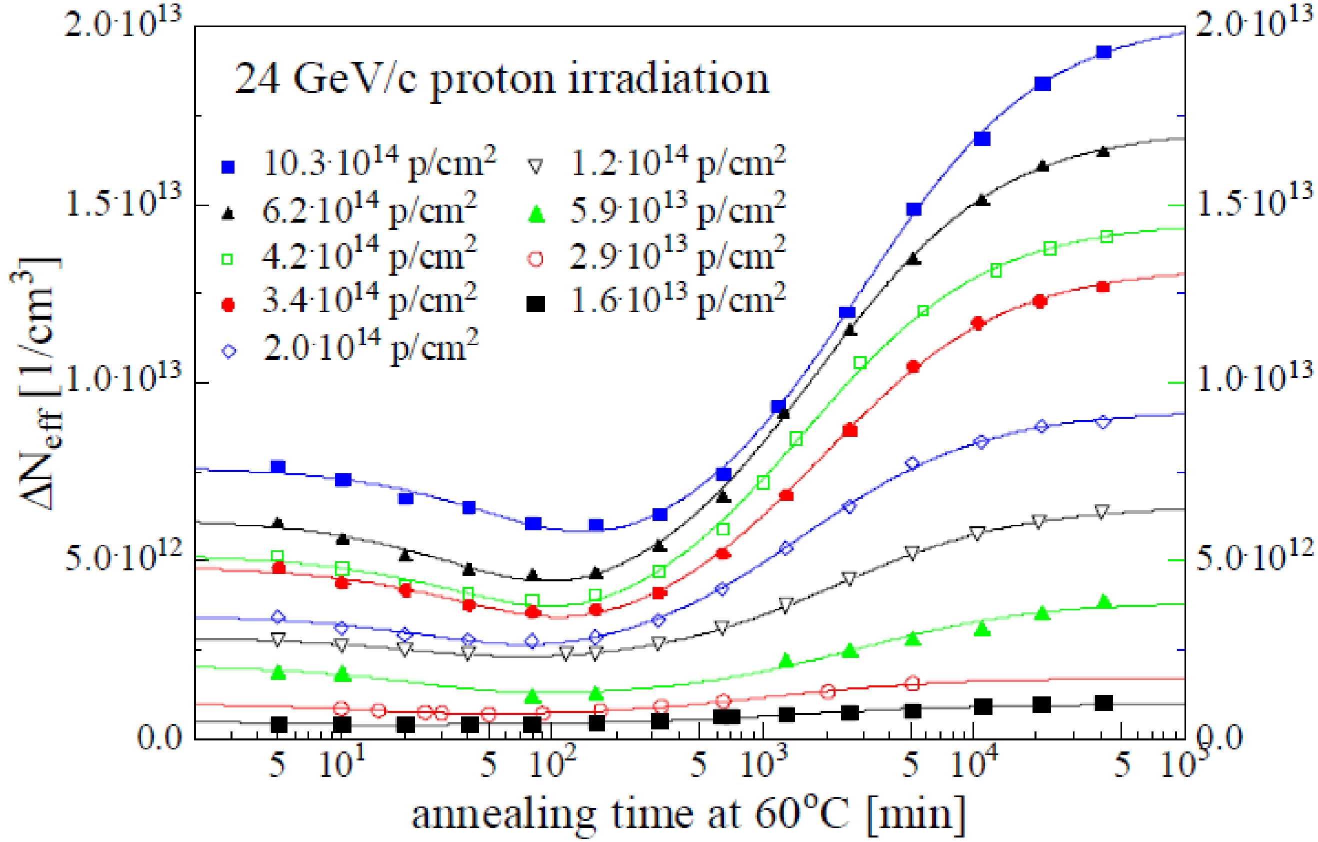
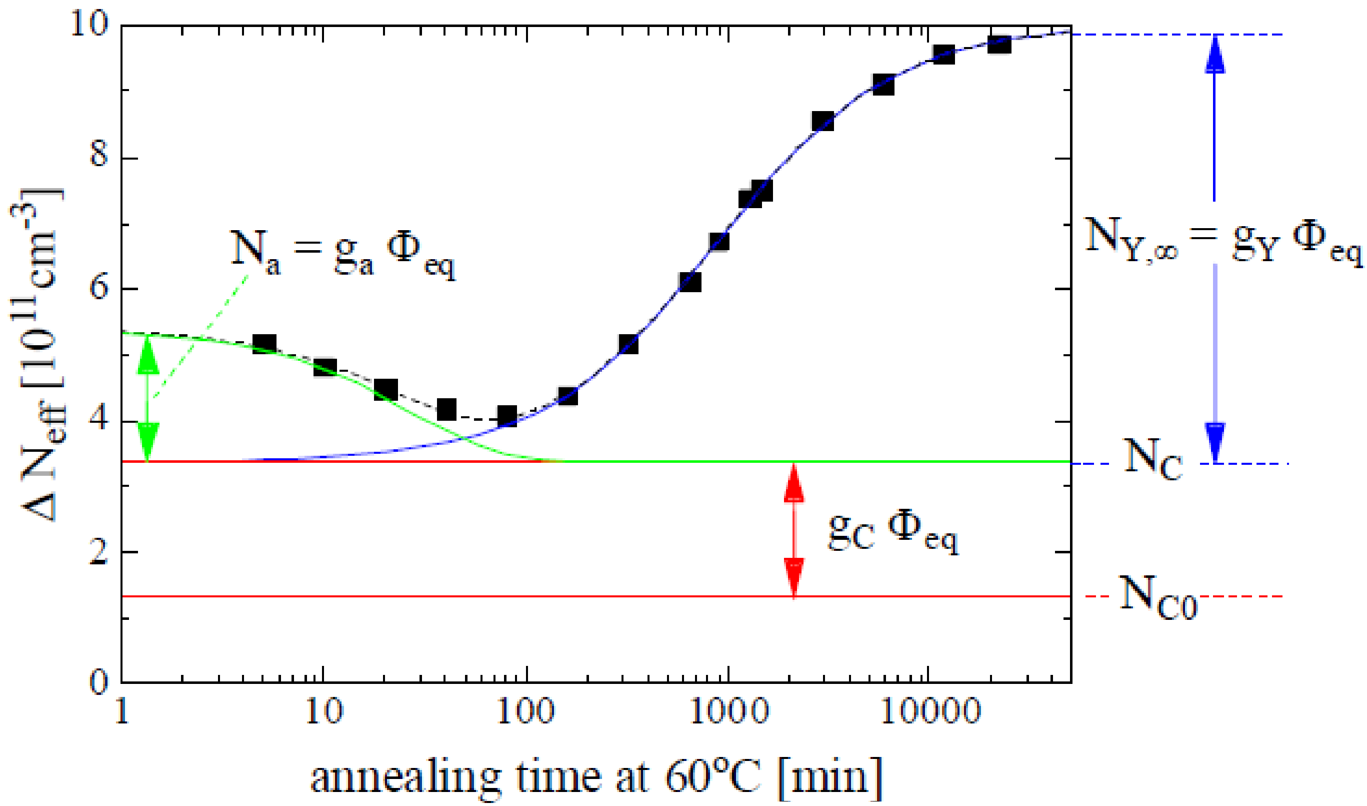
Displacement Damage (TNID) – Annealing

- Instead of depletion voltage better plot the change in the effective space charge ΔN_{eff}



Michael Moll - CERN EP-TA1-SD Seminar - 14.2.2001

Displacement Damage (TNID) – Annealing Behavior



- Hamburg model
- $\Delta N_{eff}(\Phi_{eq},t) = N_a(\Phi_{eq},t) + N_c(\Phi_{eq}) + N_Y(\Phi_{eq},t)$

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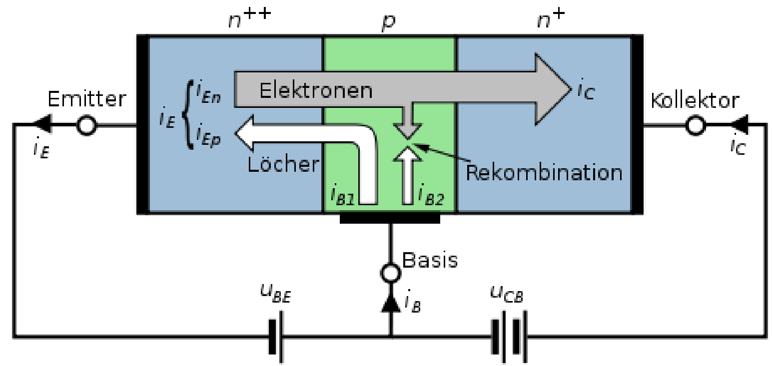
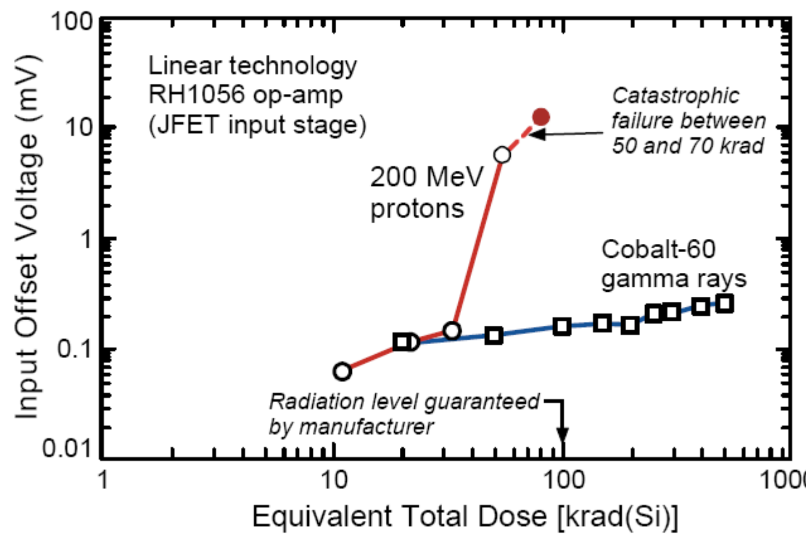
Displacement Damage (TNID) – Annealing Behavior

- $\Delta N_{eff}(\Phi_{eq}, t) = \boldsymbol{N_a(\Phi_{eq}, t)} + \boldsymbol{N_c(\Phi_{eq})} + \boldsymbol{N_\gamma(\Phi_{eq}, t)}$
- **Short term annealing**
  - $N_a = \Phi_{eq} \cdot \sum_i g_{a\,i} \cdot e^{-t/\tau_i}$
  - First order decay of acceptors introduced proportional to Φ_{eq} during irradiation
- **Stable damage**
  - $N_c = N_{c0} \cdot \left(1 - e^{-c \cdot \Phi_{eq}}\right) + g_c \cdot \Phi_{eq}$
  - Incomplete „donor removal“ + introduction of stable acceptors
- **Long term reverse annealing**
  - $N_Y = N_{Y,\infty} \cdot (1 - \frac{1}{1 + t/\tau_Y})$
  - Second order parameterization (with $N_Y = N_{Y,\infty} \cdot \Phi_{eq}$) gives best fit
  - But τ_Y independent of Φ_{eq} => underlying defect reaction based on first order process

Displacement Damage (TNID) - Bipolar Transistors

- Most prominent effect is reduction of bipolar amplification
- In discrete npn-transistors with narrow base TNID effects typically compared to TID effects
- Bipolar transistors can exhibit strong TNID sensitivity due to
  - Lateral pnp-transistors with wide base
  - Depends strongly on external circuitry
  - Relevant for proton fluences > $2 \cdot 10^{11}$ cm^{-2}

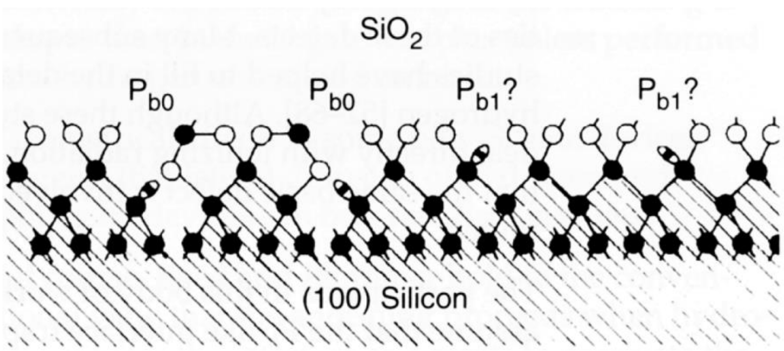


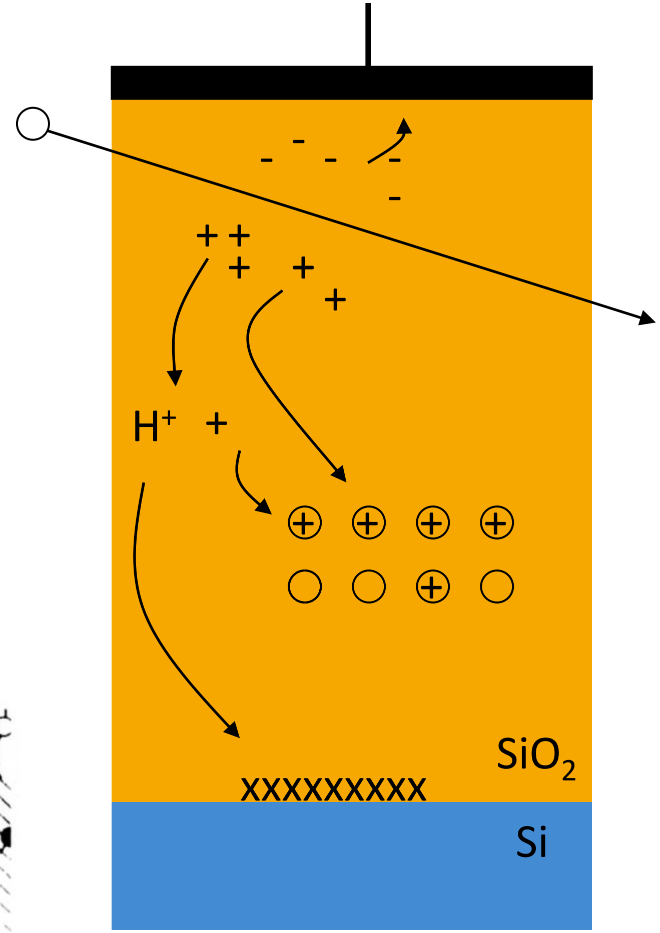


Source: B. G. Rax, *et al.*, IEEE Trans. Nucl. Sci., **45**(2632 (1998).

TID in MOS Devices - Basics

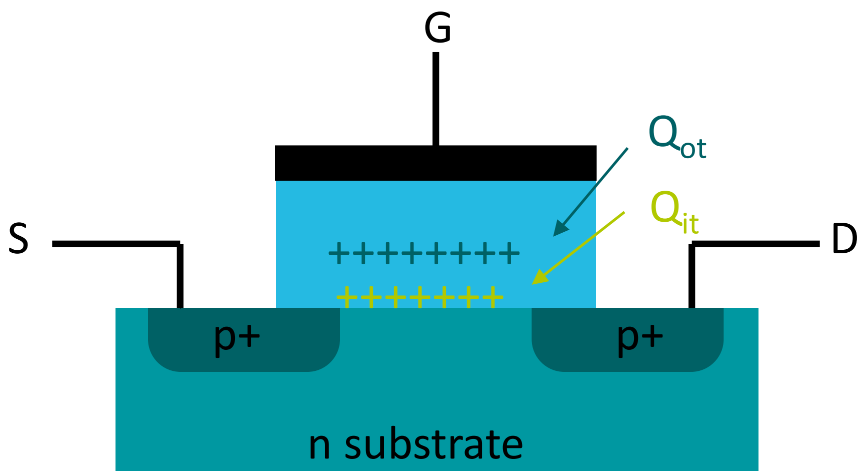
- Ionizing radiation produce electron-hole pairs in SiO_2
- Electrons leave the SiO2 rapidly
- Holes drift much slower and might be captured in oxide traps
- Drifting holes release hydrogen which change Si/SiO2 interface through deposition of interface traps which are
  - positive für pMOS
  - negative for nMOS

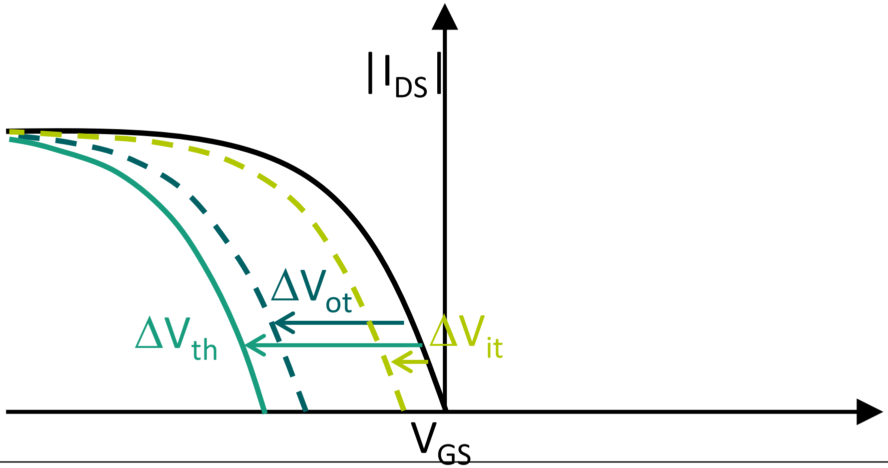




TID in MOS Devices – pMOS (I)

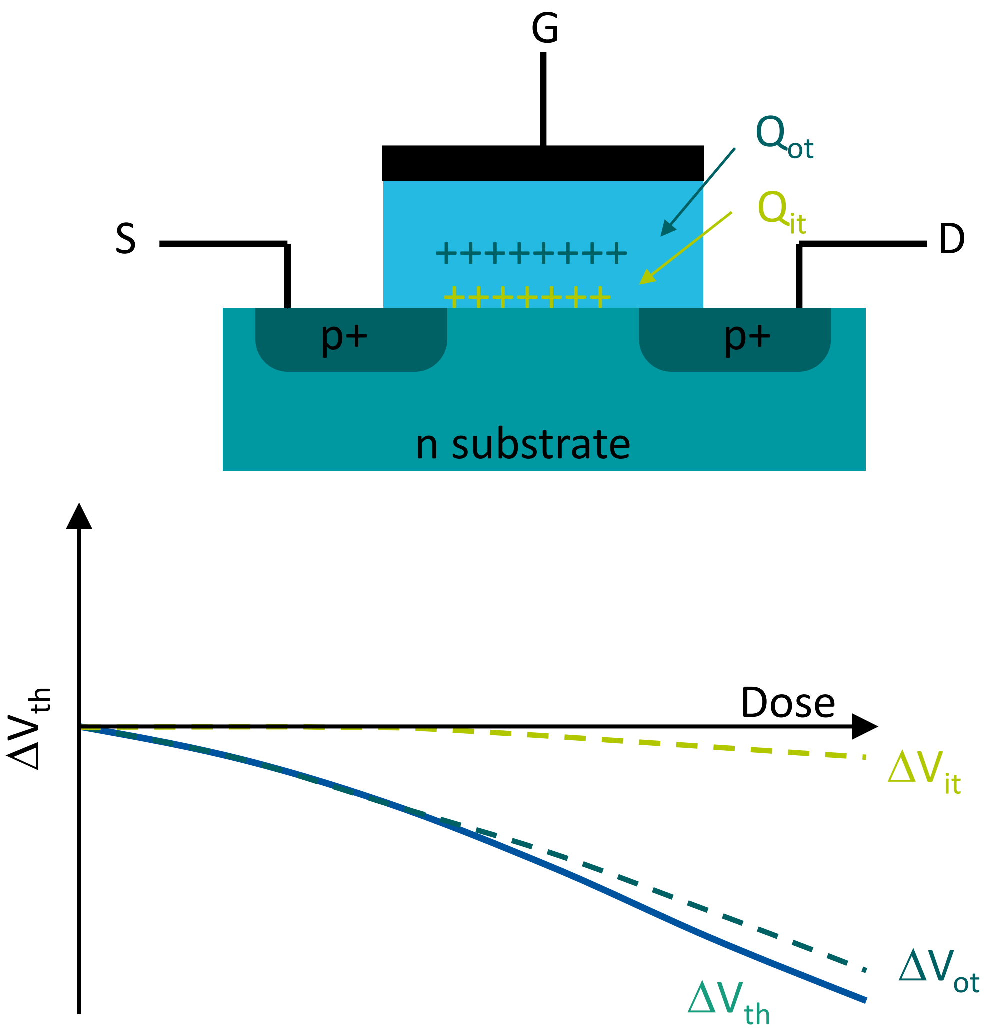
- Fast build-up of positive oxide traps (Q_{ot})
  - Negative threshold voltage shift (ΔV_{ot})
- Delayed build-up of positive interface states (Q_{it})
  - Negative threshold voltage shift (ΔV_{it})
- Always negative threshold voltage shift (ΔV_{th})





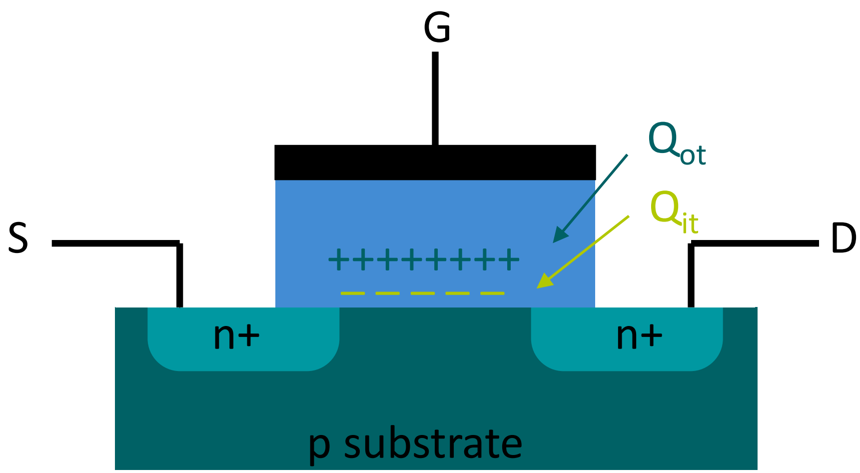
TID in MOS Devices – pMOS (II)

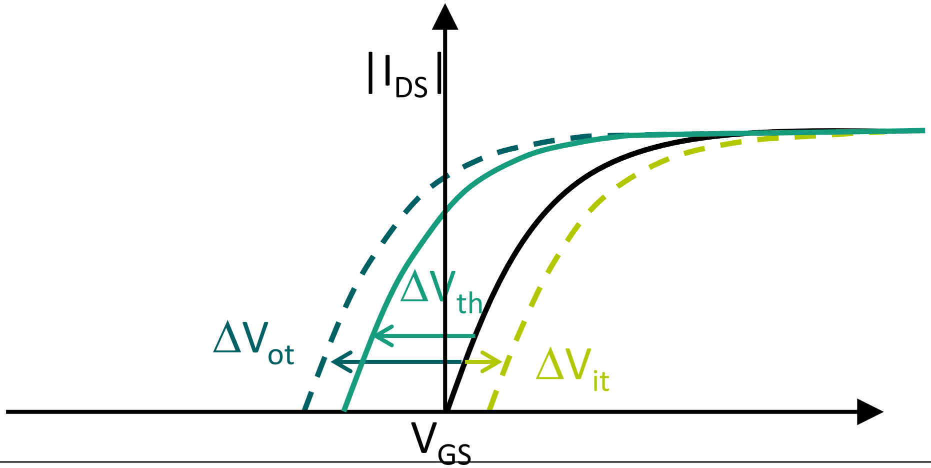
- Fast build-up of positive oxide traps (Q_{ot})
  - Negative threshold voltage shift (ΔV_{ot})
- Delayed build-up of positive interface states (Q_{it})
  - Negative threshold voltage shift (ΔV_{it})
- Always negative threshold voltage shift (ΔV_{th})



TID in MOS Devices – nMOS (I)

- Fast build-up of positive oxide traps (Q_{ot})
  - Negative threshold voltage shift (ΔV_{ot})
- Delayed build-up of negative interface states (Q_{it})
  - Positive threshold voltage shift (ΔV_{it})
- Positive threshold voltage shift (ΔV_{th}) possible depending on dose (i.e. Rebound)





TID in MOS Devices – nMOS (II)

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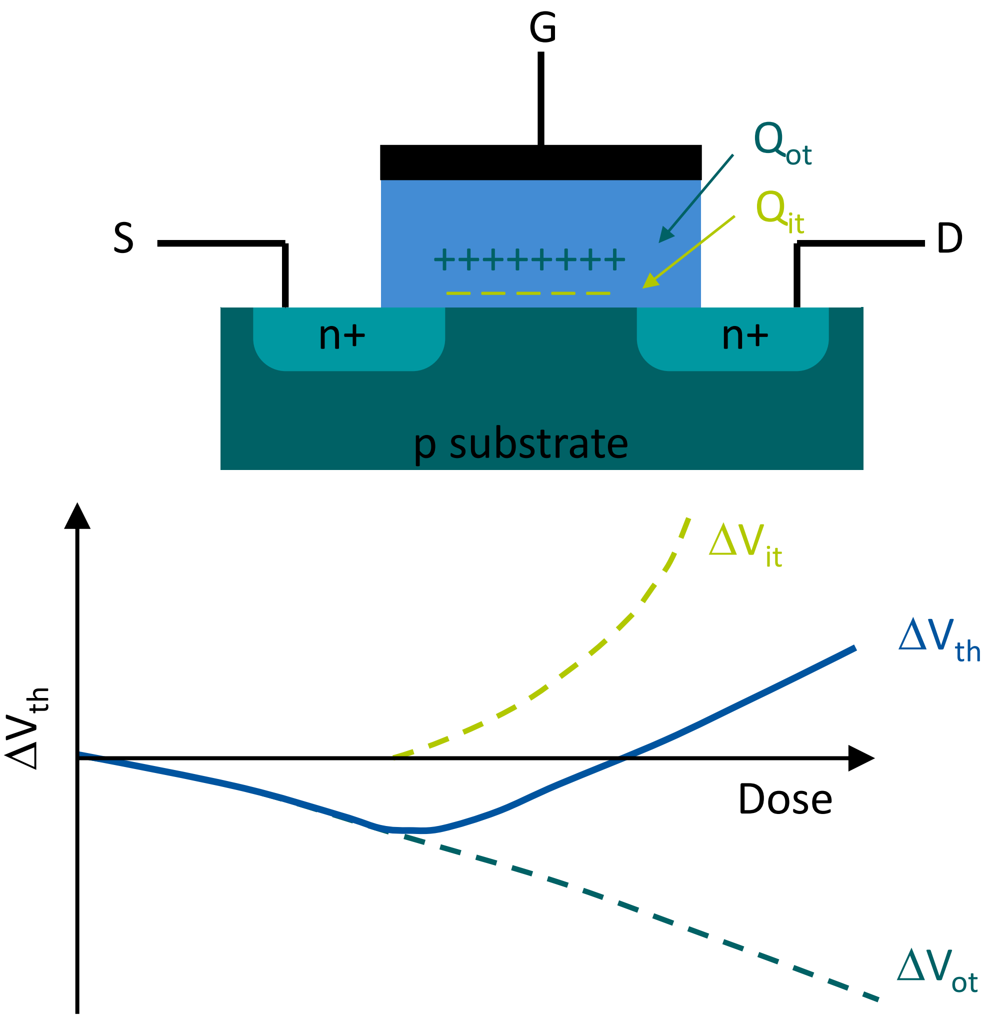
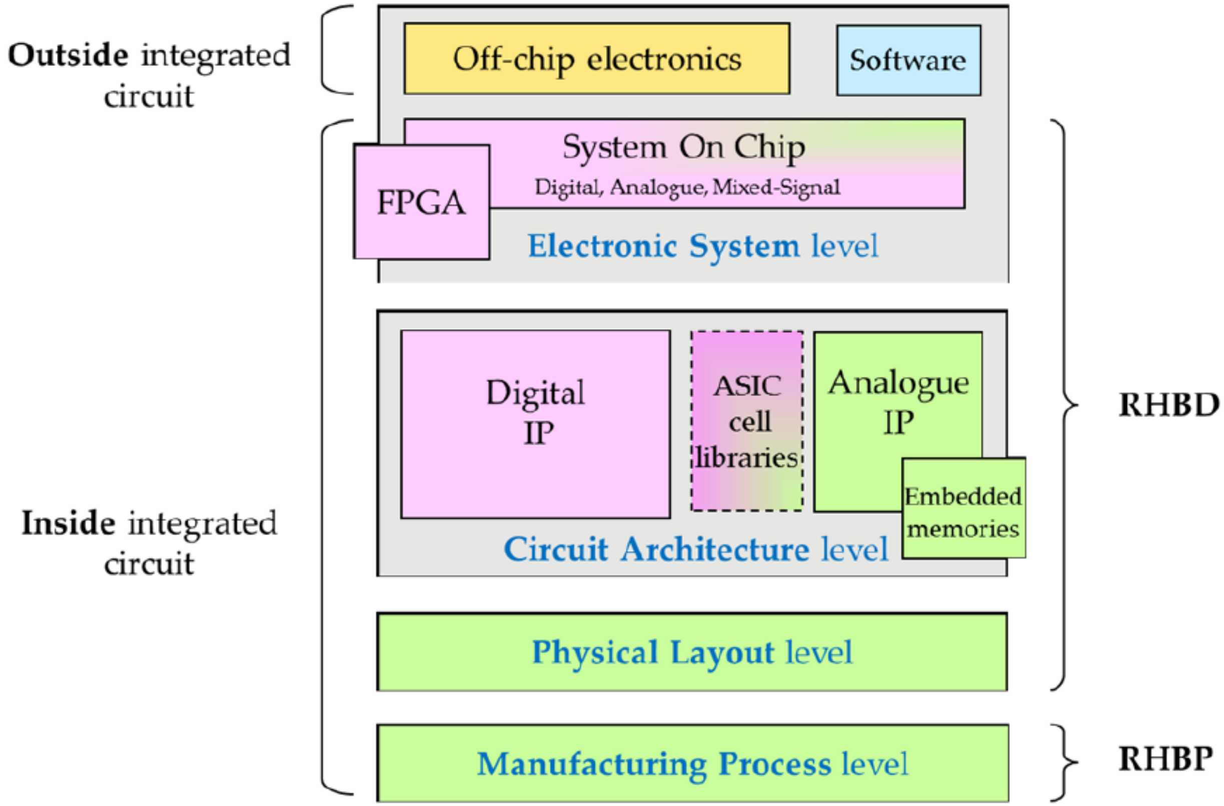


How to make Electronics and Detectors more Radiation Hard? (I)

Strategies:

1. Material engineering
2. Device engineering
3. Change of operational conditions
4. Mitigation



Source: ECSS-Q-HB-60-02A

How to make Electronics and Detectors more Radiation Hard? (II)

Material engineering

- New materials
  - Si-Ge devices
  - Silicon Carbide (SiC), Gallium Nitride (GaN)
  - Diamond
- Defect engineering of Silicon
  - Examples: Oxygen rich Silicon
  - Pre-irradiated Si
  - Needs profound understanding of radiation damage
    - Microscopic defects and macroscopic parameters
    - Dependence on particle type and energy
    - Defect formation kinetics and annealing

How to make Electronics and Detectors more Radiation Hard? (III)

Device engineering

- Thin oxides
- Silicon-on-insulator
- P-type silicon detectors (n-in-p)
- Thin detectors, epitaxial detectors
- 3D detectors and Semi 3D detectors, Stripixels
- Monolithic devices

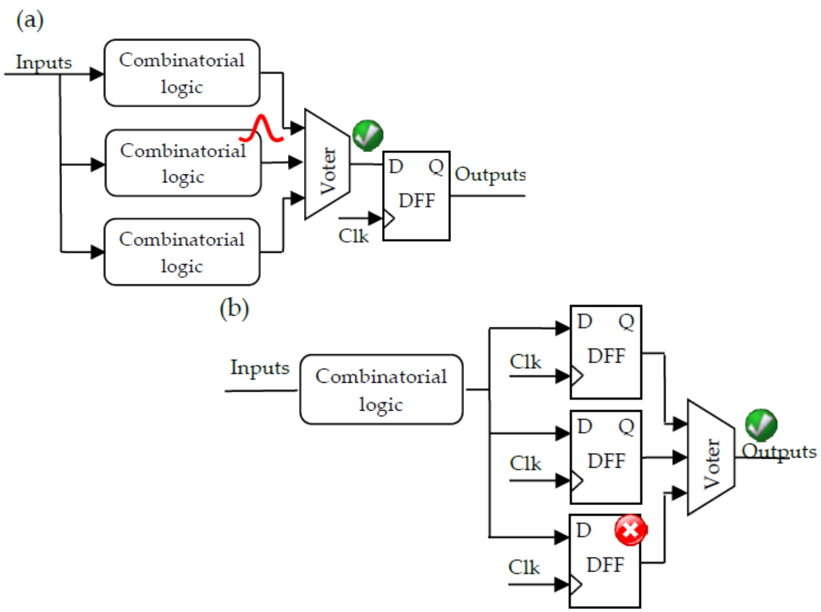
Change of detector operational conditions

- Supply voltages
- Cryogenic temperatures

How to make Electronics and Detectors more Radiation Hard? (IV)

Mitigation

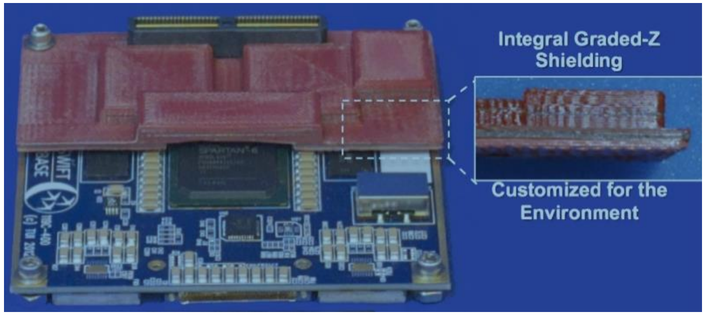
- Redundancy, e.g. Triple-modular redundancy (TMR) plus majority voter
- Error detection and correction (EDAC), e.g. parity bit, Hamming code
- Watchdogs
- Scrubbing
- Temporal annealing
- Local spot shielding



Source: ECSS-Q-HB-60-02A

But be careful when implementing TMR or other mitigation techniques into FPGAs.

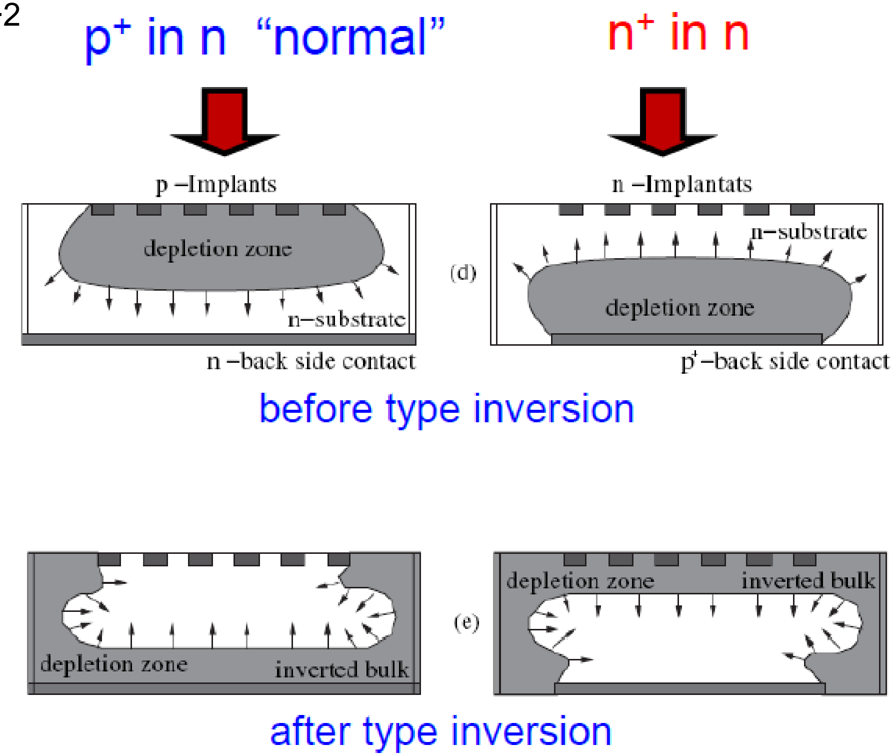
- Decreases available number of gates
- Can slow down system
- Incorrect implementation can increase errors



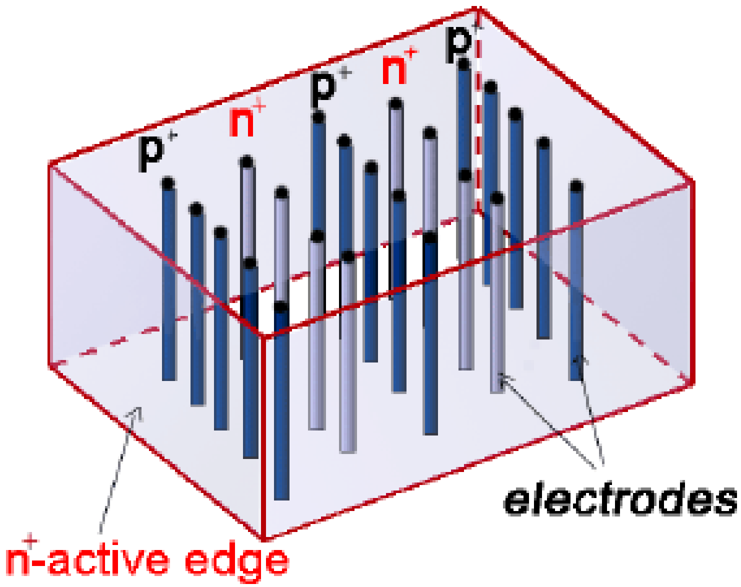
Source: Tethers Unlimited Inc.

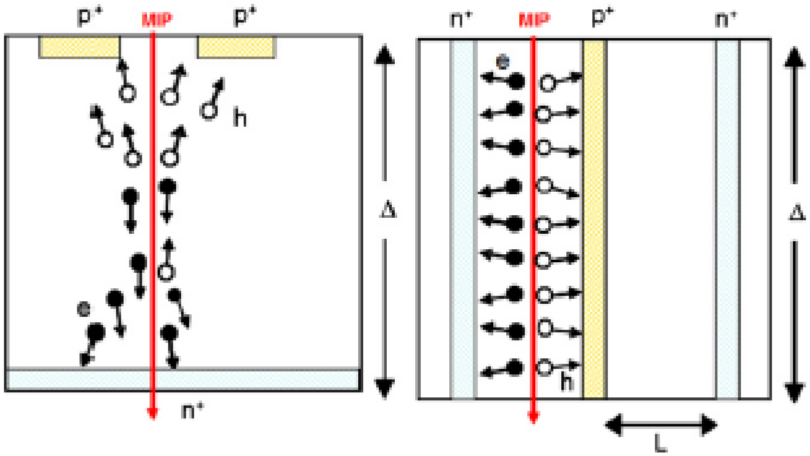
LHC Pixel Sensors

- Fluences of up to 10^{14} $cm^{-2}yr^{-1}$for innermost detectors
- Type inversion occurs at $\sim 2-3 \cdot 10^{12} cm^{-2}$
  - n-bulk effectively becomes p-bulk
  - depletion voltage first decreases, then increases with increasing fluence
  - pn interface (diode) migrates from p+n side to n+p side after type inversion
- Mitigation: n+ in n-type
  - Bias from backside
  - Guard rings
  - Insulation of n+ in n pixels with p-spray
  - operation possible also without full depletion



3D Silicon Sensors



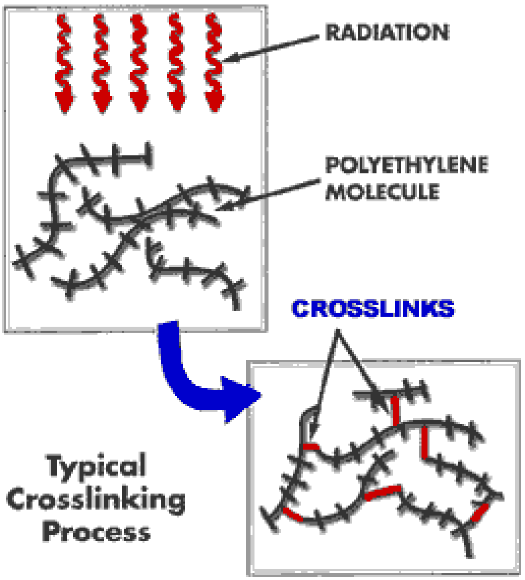


[S. Parker et al., ICFA Instr. Bull. 14, 30 (1997), C. Da Via et al., NIM A 694, 321 (2012), NIM A 765, 151 (2014)]

- 3D array of p+ and n+ electrodes
- particle path (signal) different from drift path
- short drift path, fast charge collection
- depletion (sideward) at low voltages, high field
- radiation tolerant: 50% charge @ 10^{16} cm^{-2}
- good for inclined tracks
- slightly larger C (noise)
- now also in diamond, CdTe

Radiation Effects in Polymers

- Radiolysis due to Ionization
- Breaking of Bonds
- Depending on Chemical Structure
  - Aromatics harder than Aliphates
- Possibly re-arrangement to other/new molecules
  - Material gets harder, more brittle or fluid
- Small molecules are evaporated
  - Change of volume
- Intensity of effects depend on ambient atmosphere especially Oxygen
- Rad-hard polymers
  - Kapton® (Polyimide),
  - PEEK® (Polyetheretherketon) (stable > 1 Grad)

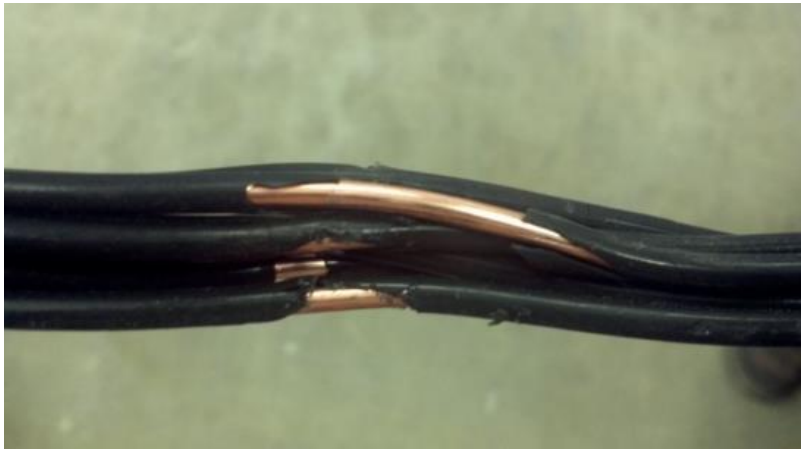


Source: http://www.orthoassociates.com/SP11B16/Crosslink.gif

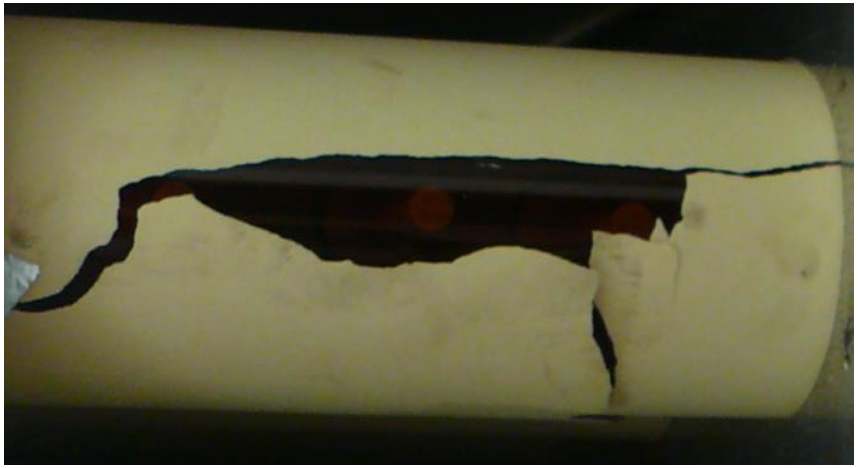
Quelle: Beta Gamma Service

Radiation Effects in Materials

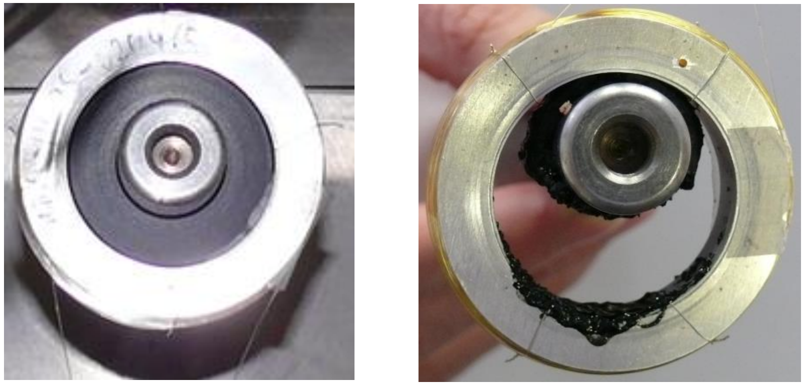
Teflon



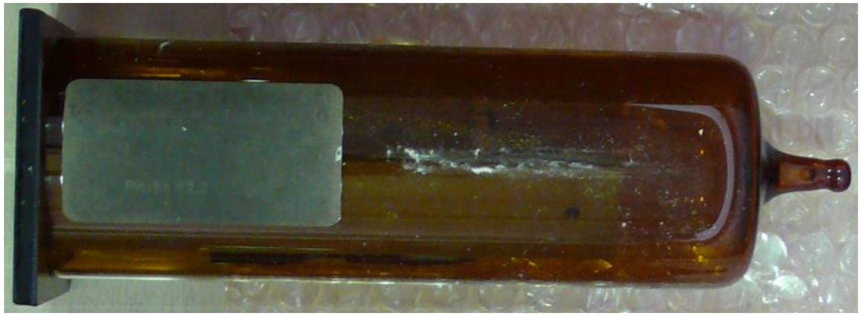
Paper



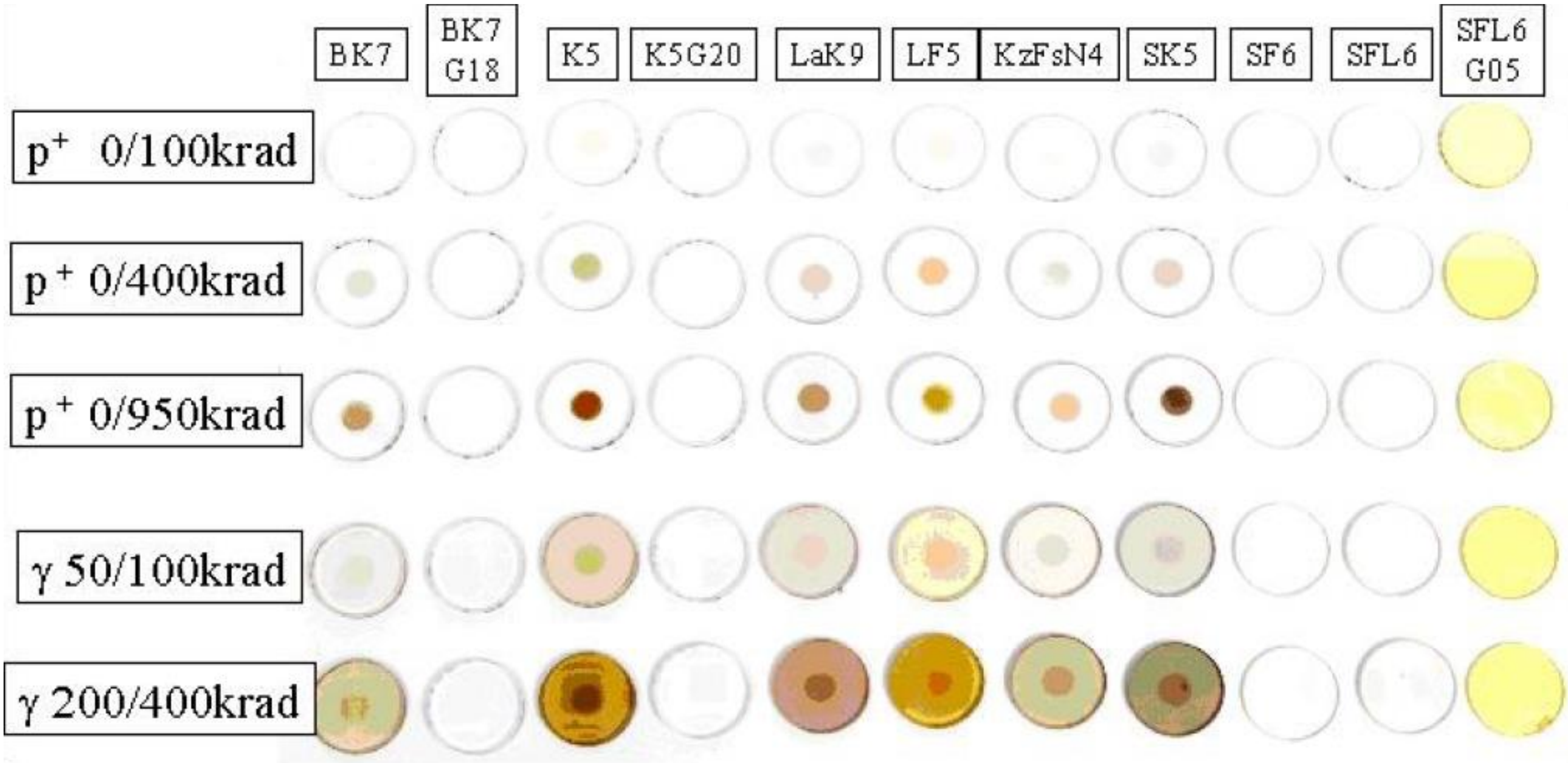
Delrin



Glass pipe



Radiation Effects in Different Glases



Fruit et al., Proc. of SPIE Vol. 4823 p. 132

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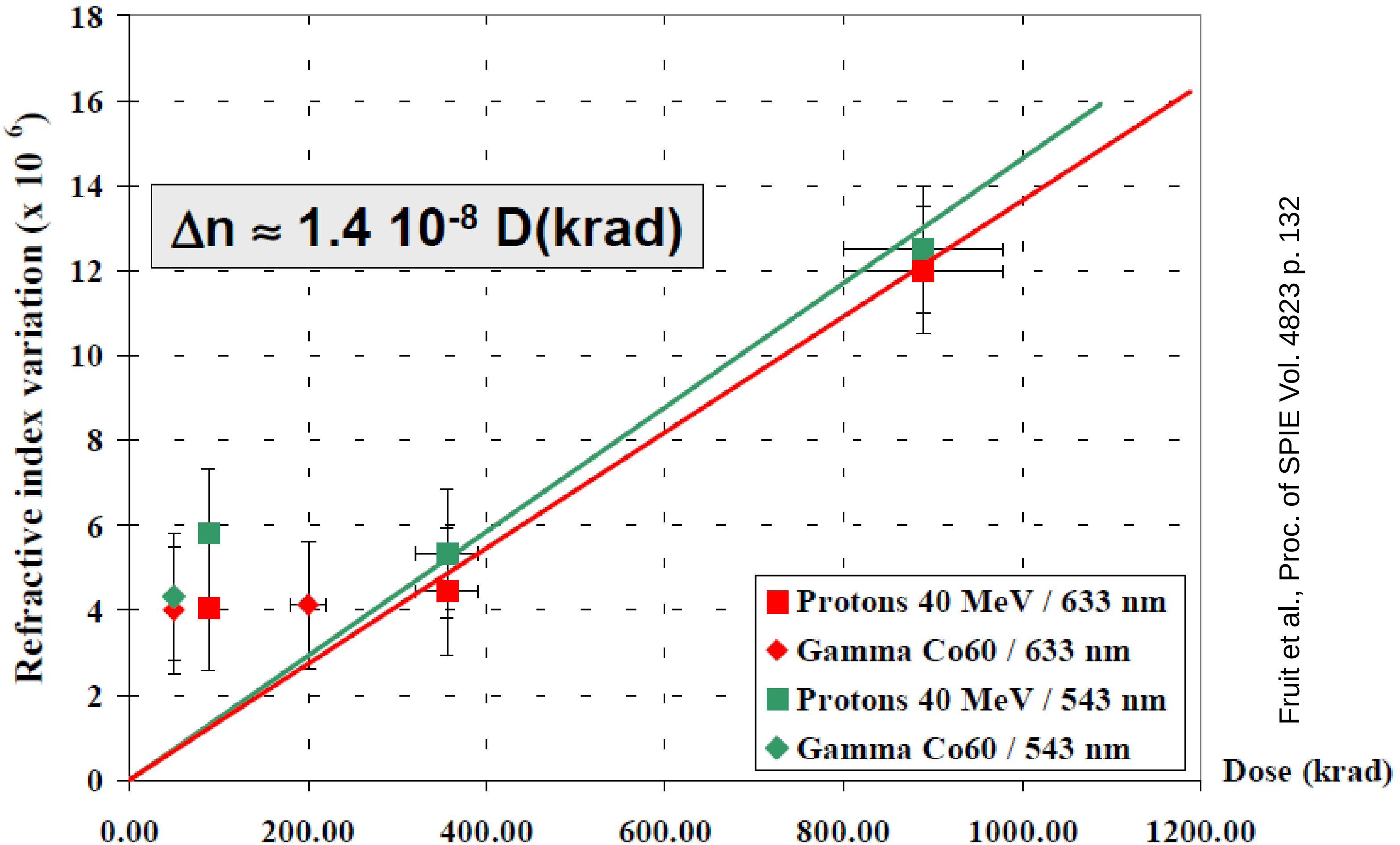
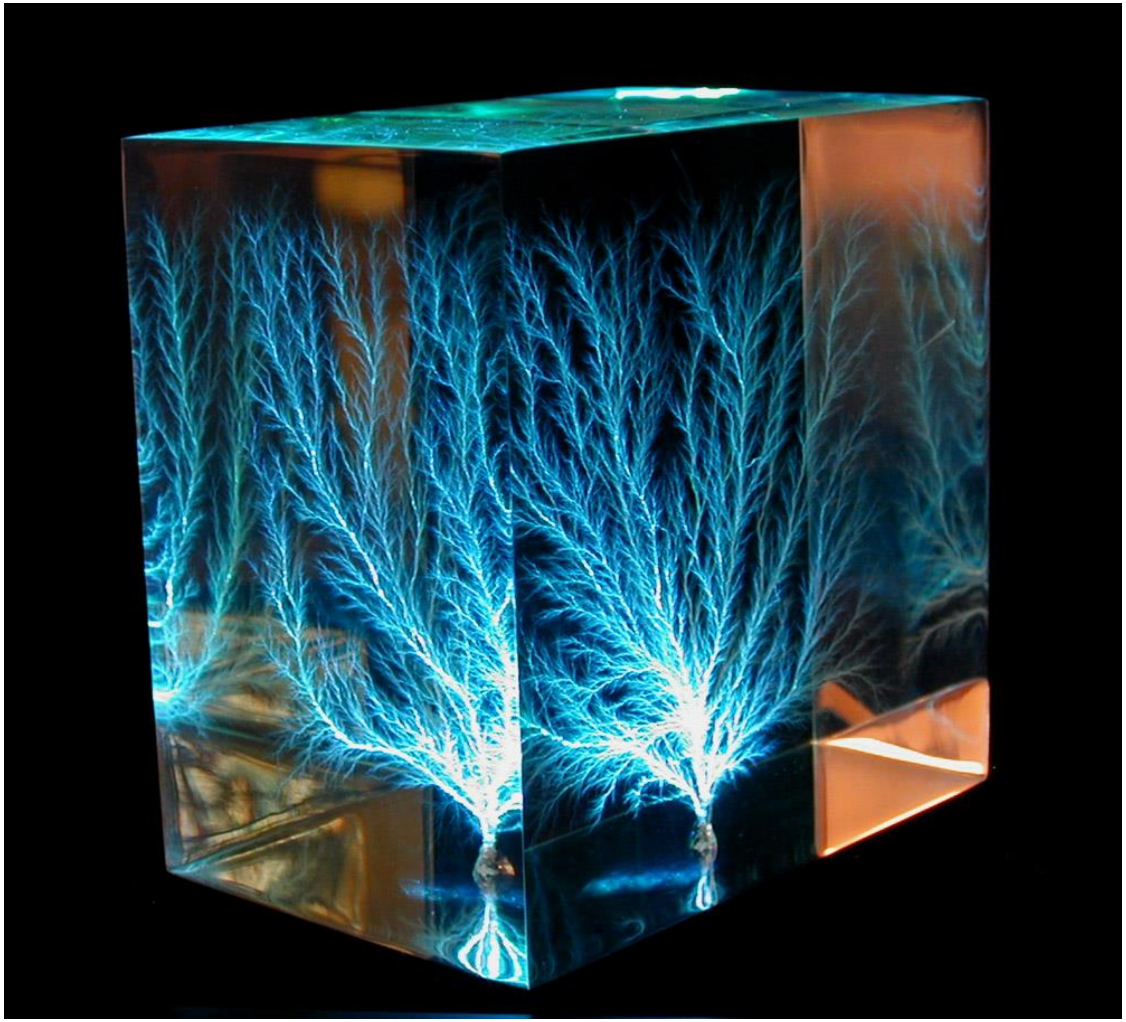
Glas - Change of Refractive Index



Fruit et al., Proc. of SPIE Vol. 4823 p. 132

Electro-Static Discharge (ESD) in Insulators

- ESD) in acrylic-glass.
- Lichtenberg-Figure



Source: Wikipedia

Thank you for your attention.