TCP/IP in hardware

- using SME

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Background and Motivation

Dedicated hardware needs to transmit data in real time, but OS network stacks are usually not enough!
Dedicated Network cards are not perfect either:

Weaknesses of network cards

- Only basic programmability
- Incompatible APIs
- Licensed VHDL code blobs
- Seldom swap-able
- **Price!**

Figure: An Intel FPGA NIC

A performant, efficient, and flexible network stack in FPGA!

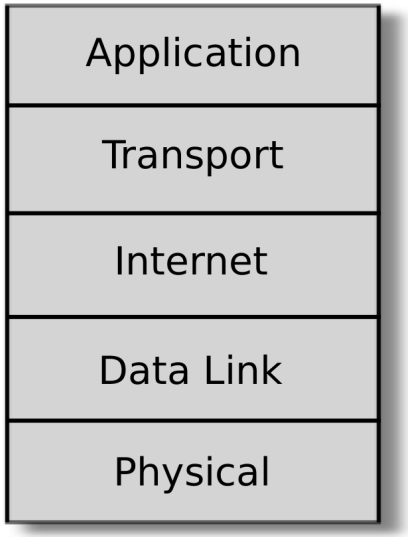
How? Using SME!

- Easy & intuitive hardware modelling
- Implicit clock
- Built-in simulation utilities
- VHDL code generation
- Verification by comparing VHDL signals with C# simulation

SME and FPGA

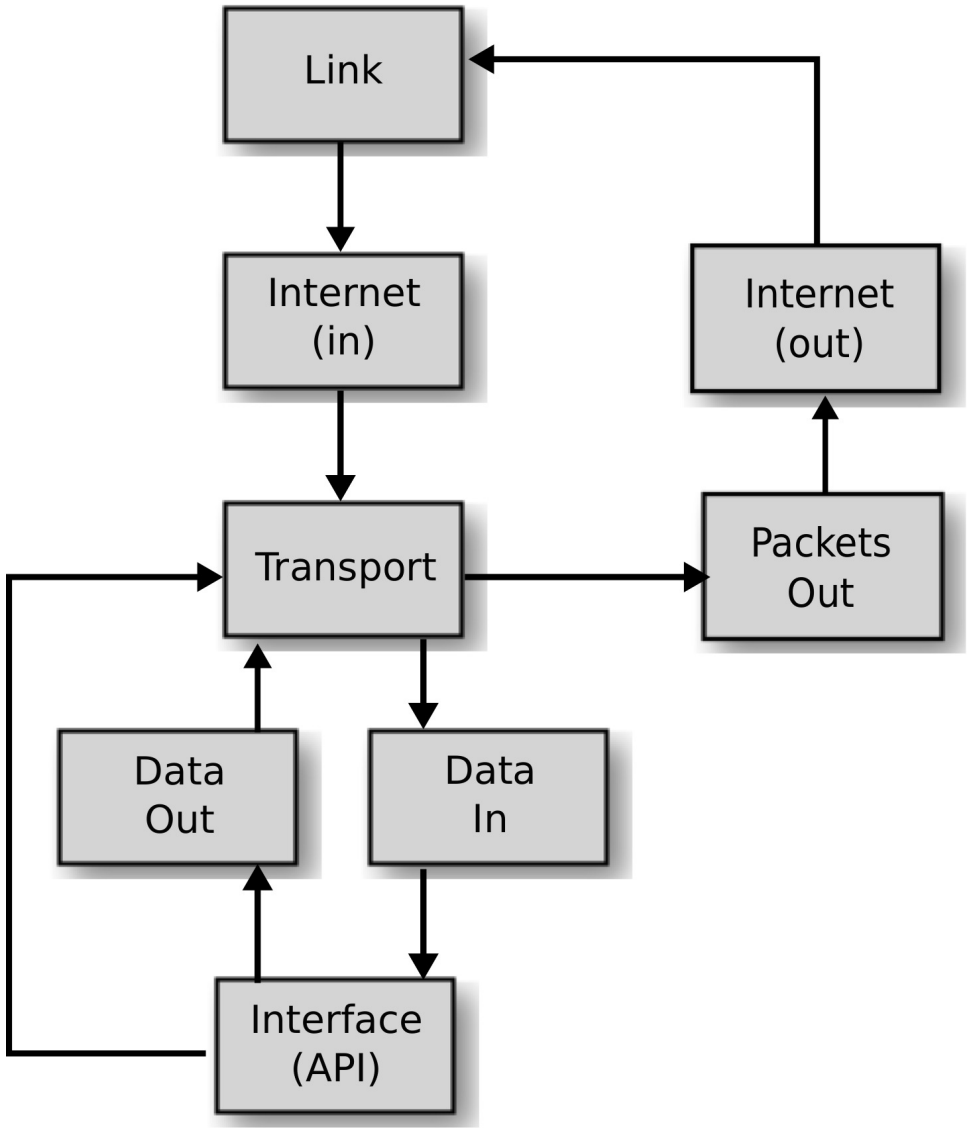
Skip this if SME has been covered

Internet Protocol Suite (TCP/IP)



Some text

Architecture



Challenges

- Clock-delays
- Data de-multiplexing
- Limited (fast) memory
- Information sharing is by design hard in SME
- Very limited programming utilities

Questions

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