TCP/IP in hardware
Using SME

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May 21, 2019

Background and Motivation

Dedicated hardware needs to transmit data in real time, but native network stacks are usually not enough!
Dedicated Network cards are not perfect either:

Weaknesses of network cards

- Only basic programmability
- Incompatible APIs
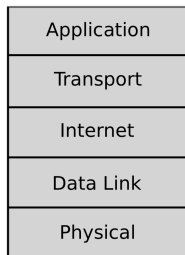- Licensed VHDL code blobs
- Seldom swap-able

A performant, efficient, and flexible network stack in FPGA!

How? Using SME!

- Easier hardware modelling
- Implicit clock
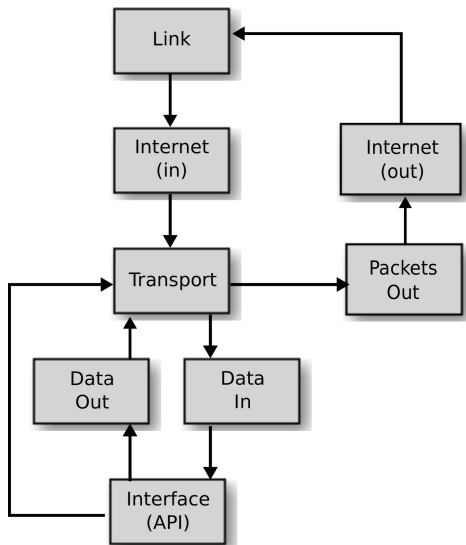- Built-in simulation utilities
- VHDL code generation

SME and FPGA

Internet Protocol Suite

Application
Transport
Internet
Data Link
Physical

Some text

Architecture

Challenges

- Clock-delays
- Data de-multiplexing
- Limited (fast) memory
- Information sharing is by design hard in SME
- Very limited programming utilities

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