

TCP/IP in hardware using SME

Mark Jan Jacobi & Jan Meznik

KU

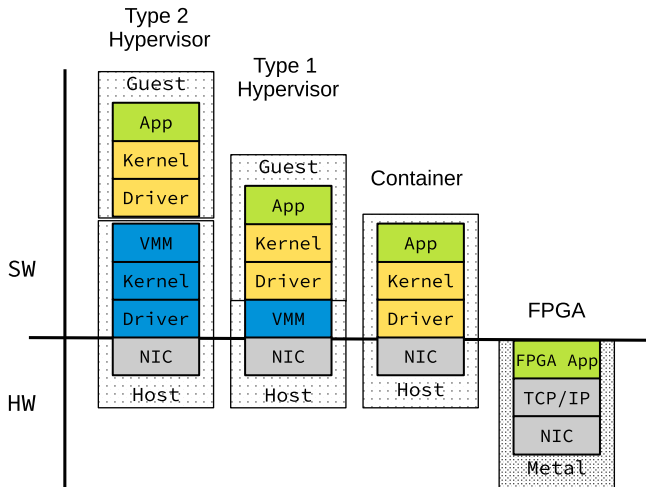
September 11, 2019

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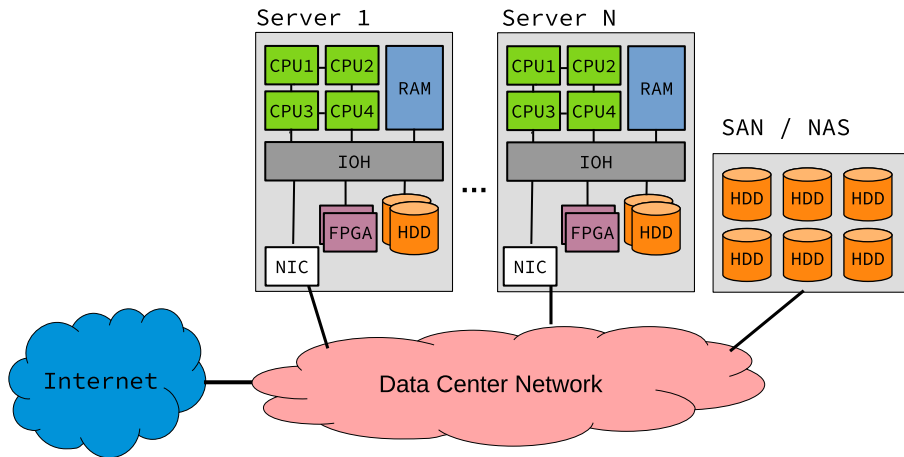
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Background and Motivation

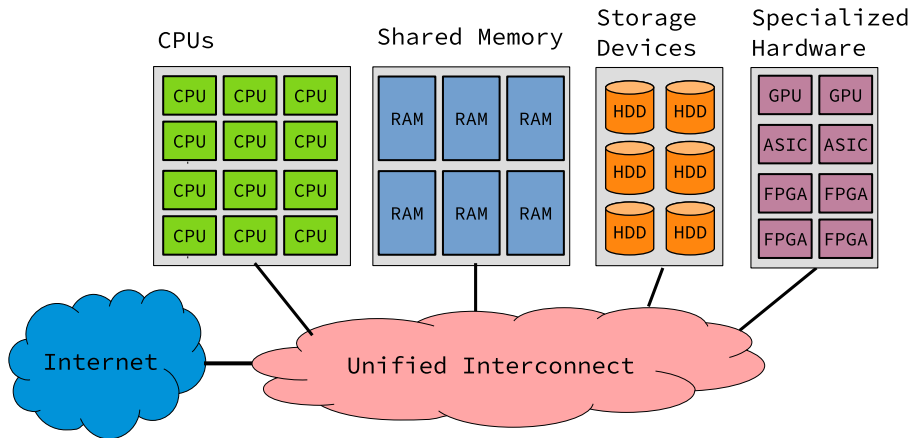
FPGAs are making their way into data centers to boost the computing power and the overall power efficiency.



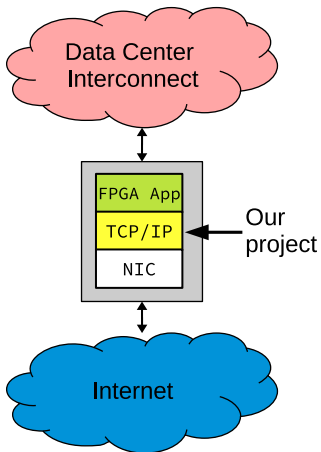
A conventional data center architecture



Proposed, disaggregated data center architecture



FPGA usage



The Internet What is the internet, and how does it work??!?

TCP/IP 4 layers

Communication example between 2 hosts

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- 1 Introduction
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- Processes
 - State machines
- Buffers
 - Memory segments
 - Dictionary
- Interface signal control
 - Buffer-Producer
 - Compute-Producer
- Interface control
 - Usage
 - Limitations

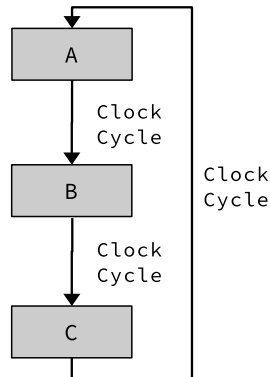
Implementation

Processes

State machines

```
1 public class SomeProcess :  
2   ↳ StateProcess  
3 {  
4     private override async  
5     ↳ Task OnTickAsync()  
6     {  
7       a();  
8       await ClockAsync();  
9       b();  
10      await ClockAsync();  
11      c();  
12      await ClockAsync();  
13    }  
14  }
```

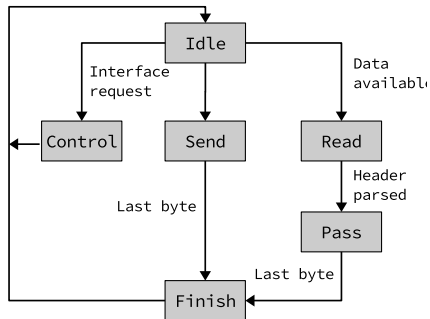
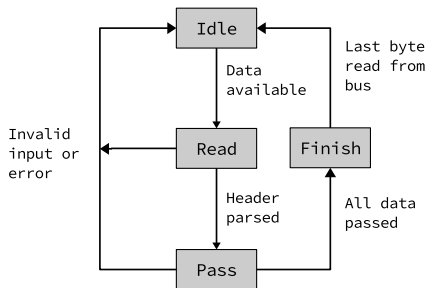
```
1 public class SomeProcess :  
2   ↳ SimpleProcess  
3 {  
4   // Initial state  
5   state = A;  
6  
7   protected override void  
8   ↳ OnTick()  
9   {  
10    switch(state) {  
11      case A:  
12        a();  
13        state = B;  
14      case B:  
15        b();  
16        state = C;  
17      case C:  
18        c();  
19        state = A;  
20    }  
21  }
```



Implementation

Processes

Examples



Buffers

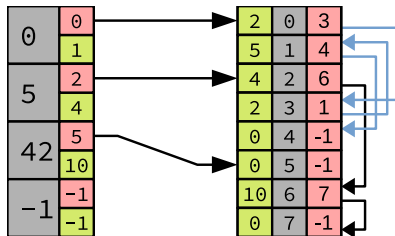
The diagram illustrates the mapping between a Segment Lookup Table and Memory. The table has five entries, each with a 'Start' and 'End' address. The memory is a linear sequence of 16 slots, indexed 0 to 15. Arrows show the mapping: Table entry 0 maps to memory slots 4 and 1; entry 1 maps to slots 0 and 2; entry 2 maps to slots 0 and 5; entry 3 maps to slots 1 and 6; entry 4 maps to slots 1 and 8. A separate block contains 'Table Head', 'Table Tail', 'Mem Head', and 'Mem Tail'. Arrows show 'Table Head' pointing to memory slot 12, 'Table Tail' pointing to slot 13, 'Mem Head' pointing to slot 14, and 'Mem Tail' pointing to slot 15.

Segment Lookup Table		Memory
0	Start	0
	End	1
1	Start	2
	End	3
2	Start	4
	End	5
3	Start	6
	End	7
4	Start	8
	End	9
		10
		11
		12
		13
		14
		15

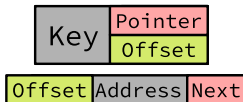
Implementation

Buffers

Memory dictionary



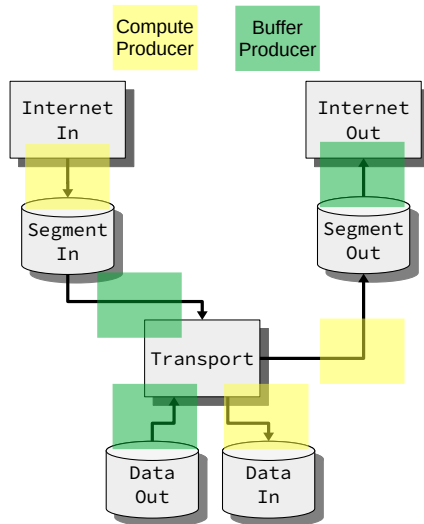
Value Legend



Implementation

Interface signal protocol

Identifying the scenarios

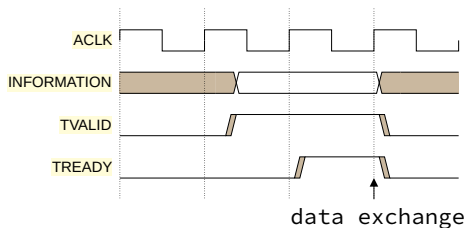


Implementation

Interface signal protocol

Inspired by AXI4

- Single clock offset when sending data.
- Indicate end of stream with `bytes_left`.

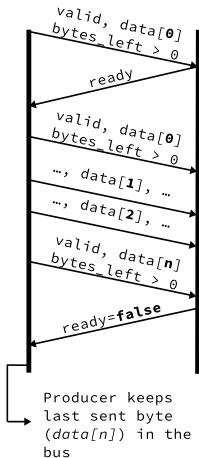


Implementation

Interface signal protocol

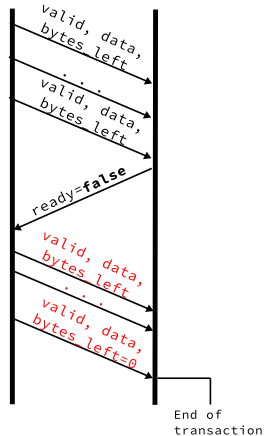
Buffer-Producer (BP)

Producer Consumer



Compute-Producer (CP)

Producer Consumer



Implementation

Interface protocol

The interface structures

```
1  enum InterfaceFunction : byte
2  {
3      INVALID = 0,
4      // BIND = 1,
5      LISTEN = 2,
6      CONNECT = 3,
7      ACCEPT = 4,
8      CLOSE = 7,
9      // ...
10     OPEN = 255,
11 }
12
13 struct InterfaceData
14 {
15     public int socket;
16     public uint ip;
17     public byte protocol;
18     public ushort port;
19 }
```

```
1  interface InterfaceBus : IBus
2  {
3      bool valid;
4      byte interface_function;
5      InterfaceData request;
6  }
7
8  interface InterfaceControlBus : IBus
9  {
10     bool valid;
11
12     byte exit_status;
13     byte interface_function;
14     InterfaceData request;
15     InterfaceData response;
16 }
```

Implementation

Interface protocol

Limitations

- One request at a time.
- Arbitrary delay between request and response.

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- Setup
 - Graph file simulator
- Test
- Validation
 - Latency
 - Outgoing packet validation
 - Internet Protocol Suite compliancy as per RFC 1122

Graph file simulation

- Full input - output
- Does not take latency between packets into account
- Simplifies test cases

Evaluation

Setup

Graph simulation node types



Data In



Data Out



Send



Receive



Command



Wait

State and Color

Description

Waiting

Vertex is not in use.

Ready

Vertex is ready
for activation.

Active

Vertex is active.
Simulator is
gathering data.

Inactive

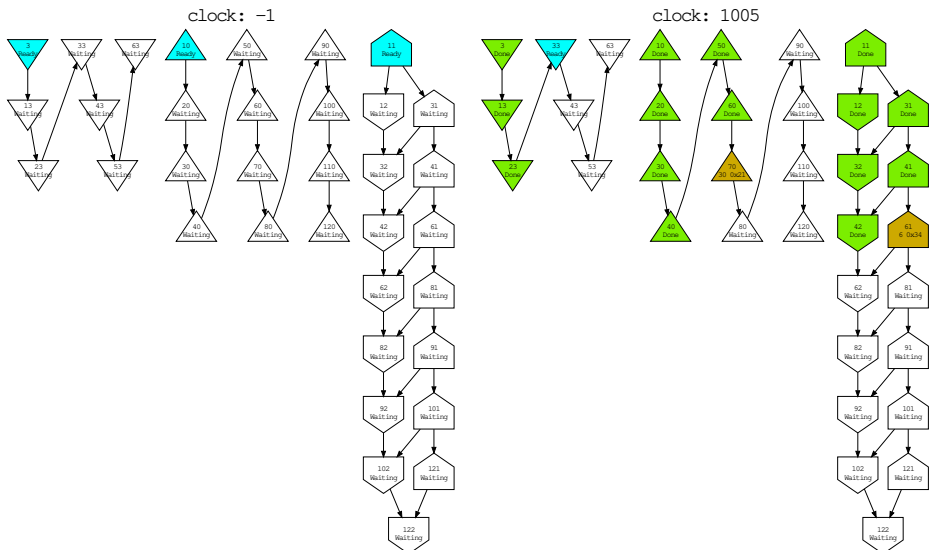
Vertex is inactive.
Simulator is not
gathering data.

Done

Vertex is done
and validated.

Evaluation

Setup



Senario

- Real life scenario
- Test at high workloads
- Remove garbage
- Respond to packet
- Differ between concurrent connections

The test

- 17283 packets in total
- Two "sessions"
- 640*2 UDP packets that needs a response
- 640 well formed UDP packets with no session (discard)
- Rest of data is "background noise" (TCP packets with state, data, etc)
- Total data sent through: 1832958 bytes
- 1.83 Million clocks used

Latency calculations:

n_D : The number of bytes in the data part of the protocol. This excludes both headers from transport and internet.

n_I : The internet header size.

n_T : The transport header size.

n : The total packet size.

From packet to user

$$6 + n_I + 2n_T + 3n_D$$

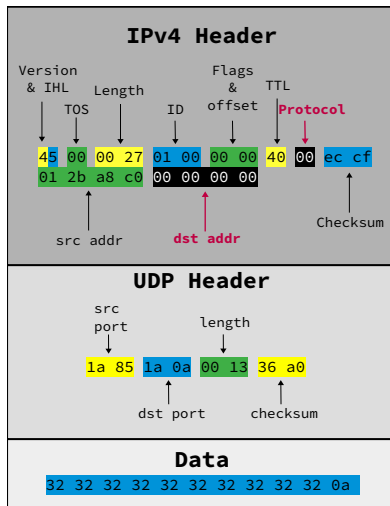
From user to packet

$$8 + 2n_I + 3n_T + 4n_D$$

Evaluation

Validation

Outgoing packet validation:



Internet Protocol Suite compliancy as per RFC 1122

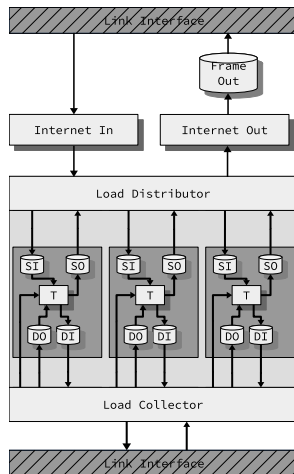
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Improving the performance:

Estimated performance:

$$1 \text{ Byte} * 10 \text{ MHz} = 80 \text{ Mbps}$$



Usability

SOMETHING

Using C#

State modelling
Simulation
Concurrency

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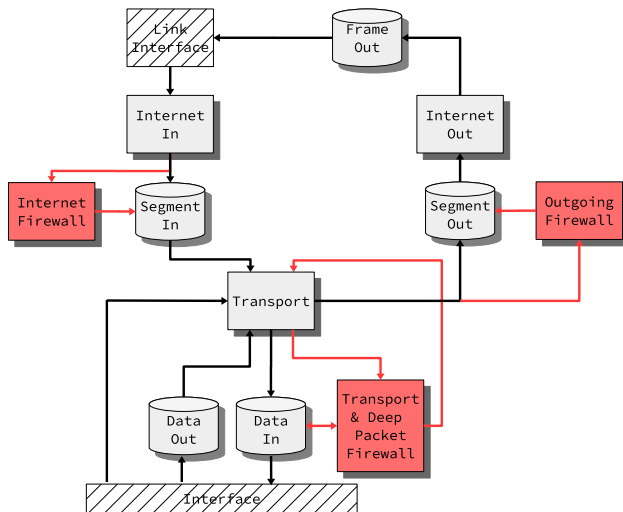
- Lot of trial and error to find the optimal design in the beginning
- In 10 mio. simulated clock cycles, 17283 packets were handled, 1280 of which were correctly received by the Application layer, and then sent out again
- Even with a few flaws, SME is a great framework for hardware modelling

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Future Work

Firewall



Future Work

TCP

How to implement TCP

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? Some random citation so it does not
complain[Andrew S Tanenbaum(2013)]



Todd Austin Andrew S Tanenbaum.

Structured computer organization.

Pearson, Boston, 2013.

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