ELEC5566M Assessment Summary

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| **Week** | |  | **Unit** | **Assessment** | **Weighting** | **Date Set** | **Deadline** |
| 14 | 29 January 2024 |  | Module Introduction & Software Install |  |  |  |  |
| 15 | 05 February 2024 |  | Unit 1.1: Gate Level Verilog |  |  |  |  |
| 16 | 12 February 2024 |  | Unit 1.2: Behavioural Verilog |  |  |  |  |
| 17 | 19 February 2024 |  | Unit 2.1: Synchronous Logic | Unit 1 - Design Task -  Code with incremental GitHub commits (30%) Test Bench (30%) Report and Documentation (40%) | 30% | 20th February 2024 | 5th March 2024 |
| 18 | 26 February 2024 |  | Unit 2.2: Finite State Machines |
| 19 | 04 March 2024 |  | Unit 3.1: FPGA Hardware | Units 2/3 – Mini-Projects - Working in small groups to wide design brief. Each student works on defined part of project. Must have separation of tasks. Code submission via GitHub (30%) Technical Report with Structure - Explanation of Code - Testing - Results - Frequency of reporting (40%) In person viva with demo, presentation and Q&A (30%) | 40% | 5th March 2024 | Code and Report 2nd May 2024 |
| 20 | 11 March 2024 |  | Unit 3.2: FPGA Hardware |
| 21 | 18 March 2024 |  | Unit 4 (Optional): Cyclone V HPS |
| E1 | 25 March 2024 |  | Easter Break |
| E2 | 01 April 2024 |  |
| E3 | 08 April 2024 |  |
| E4 | 15 April 2024 |  |
| 22 | 22 April 2024 |  |  |
| 23 | 29 April 2024 |  |  |
| 24 | 06 May 2024 |  |  |  |  |  |  |
| 25 | 13 May 2024 |  | Revision Week |  |  |  |  |
| 26 | 20 May 2024 |  | Assessment Weeks | Units 1 to 3 In-person online MCQ and short answer test  Date to be confirmed by exams office | 30% |  | Group Viva  and  Demonstration  Date to be confirmed |
| 27 | 27 May 2024 |  |
| 28 | 03 June 2024 |  |