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Informatik 11 Embedded Software | RWTH AACHEN UNIVERSITY

Exercise for

Embedded Systems

Summer Term 2025

Sheet 2: Data Buses

Exercise 1: Basics

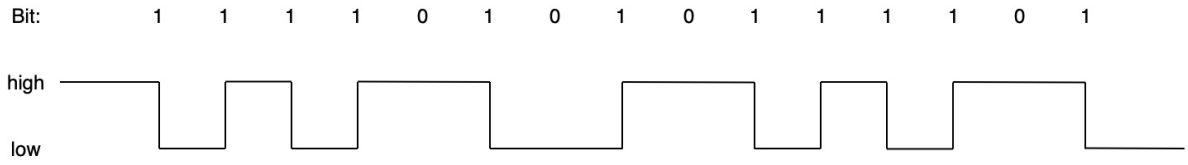
- Name two advantages that the star topology has over the bus topology.

  Solution:

  - Multiple senders at same time
  - Only one single point of failure
  - No collisions
  - No implicit broadcasts

- Use the 4B/5B table introduced in the lecture to encode the message **000000111111**. Then draw the signal diagram using Differential NRZI (that is Differential NRZ with inverted semantics: a level change represents a 1).

  Solution:



- What are the names of the two sublayers of Layer 2? What are their tasks?

  Solution:
  The sublayers of the Data Link Layer (DLL are:)

  - Logic Link Control (LLC)
    * Defines the frame format
    * Defines Adresses / IDs
    * Provides flow control
    * Provides error detection / correction

- Medium Access Control (MAC)
  - Defines which participant may send with which (Frequency / Code / Time)
  - Defines how collisions are handled (if possible)

Exercise 2: Hamming code

In 1950 Richard Hamming published his famous Hamming code. It's a linear error-correcting code, i.e., you cannot only detect errors, but also fix them. In this code, $2^n - 1$ bit are divided into n parity bits and $2^n - n - 1$ data bits. These bits are numbered from 1 to $2^n - 1$ and bits whose index is a power of two are the parity bits. E.g., for $n = 5$, bits 1, 2, 4, 8, and 16 are parity bits. Each data bit is protected by a unique set of parity bits: decompose the index of a data bit into a sum of unique powers of two; these summands are the parity bits for that data bit.
Example: Data bit 15 is protected by parity bits 1, 2, 4, and 8, because $1 + 2 + 4 + 8 = 15$.

- Calculate the even parity Hamming code of the following bit sequence:
  11001110

  Solution:
  The result is: 011110011110

- Correct and extract the 11 bit data sequence from this Hamming code protected sequence (even parity):
  100100101100011

  Solution:
  The result after correction is: 00011100011

Exercise 3: Inter-Integrated Circuit

- What topology does I^2C use?

  Solution:
  Bus Topology.

- What does Wired-AND mean?

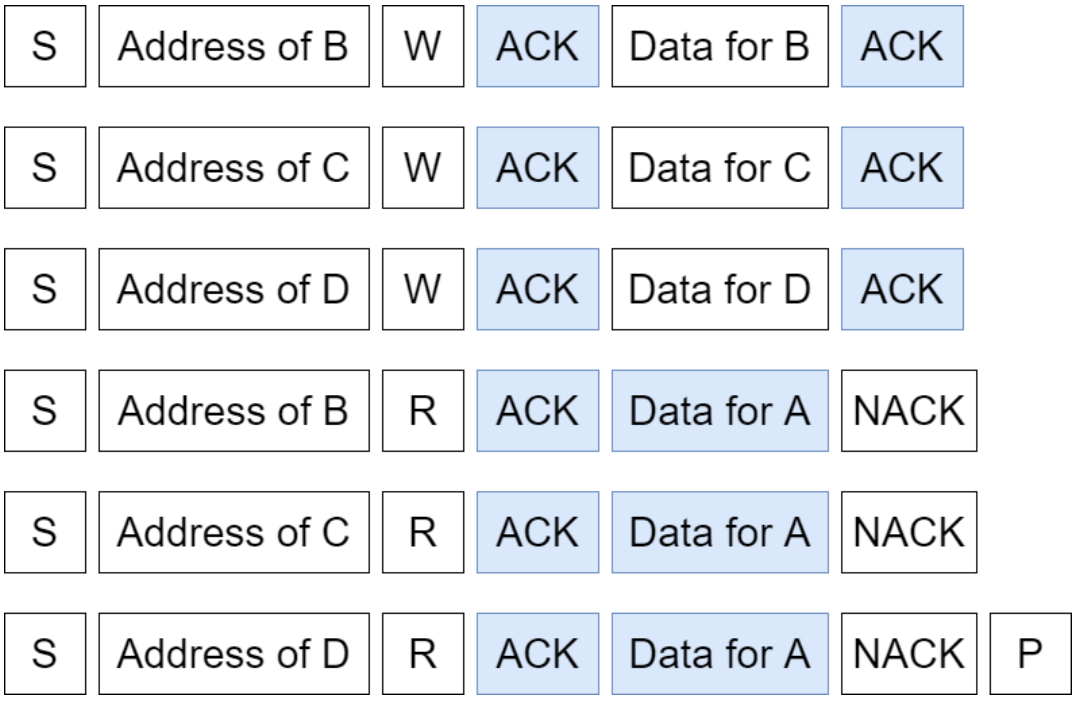
  Solution:
  A zero on the Bus is dominant.

- What is the basic MAC concept? Why are there no collisions when multiple senders start at the same time?

  Solution:
  The basic concept of Master-Slave is that the Master decides who can send at which time, while Slaves can only answer to read requests by Master.
  When there are multiple Masters the dominant 0 "wins", thus the Masters with a one at the first bit that differs between the senders stops transmitting.

- Use a block scheme to depict the following communication. A sends three participants B, C, and D a data byte each. Immediately after A sent the third data byte, it starts querying B, C, and D for a one byte response. You may use these blocks ($X \in \{A, B, C, D\}$), but you must indicate who controls the data line for each block:
  - Start-Flag
  - Stop-Flag
  - Address of X
  - Data for X
  - Read-Flag
  - Write-Flag
  - (N)ACK-Flag

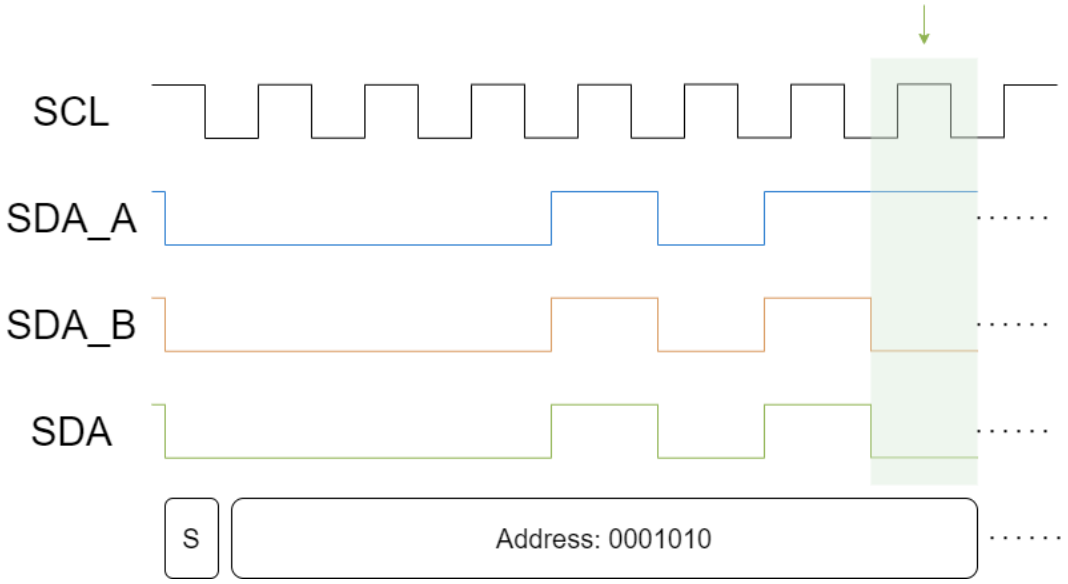
Solution:



Blue blocks are the ones not sent by A.

- A (address = 0x0a) and B (address = 0x0b) want to send messages to each other at the same time. A's message is 0xaa while B's message is 0xbb. Assume their clocks are perfecly synchronous, there is no transmission delay on the bus, and they start at the exact same point in time. Draw SCL, SDA_A, SDA_B, and SDA until the first transmission is complete. Mark the bit that decides who becomes master.

  Solution:



  The green marking shows the deciding Bit.

Exercise 4: Masters of Profibus
What is the topology of Profibus (using regular wire) and how is medium access controlled?

Solution:
Profibus uses a Bus Topology.
Medium Access is controlled through Master/Slave and Multiple Masters are managed using a Token Bus.