THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

This exam paper must not be removed from the venue

Venue _____

Seat Number _____

Student Number |__|__|__|__|__|__|__|__|

Family Name _____

First Name _____

School of Information Technology and Electrical Engineering

SAMPLE MID-SEMESTER EXAMINATION #3

Semester One Mid-semester Examinations, 2020

CSSE2010/CSSE7201 Introduction to Computer Systems

This paper is for St Lucia Campus students.

Examination Duration: 60 minutes

Reading Time: 10 minutes

Exam Conditions:

This is an Open Book Examination

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

Calculators - Casio FX82 series or UQ approved (labelled)

Materials To Be Supplied To Students:

1 x Multiple Choice Answer Sheet

Instructions To Students:

Answer all questions on the supplied "True/False and Multiple Choice Answer Sheet".

Choose the answer which best answers the question or completes the statement. Correct answers will be awarded one mark. Incorrect, missing or multiple answers will be awarded zero marks.

Total number of questions for the paper: 25

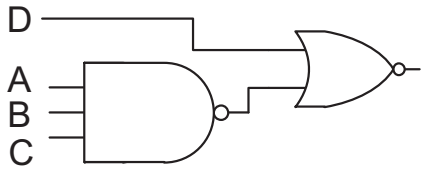
1. What is -57_{10} expressed in 9-bit excess-256 format?
   (a) 000111001
   (b) 011000111
   (c) 100111001
   (d) 111000111
   (e) None of the above

2. 0xB9 is equal to
   (a) 11001001_2
   (b) 10101001_2
   (c) 169_{10}
   (d) 201_{10}
   (e) 271_8

3. A 6-bit binary number in signed magnitude representation can represent integers from
   (a) -32 to 32
   (b) -32 to 31
   (c) -31 to 31
   (d) 0 to 31
   (e) None of the above

4. How can any n-bit binary number in two's complement representation (other than -2^{n-1}) be converted to n-bit one's complement representation?
   (a) By subtracting 1
   (b) By subtracting 1 and flipping all the bits
   (c) By subtracting the value of the most-significant bit
   (d) By adding the value of the most-significant bit
   (e) By flipping all the bits and subtracting the value of the most-significant bit

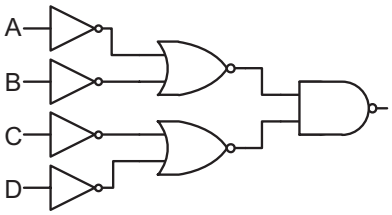
5. What function does the following circuit implement?

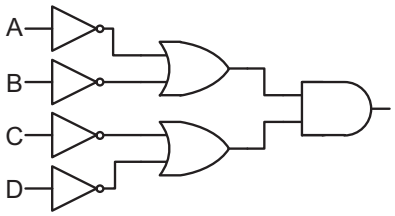


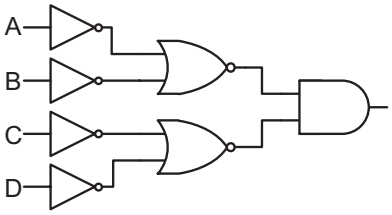
   (a) $A.B.C + \bar{D}$
   (b) $\overline{A.B.C} \oplus D$
   (c) $\overline{\overline{A.B.C} \oplus D}$
   (d) $\overline{\bar{A}.\bar{B}.\bar{C} + D}$
   (e) $\overline{\overline{A.B.C} + D}$

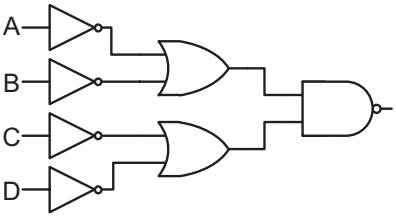
6. Which of the following logic functions is equivalent to $(A.\bar{B} + C).\overline{(\overline{A.C} + B)}$?
   (a) $A.\bar{B}$
   (b) $A.\bar{B}.C$
   (c) $A.\bar{B} + \bar{B}.C$
   (d) $A.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C$
   (e) None of the above

7. Which of the following circuits implements the function $A.B + C.D$?

(a) 

(b) 

(c) 

(d) 

(e) None of the above

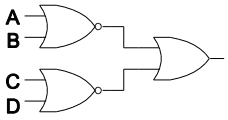
8. Consider the logic function represented by the following truth table:

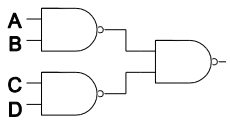
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

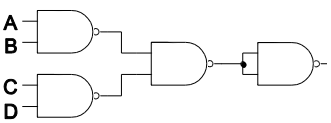
Which of the following expressions is equivalent to the function represented by this table?

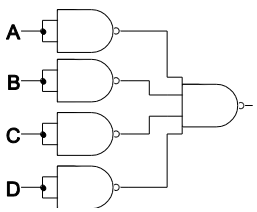
(a) $(A \oplus B).\bar{C} + (\overline{A + B}).C$
(b) $(A \oplus B) + C$
(c) $(A \oplus B) + \bar{A}.\bar{B}.C$
(d) $\bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + A.B.\bar{C}$
(e) None of the above

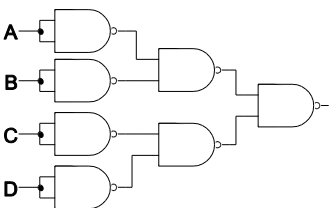
9. Which of the following circuits is a NAND-gate only implementation of the following function:



(a) 

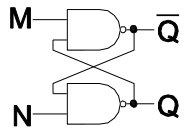
(b) 

(c) 

(d) 

(e) None of the above

10. Which truth table correctly captures the behaviour of the following latch circuit?



(a)

M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	0	0

(b)

M	N	Q	$\overline{Q}$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Q	$\overline{Q}$

(c)

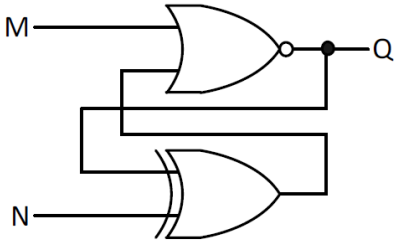
M	N	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

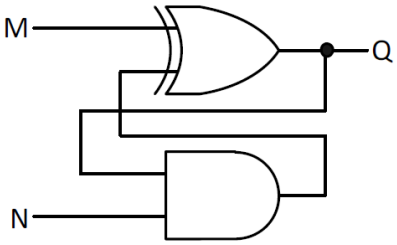
(d)

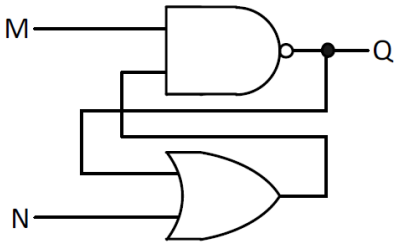
M	N	Q	$\overline{Q}$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

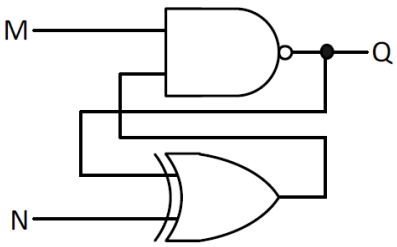
(e) None of the above

11. Which of the following circuits is capable of acting as a latch? i.e. it has combinations of inputs (M,N) which allow a bit (0 or 1) to be stored, the latch to be set (Q=1) with a single input transition, and the latch to be cleared (Q=0) with a single input transition?

(a)


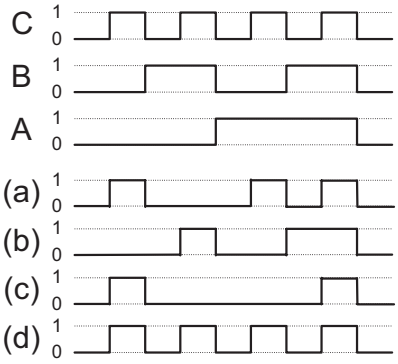
(b)


(c)


(d)


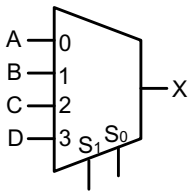
(e) None of the above

12. Which of the following timing diagrams represents the function $A.B.C + \bar{B}.C$?



(e) None of the above

13. Consider the following multiplexer. What must the inputs A,B,C,D be so that the multiplexer implements the function $X = S_1 + S_0.G$?



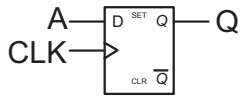
(a) A=**0** B=***G*** C=**1** D=**1**
(b) A=**1** B=**1** C=**0** D=***G***
(c) A=**1** B=**1** C=***G*** D=**0**
(d) A=***G*** B=***G*** C=**1** D=**1**
(e) A=***G*** B=**0** C=**1** D=**1**

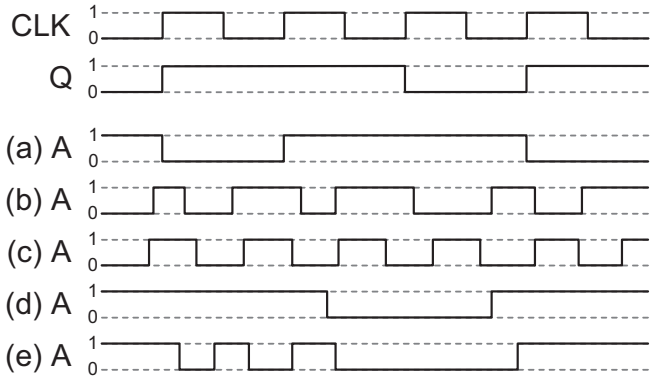
14. What is the result of adding the 6-bit two's complement numbers 010110 and 110011?
(a) 000001
(b) 001001
(c) 100101
(d) 101001
(e) 110111

15. Which of the following operations will result in an overflow in 4-bit two's complement arithmetic?
(a) 0100+0101
(b) 0100–0101
(c) 1001–0001
(d) 1001+0001
(e) None of the above

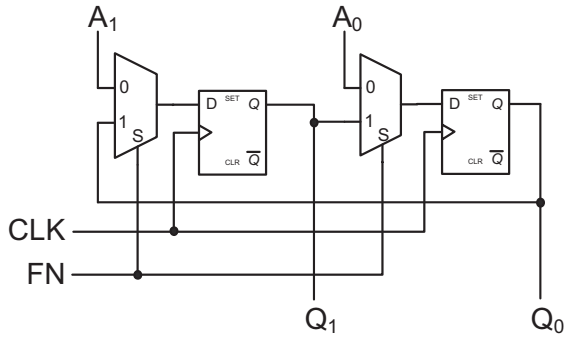
16. Consider the binary addition operation 1001 + 1110. Which of the following statements is true if the numbers are interpreted as two's complement?
(a) The result is negative and no overflow occurs
(b) The result should be negative but overflow occurs
(c) The result is positive and no overflow occurs
(d) The result should be positive but overflow occurs
(e) The result is zero

17. Consider the flip-flop circuit shown below and the associated CLK and output (Q) signals. Which timing diagram shows input (A) values over time which would have resulted in the given output (Q).





18. Consider the following circuit. If A_1 is 1 and A_0 is 0, what will be the values of Q_1 and Q_0 after three rising clock edges if FN is 0 for one rising clock edge then 1 for two rising clock edges?



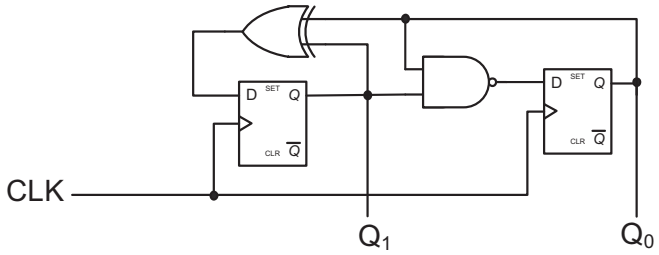
(a) $Q_1 = 0$ $Q_0 = 0$
(b) $Q_1 = 0$ $Q_0 = 1$
(c) $Q_1 = 1$ $Q_0 = 0$
(d) $Q_1 = 1$ $Q_0 = 1$
(e) Insufficient information is provided to determine the values

19. A sequential circuit has four outputs (X_3,X_2,X_1,X_0) which advance through the following repeating sequence:

$X_3X_2X_1X_0$: $0000 \rightarrow 0001 \rightarrow 0011 \rightarrow 0111 \rightarrow 1111 \rightarrow 1100 \rightarrow 0000 \rightarrow \ldots$

What is the minimum number of flip-flops needed to implement this circuit?
(a) 2
(b) 3
(c) 4
(d) 6
(e) 8

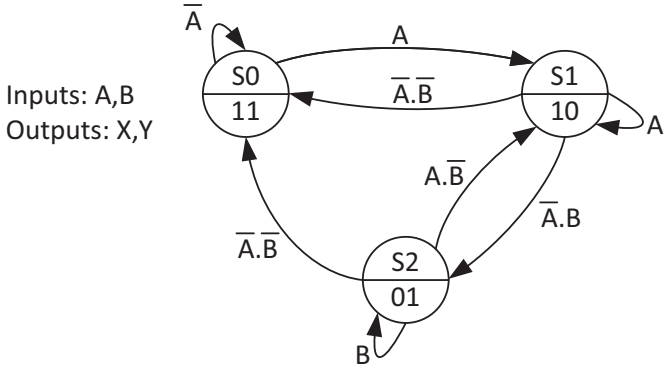
20. What sequence will the following synchronous counter count through, if it starts at $Q_1Q_0 = 00$?



(a) Q_1Q_0: $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \rightarrow \ldots$
(b) Q_1Q_0: $00 \rightarrow 01 \rightarrow 11 \rightarrow 00 \rightarrow \ldots$
(c) Q_1Q_0: $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \ldots$
(d) Q_1Q_0: $00 \rightarrow 10 \rightarrow 11 \rightarrow 00 \rightarrow \ldots$
(e) Q_1Q_0: $00 \rightarrow 11 \rightarrow 00 \rightarrow \ldots$

21. What's the minimum number of flip-flops needed to build a synchronous binary counter capable of counting from 0 to 16 (inclusive)?
(a) 3
(b) 4
(c) 5
(d) 16
(e) 17

22. Consider the state diagram below.



Which of the following is an equivalent state table?

(a)

Current State	Next State				Outputs (X,Y)
	AB=00	AB=01	AB=10	AB=11	
S0	S0	S0	S1	S1	11
S1	S0	S2	S1	S2	10
S2	S0	S2	S1	S2	01

(b)

Current State	Next State				Outputs (X,Y)
	AB=00	AB=01	AB=10	AB=11	
S0	S0	S1	S0	S1	11
S1	S0	S2	S1	S1	10
S2	S0	S1	S2	S2	01

(c)

Current State	Next State				Outputs (X,Y)
	AB=00	AB=01	AB=10	AB=11	
S0	S0	S1	S0	S1	00
S1	S0	S2	S1	S1	01
S2	S0	S2	S1	S2	10

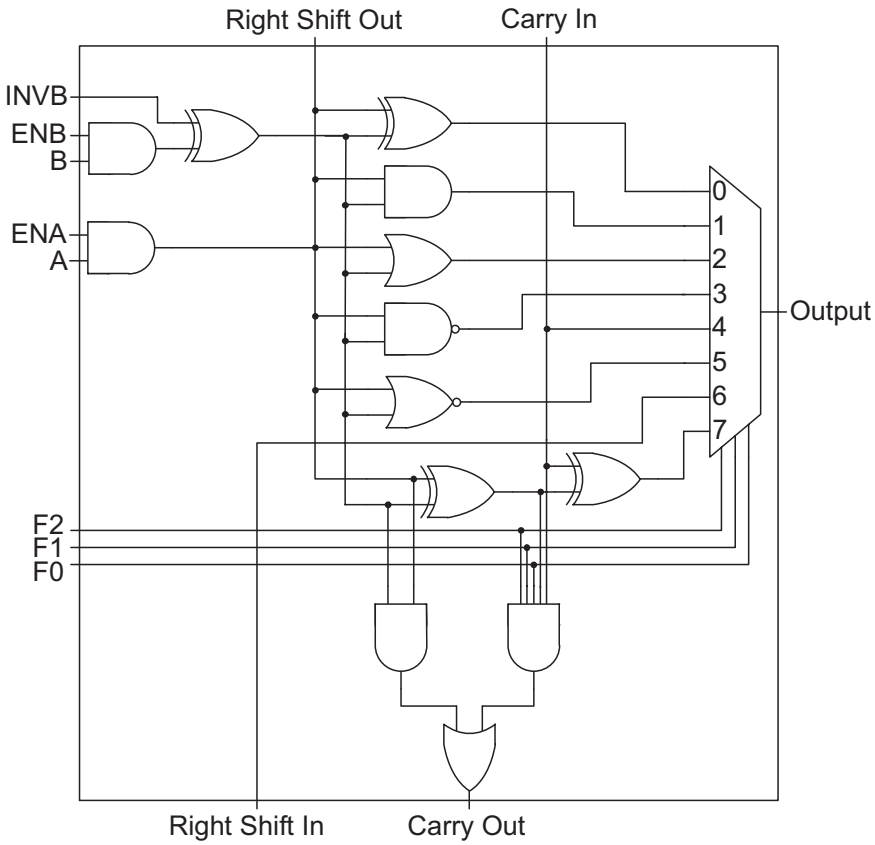
(d)

Current State	Next State				Outputs (X,Y)
	AB=00	AB=01	AB=10	AB=11	
S0	S0	S0	S1	S1	11
S1	S0	S2	S1	S1	10
S2	S0	S2	S1	S2	01

(e) None of the above

23. Consider the state machine represented by the state diagram shown in question 22. What sequence of states is traversed if the machine starts in state S0 and A goes through the sequence 1010101 and B is always the inverse of A?
(a) S0→S0→S1→S2→S1→S2→S1→S2
(b) S0→S1→S1→S2→S1→S2→S1→S2
(c) S0→S1→S2→S2→S1→S2→S1→S2
(d) S0→S1→S2→S1→S2→S1→S2→S1
(e) None of the above

24. Consider the ALU bit slice below (not the same as seen previously).



For an ALU made up of 8 of the bit slices above, which of the following control input settings will result in the ALU output being $\bar{A}.B$ (bitwise)? (The "Right Shift In" control input refers to that for the most significant bit; the "Carry in" control input refers to that for the least significant bit.)

(a) ENA=**1** ENB=**1** INVB=**0** F_2=**0** F_1=**0** F_0=**0** Right Shift In=**1** Carry in=**1**
(b) ENA=**1** ENB=**1** INVB=**0** F_2=**0** F_1=**0** F_0=**1** Right Shift In=**1** Carry in=**1**
(c) ENA=**1** ENB=**1** INVB=**1** F_2=**0** F_1=**0** F_0=**1** Right Shift In=**1** Carry in=**1**
(d) ENA=**1** ENB=**1** INVB=**0** F_2=**0** F_1=**1** F_0=**1** Right Shift In=**1** Carry in=**1**
(e) ENA=**1** ENB=**1** INVB=**1** F_2=**1** F_1=**0** F_0=**1** Right Shift In=**1** Carry in=**1**

25. For an ALU made up of 8 of the bit slices shown in question 24 above, which of the following control input function settings can **NOT** be used to output $\bar{B}$ (bitwise) – assuming other control inputs are chosen appropriately?

(a) F_2=**0** F_1=**0** F_0=**0** XOR
(b) F_2=**0** F_1=**1** F_0=**0** OR
(c) F_2=**0** F_1=**1** F_0=**1** NAND
(d) F_2=**1** F_1=**0** F_0=**1** NOR
(e) None of the above

END OF PAPER