THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

This exam paper must not be removed from the venue

Venue _____

Seat Number _____

Student Number |__|__|__|__|__|__|__|__|

Family Name _____

First Name _____

School of Information Technology and Electrical Engineering

SAMPLE MID-SEMESTER EXAMINATION #1

Semester One Mid-semester Examinations, 2020

CSSE2010/CSSE7201 Introduction to Computer Systems

This paper is for St Lucia Campus students.

Examination Duration: 60 minutes

Reading Time: 10 minutes

Exam Conditions:

This is an Open Book Examination

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

Calculators - Casio FX82 series or UQ approved (labelled)

Materials To Be Supplied To Students:

1 x Multiple Choice Answer Sheet

Instructions To Students:

Answer all questions on the supplied "True/False and Multiple Choice Answer Sheet".

Choose the answer which best answers the question or completes the statement. Correct answers will be awarded one mark. Incorrect, missing or multiple answers will be awarded zero marks.

Total number of questions for the paper: 25

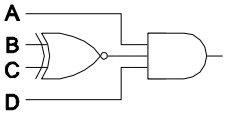
1. What is -21_{10} expressed in 8-bit one's complement format?
   (a) 10010101
   (b) 11101010
   (c) 11101011
   (d) 11110010
   (e) None of the above

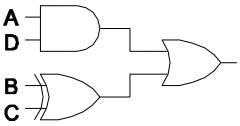
2. 111_8 is equal to
   (a) 1001001_2
   (b) 71_{10}
   (c) 0x73
   (d) 7_{10}
   (e) None of the above

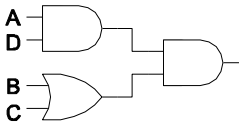
3. An n-digit radix-r number can represent unsigned integer values from 0 up to
   (a) $2^{(n-1)}$
   (b) $2^n - 1$
   (c) $r^{(n-1)} - 1$
   (d) $r^n - 1$
   (e) None of the above

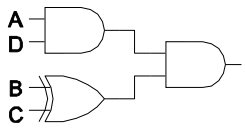
4. Which of the following statements about the 8 bit binary number 01100101 is true?
   (a) The number is negative in signed magnitude, two's complement, one's complement and excess-128 formats.
   (b) The number is positive in signed magnitude, two's complement, one's complement and excess-128 formats.
   (c) The number is odd when considered to be in signed magnitude, two's complement, one's complement or excess-128 formats.
   (d) The number is even when considered to be in signed magnitude, two's complement, one's complement or excess-128 formats.
   (e) None of the above

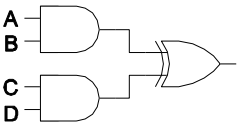
5. Which of the following logic circuits is an implementation of the function $A.(B \oplus C).D$?

(a) 

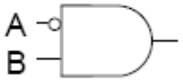
(b) 

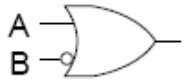
(c) 

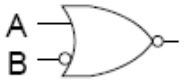
(d) 

(e) 

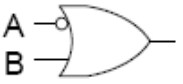
6. Which of the following circuits is equivalent to:



(a) 

(b) 

(c) 

(d) 

(e) None of the above

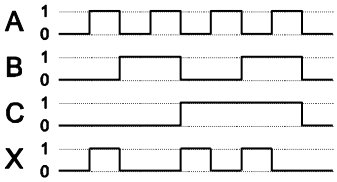
7. Which of the following logic functions is identical to $\overline{(\overline{\overline{A}+\overline{B}}).\overline{C}+\overline{B}}$?
   (a) 0
   (b) $AC+\overline{B}$
   (c) $AB+\overline{B}C$
   (d) $\overline{A}B+BC$
   (e) None of the above

8. Consider the logic function represented by the following truth table:

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

   Which of the following expressions is equivalent to the function represented in this table?
   (a) $X=A+B+C$
   (b) $X=A\overline{B}.\overline{C}+\overline{A}.\overline{B}.C+\overline{A}.B.\overline{C}$
   (c) $X=\overline{A}.B.\overline{C}+\overline{A}.B.C+\overline{A}.\overline{B}.\overline{C}$
   (d) $X=\overline{A.B.C}$
   (e) None of the above

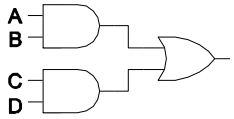
9. What logic function is represented by the following timing diagram?

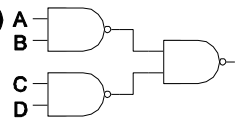


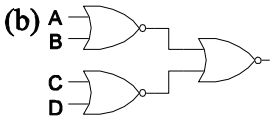
   (a) $X=\overline{C}.\overline{B}.A+\overline{C}.B.A+C.B.\overline{A}$
   (b) $X=\overline{C}.\overline{B}.\overline{A}+C.B.\overline{A}+\overline{C}.B.\overline{A}$
   (c) $X=C.\overline{B}.A+C.\overline{B}+C.\overline{A}$
   (d) $X=\overline{C}.\overline{B}.A+C.\overline{B}.\overline{A}+C.B.\overline{A}$
   (e) None of the above

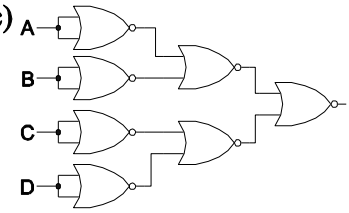
10. Which of the following logic functions is identical to $A\oplus\overline{B}$?
    (a) $A.\overline{B}+\overline{A}.B$
    (b) $\overline{A}.\overline{B}+\overline{A}.B+A.B$
    (c) $A+\overline{B}$
    (d) $\overline{A\oplus B}$
    (e) None of the above

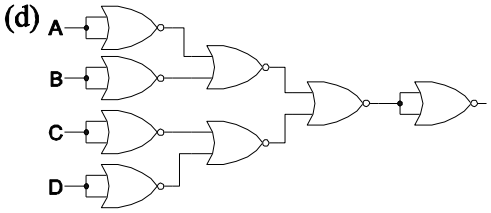
11. Which of the following circuits is a NOR-gate only implementation of the following function:



(a)


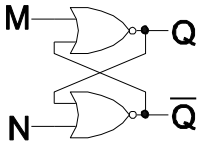
(b)


(c)


(d)


(e) None of the above

12. Which truth table correctly captures the behaviour of the following latch circuit?



(a)

M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

(b)

M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	1	1

(c)

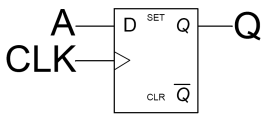
M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	1	1

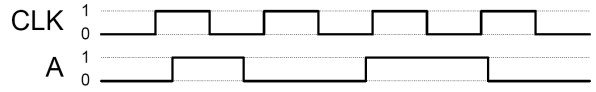
(d)

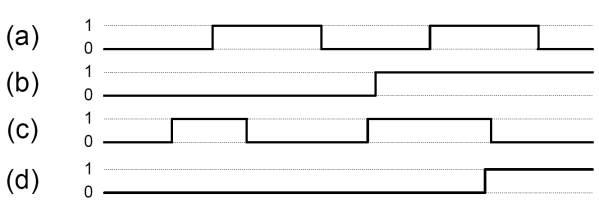
M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	0	0

(e) None of the above

13. For the flip-flop circuit below and the given CLK and A values over time, which of the diagrams below best shows the Q output?







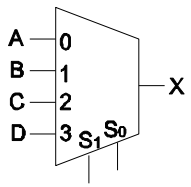
(e) None of the above

14. What's the result of adding the 5-bit two's complement numbers 11101 and 01001?
    (a) 00110
    (b) 00111
    (c) 01100
    (d) 10110
    (e) 10111

15. Which of the following operations will result in an overflow in 5-bit two's complement arithmetic?
    (a) 10010+00010
    (b) 10010–00010
    (c) 01000+01010
    (d) 01000–01010
    (e) None of the above

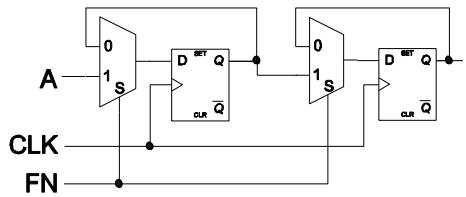
16. Consider the binary addition operation 0111 + 0001. Which of the following statements is true if the numbers are interpreted as two's complement?
    (a) The result is negative and no overflow occurs
    (b) The result should be negative but overflow occurs
    (c) The result is positive and no overflow occurs
    (d) The result should be positive but overflow occurs
    (e) The result is zero

17. Consider the following multiplexer. What must the inputs A,B,C,D be so that the multiplexer implements the function $X = S_1 \oplus S_0$?



    (a) A=1, B=1, C=1, D=1
    (b) A=1, B=0, C=0, D=1
    (c) A=0, B=1, C=1, D=0
    (d) A=1, B=1, C=0, D=0
    (e) None of the above

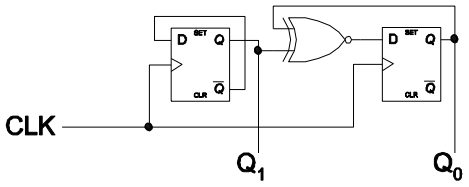
18. Which of the following statements about this shift register circuit is true?



    (a) When A is 1, data will be shifted to the right on every rising clock edge
    (b) When A is 0, data will be shifted to the right on every rising clock edge
    (c) When FN is 1, data will be shifted to the left on every rising clock edge
    (d) When FN is 0, the flip-flops will maintain their values (even if the circuit is clocked)
    (e) None of the above

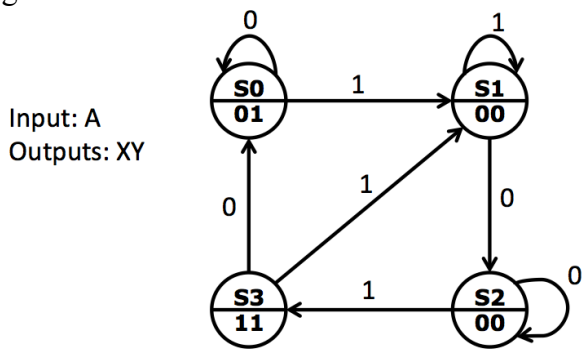
19. What's the minimum number of flip-flops needed to build a synchronous binary counter capable of counting from 0 to 32 (inclusive)?
    (a) 5
    (b) 6
    (c) 7
    (d) 32
    (e) 33

20. What sequence will the following synchronous counter count through?



    (a) Q_1Q_0: 00 → 01 → 10 → 11 → 00 → …
    (b) Q_1Q_0: 00 → 10 → 11 → 01 → 00 → …
    (c) Q_1Q_0: 00 → 11 → 01 → 10 → 00 → …
    (d) Q_1Q_0: 00 → 01 → 11 → 10 → 00 → …
    (e) None of the above

21. Consider the state diagram below.



Which of the following is an equivalent state table?

(a)

Current State	Input (A)	Next State	Outputs (X,Y)
S0	0	S0	01
S0	1	S1	01
S1	0	S1	00
S1	1	S2	00
S2	0	S2	00
S2	1	S3	00
S3	0	S0	11
S3	1	S1	11

(b)

Current State	Input (A)	Next State	Outputs (X,Y)
S0	0	S0	01
S0	1	S1	01
S1	0	S2	00
S1	1	S1	00
S2	0	S2	00
S2	1	S3	00
S3	0	S0	11
S3	1	S2	11

(c)

Current State	Next State		Outputs (X,Y)
	A=0	A=1	
S0	S0	S1	01
S1	S2	S1	00
S2	S2	S3	00
S3	S0	S1	11

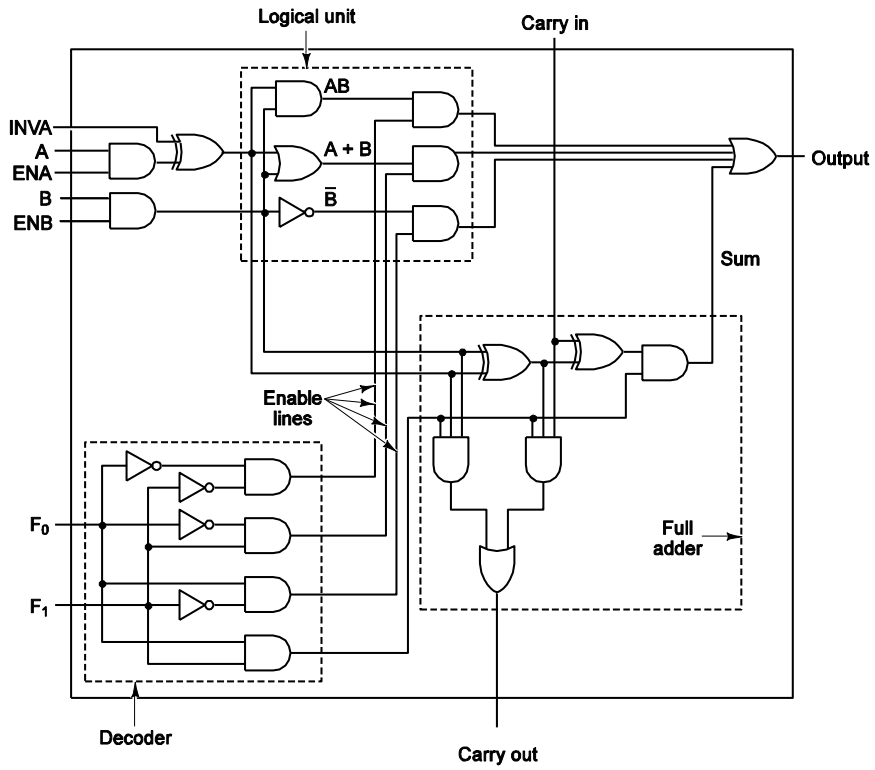
(d)

Current State	Next State		Outputs (X,Y)
	A=0	A=1	
S0	S0	S1	00
S1	S2	S1	01
S2	S2	S3	10
S3	S0	S1	11

(e) None of the above

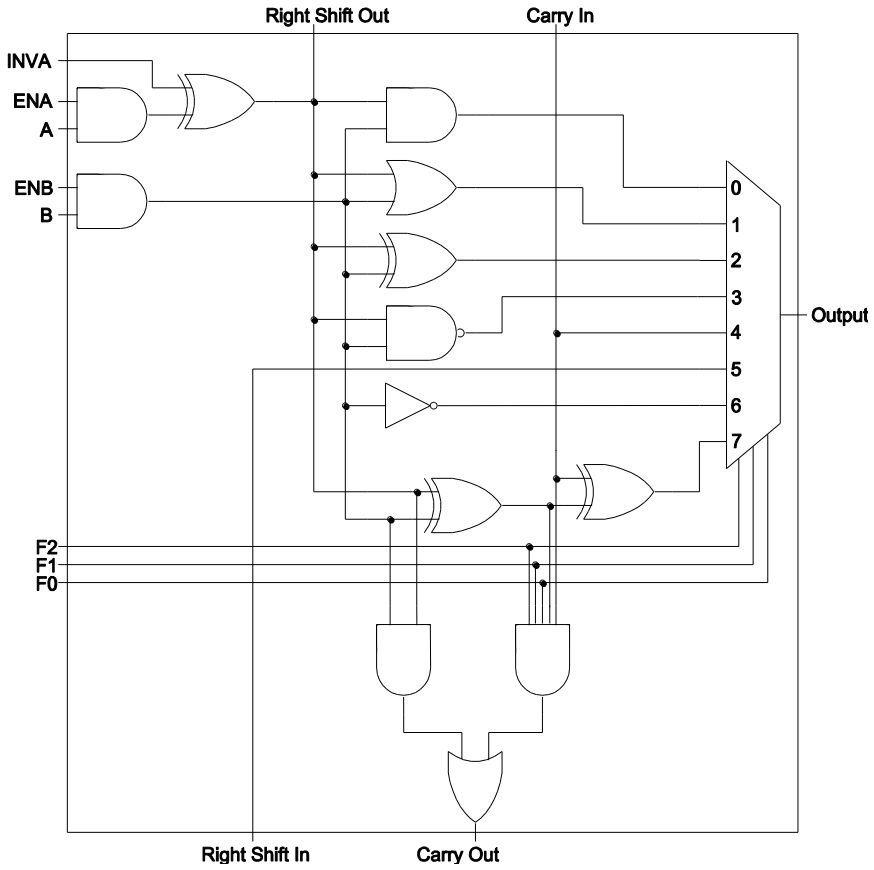
22. Consider the state machine represented by the state diagram in question 21 above. What sequence of states is traversed if the machine starts in state S0 and A goes through the sequence 110011 (i.e. two 1's followed by two 0's followed by two 1's)?
    (a) S0→S1→S2→S2→S3→S1→S1
    (b) S0→S1→S2→S3→S0→S1→S2
    (c) S0→S1→S1→S2→S2→S3→S3
    (d) S0→S1→S2→S3→S1→S2→S3
    (e) S0→S1→S1→S2→S2→S3→S1

23. Consider the ALU bit slice below (from the Tanenbaum textbook, also shown in lectures)



For the ALU bit slice above, under what conditions will the ALU output be A?
(a) ENA = 0, ENB = 0, INVA = 1, F_0 = 1, F_1 = 0, Carry in = 0
(b) ENA = 1, ENB = 1, INVA = 1, F_0 = 0, F_1 = 0, Carry in = 0
(c) ENA = 1, ENB = 0, INVA = 1, F_0 = 0, F_1 = 1, Carry in = 0
(d) ENA = 1, ENB = 0, INVA = 0, F_0 = 1, F_1 = 1, Carry in = 0
(e) None of the above

24. Consider the ALU bit slice below.



For an ALU made up of 8 of the bit slices above, which of the following control input settings will result in the ALU output being $A-1$? (The "Right Shift In" control input refers to that for the most significant bit; the "Carry in" control input refers to that for the least significant bit.)

(a) ENA = 1, ENB = 0, INVA = 0, $F_2 = 1$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 0
(b) ENA = 1, ENB = 0, INVA = 1, $F_2 = 1$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 0
(c) ENA = 1, ENB = 0, INVA = 0, $F_2 = 1$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 1
(d) ENA = 1, ENB = 0, INVA = 1, $F_2 = 1$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 1
(e) None of the above

25. For the ALU in question 24, which of the following arithmetic operations can NOT be performed?

(a) $A + 1$
(b) $B + 1$
(c) $A - 1$
(d) $B - 1$
(e) All of the above operations can be performed