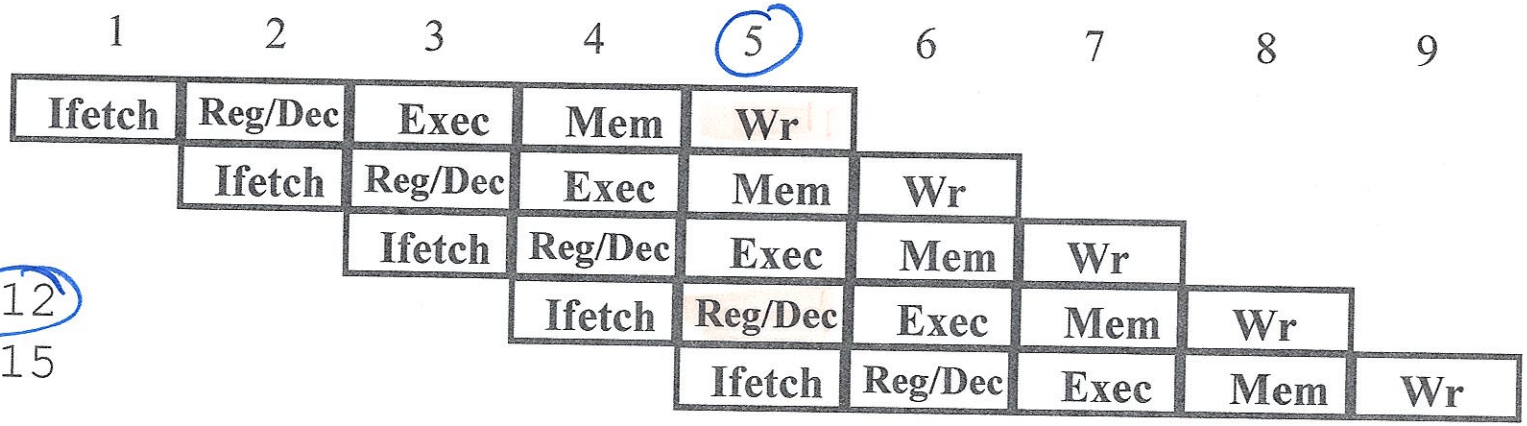
Review Problem 31

- What registers are being read and written in the 5th cycle of a pipelined CPU running this code?

```
ADD X1, X2, X3
ORR X4, X5, X6
SUB X7, X8, X9
EOR X10, X11, X12
AND X13, X14, X15
```



Writing X1

Reading X11, X12

The Stages of Conditional Branch

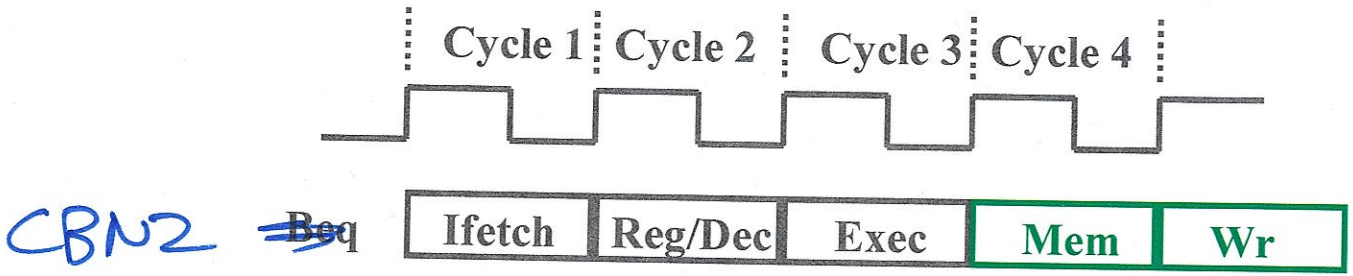
Ifetch: Fetch the instruction from the Instruction Memory

Reg/Dec: Register Fetch and Instruction Decode, compute branch target

Exec: Test condition & update the PC

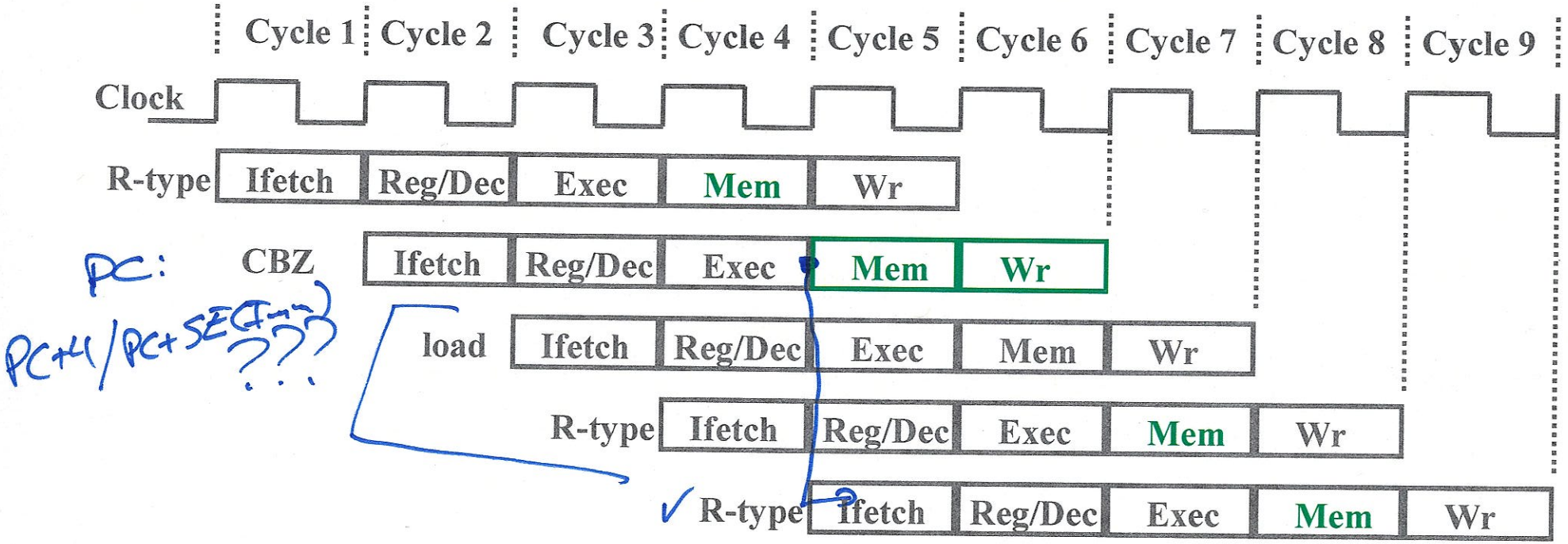
Mem: NOOP

Wr: NOOP



Control Hazard

Branch updates the PC at the end of the Exec stage.

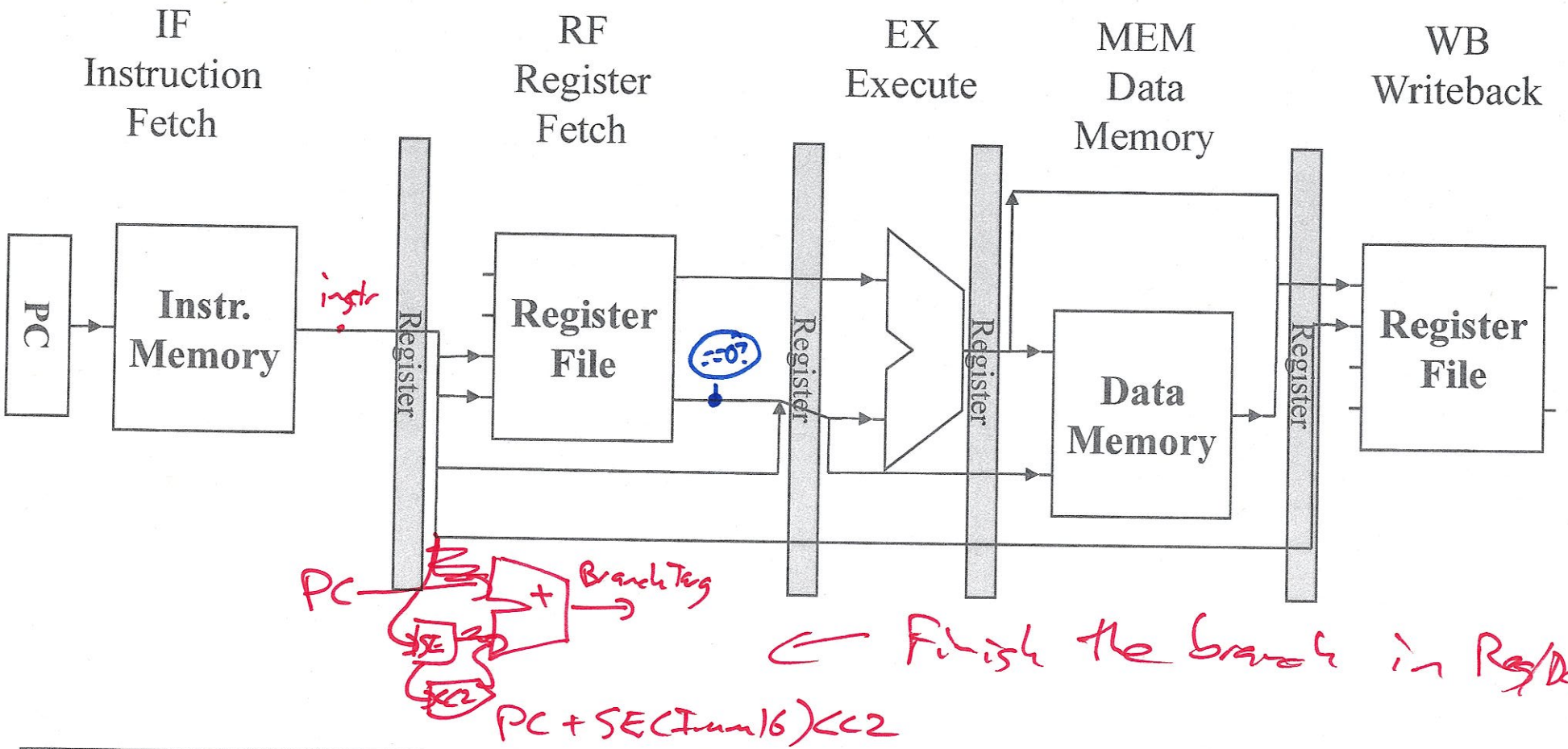


Accelerate Branches

PC = PC + SEC Imm16)

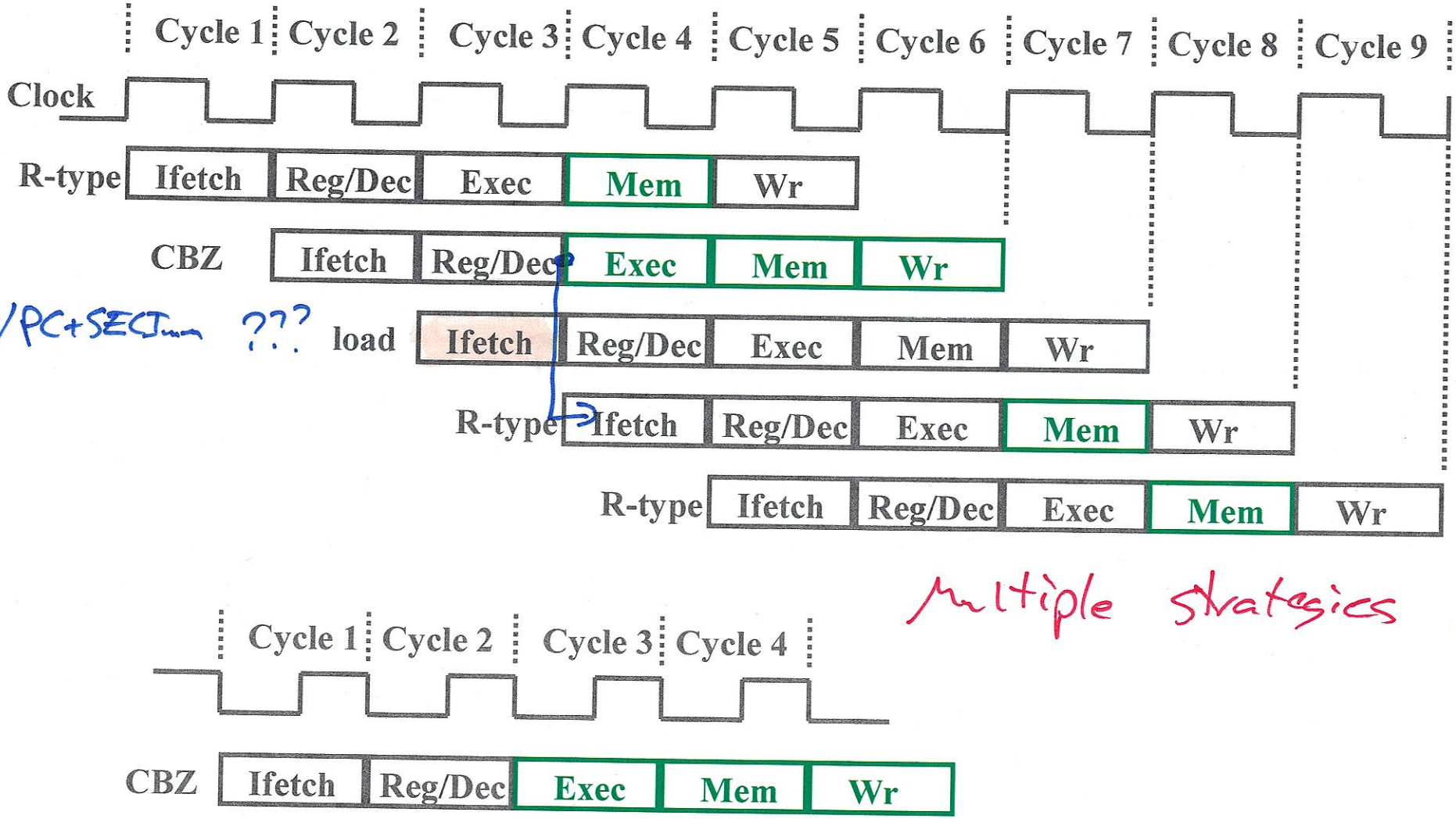
When can we compute branch target address?

When can we compute the CBZ condition?



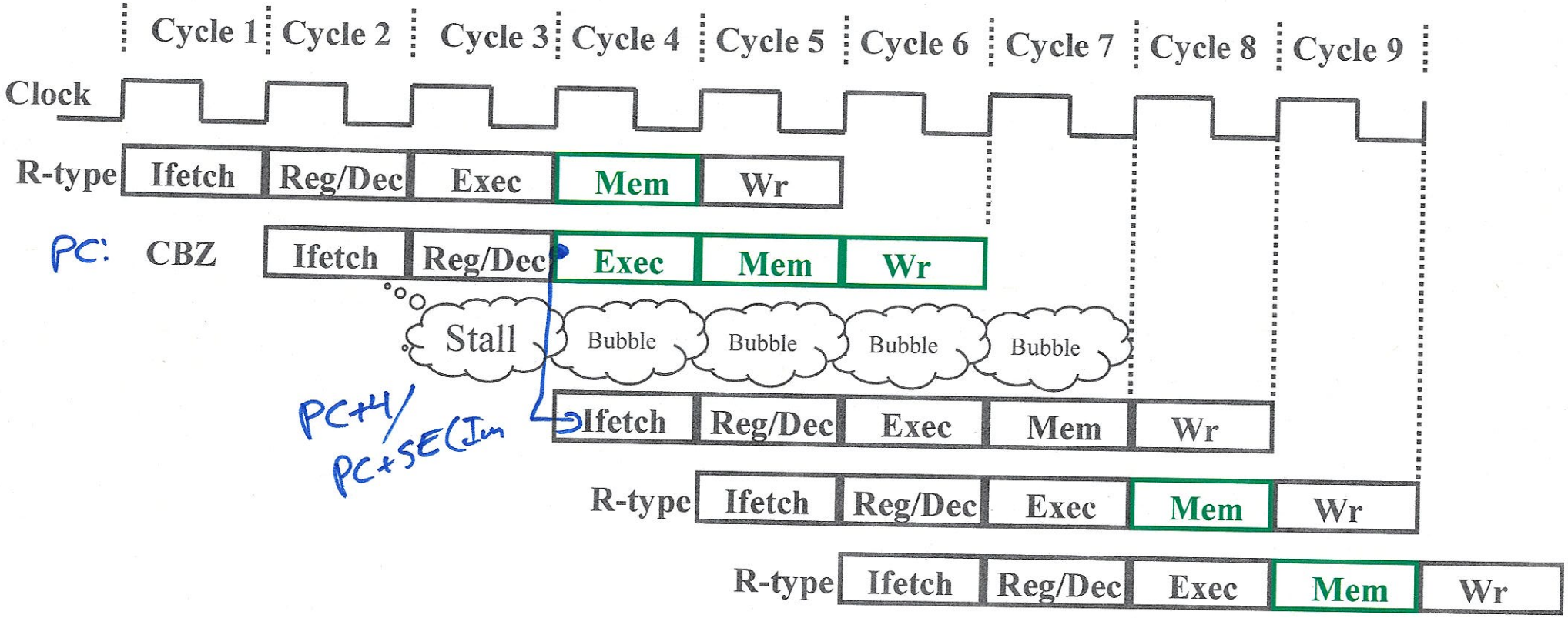
Control Hazard 2

Branch updates the PC at the end of the Reg/Dec stage.



Solution #1: Stall

Delay loading next instruction, load no-op instead

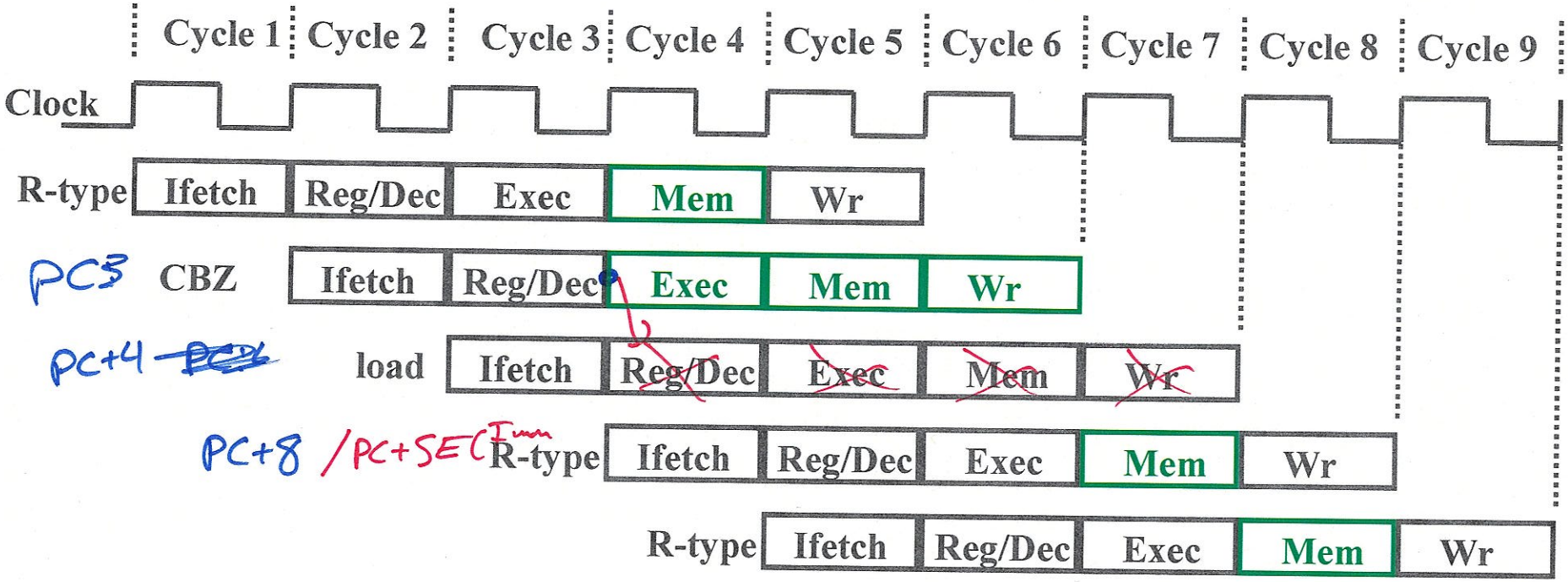


CPI if all other instructions take 1 cycle, and branches are 20% of instructions?

CPI = 80%×1 + 20%(1 fetch + 1 stall) = 0.8 + 0.4 = 1.2

Solution #2: Branch Prediction

Guess all branches not taken, squash if wrong



CPI if 50% of branches actually not taken, and branch frequency 20%?

$CPI = 80\% \times 1 + 20\%\,(\overbrace{50\% \times 1}^{NT} + \overbrace{50\% \,(2)}^{T})$

$= 0.8 + 0.2\,(1.5) = 0.8 + 0.3 = 1.1$