Xi'an Jiaotong-Liverpool University

西交利物浦大学

PAPER CODE	EXAMINER	DEPARTMENT	TEL
EEE339		Electrical & Electronic Engineering	

1st SEMESTER 2023/24 FINAL EXAMINATION

BACHELOR DEGREE – Year 4

DIGITAL SYSTEM DESIGN WITH HDL

TIME ALLOWED: 3 Hours

INSTRUCTIONS TO CANDIDATES

1、 **Answer all questions.**

2、 **Total marks available are 100.**

3、 **The marks without parenthesis are the marks for whole questions, while those within a pair of parentheses are the marks for sub-questions.**

4、 **In answering the questions in this paper, it is particularly important to give explanations with your answer. Only partial marks will be awarded for correct answers with inadequate explanations.**

5、 **Answers should be written in the answer booklet(s) provided.**

1 Read each of the following statements carefully. If the following statement is true for Verilog code, answer T, otherwise answer F and give reasons. In the latter case, if there are no correct reasons provided, no mark will be awarded. **Each correct answer is worth 1 mark**. **10**

2 Write Verilog code for the circuit shown in Figure Q2. As indicated in the figure, assume positive edge triggered flip-flops, and an active-HIGH asynchronous reset. **15**

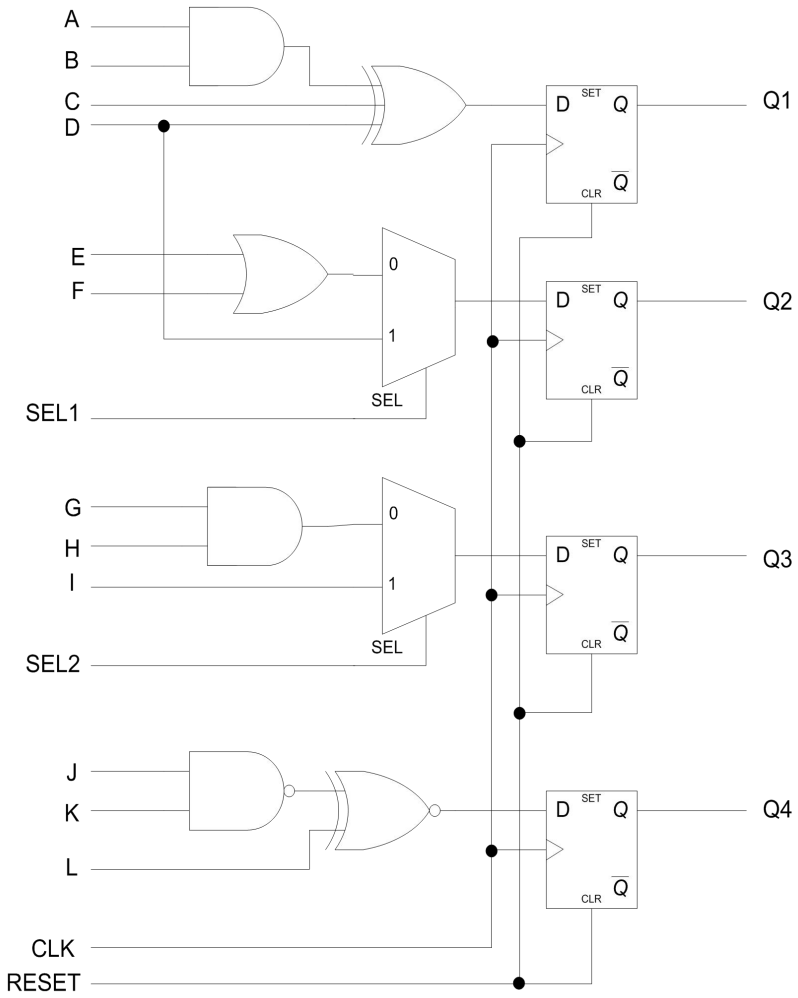

Figure Q2

3 (a) Write Verilog code for a T-type flip-flop. This flip-flop has an input T and an output Q. At each positive edge of clock (clk), the output (Q) is inverted, if the input T is logic HIGH, and the output (Q) doesn't change if the input (T) is logic LOW. The flip-flop has an active-HIGH asynchronous reset (rst). Only use the given inputs and output (T, Q, Clk, Rst). **15 (6)**

(b) Write the Verilog code for a 4-bit synchronous counter using such toggle (T-type) flip-flops (module instantiation), as shown in Figure Q3. The counter has an active-HIGH asynchronous reset (rst) and a terminal count output (Tc). **(9)**

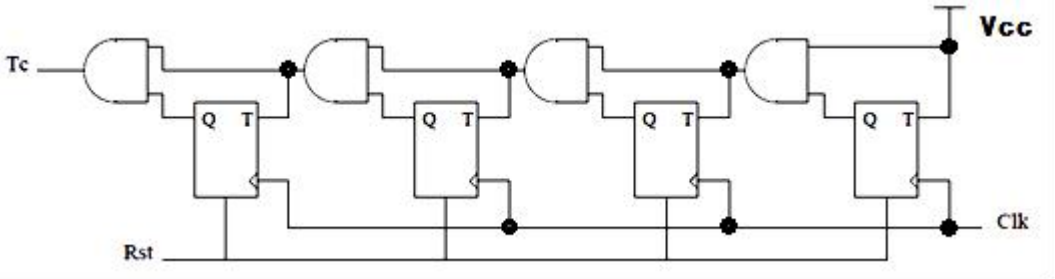

Figure Q3

4 A state machine used in a process control system has 3 states. It has a clock and an asynchronous (active high) reset signal, one input called *sensor* and one output called *valve*. The *valve* output is high in state S1 or S2. The next state/output table is: **20**

Current State	sensor		valve
	0	1	
S0	S0	S1	0
S1	S1	S2	1
S2	S0	S0	1
	S*		

(a) Is this of Moore type or of Mealy type? Why? **(2)**
(b) Draw a state diagram of the state machine. **(4)**
(c) Write Verilog code to implement this state machine. **(14)**

5 Suppose in a computer there are three types of instructions A, B and C. The Cycles per Instruction (CPI) for these instructions are: $CPI_A = 1.1$, $CPI_B = 2.7$, $CPI_C = 1.9$. **10**

(a) What is the average CPI of computer M for running program P_1 with 32% type A instructions, 27% type B instructions and the remainder typeC instructions? What is the average CPI of M for running program P_2 with 29% type A instructions, 17% type B instructions and the remainder type C instructions? **(5)**

(b) Let the non-pipelined computer M have a clock rate of 2.8 GHz. Both P_1 and P_2 have 100 instructions. Given the average CPIs for P_1 and P_2 (from (a)), calculate the CPU times to run programs P1 and P2. Which program is faster to run? **(5)**

6 (a) Identify and explain *all* data hazards (including hazard type and each operand pair that causes the hazard) in the execution of the following MIPS instructions on a five stage pipelined implementation (assume not-taken branch prediction, and a register file and memories capable of half clock cycle (e.g., split-cycle) writes/reads) : **15 (5)**

```
L1 add $s1, $s2, $s1
L2 beq $s1, $s2, Exit
L3 sub $s2, $s1, $s2
L4 sw $s2, 16($s1)
```

(b) Draw the IF-ID-EX-MEM-WB pipeline diagram using EX-> EX and EX-> MEM forwarding. **(5)**

(c) How many cycles are required to execute these four instructions? Given this information, calculate the CPI of this program on this pipeline. **(5)**

7 For the MIPS multicycle datapath shown in Figure Q7, determine the functions of the ALU and the values of the control signals ALUSrcA, ALUSrcB, ALUOp, PCSource in all the clock cycles of a beq instruction. ALUOp = 00 for addition, and ALUOp = 01 for subtraction. **15**

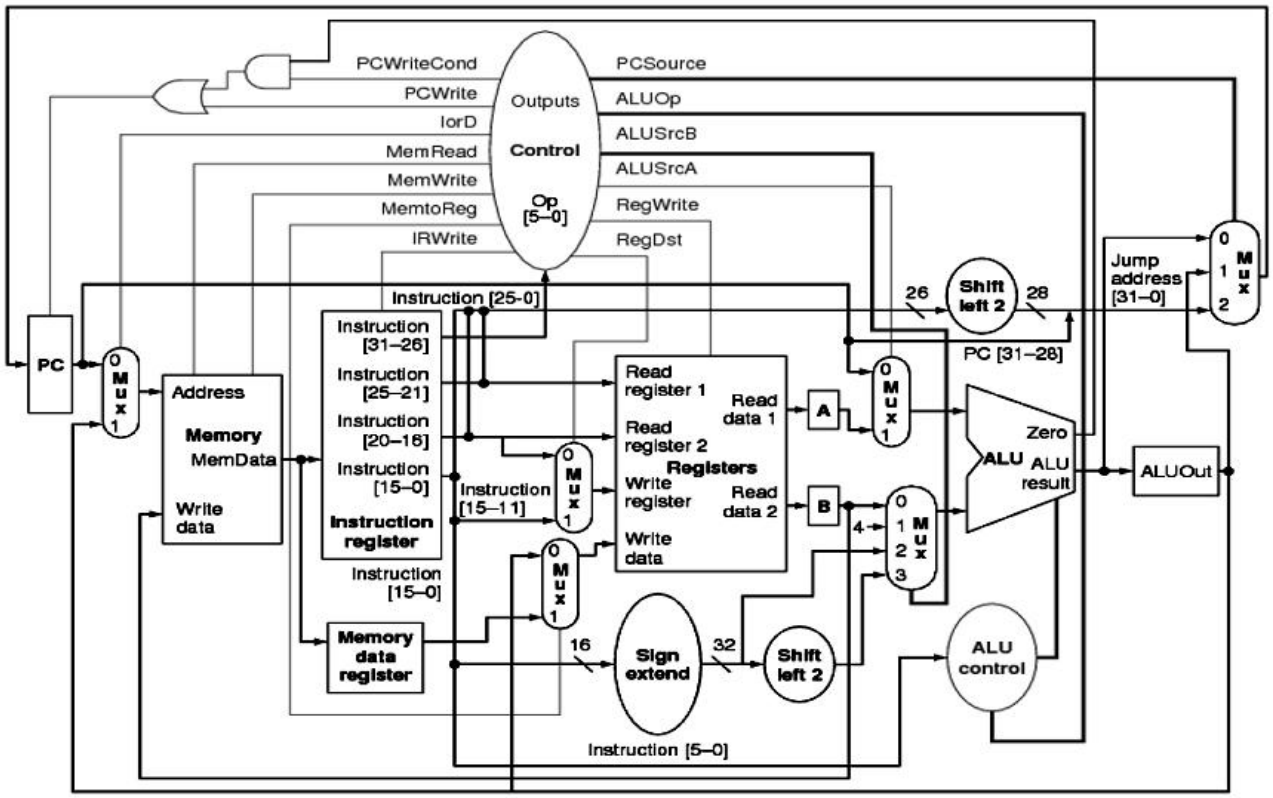

Figure Q7

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