

1. *What is the purpose of this study?*  
 2. *What are the research objectives?*  
 3. *What is the research methodology?*  
 4. *What are the results of the study?*  
 5. *What are the conclusions of the study?*  
 6. *What are the limitations of the study?*  
 7. *What are the implications of the study?*  
 8. *What are the future research directions?*  
 9. *What are the contributions of the study?*  
 10. *What are the key findings of the study?*  
 11. *What are the main results of the study?*  
 12. *What are the primary outcomes of the study?*  
 13. *What are the secondary outcomes of the study?*  
 14. *What are the tertiary outcomes of the study?*  
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Ifetch	Reg/Dec	Exec	Mem	W/r	6	7	8	9
Ifetch	Reg/Dec	Exec	Mem	W/r				
Ifetch	Reg/Dec	Exec	<del>Reg/Dec</del>	Exec	Mem	W/r	8	9
Ifetch	Reg/Dec	Exec	Mem	W/r	W/r			
Ifetch	Reg/Dec	Exec	Mem	W/r	6	7	8	9

Fixed by the

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M

X2 Forwarded in cycle 5

X0 forwarded in cycle 4

Dor't for ward X311

# Pipelined CPI, cycle time

CPI, assuming compiler can fill 50% of delay slots

Instruction Type	Type Cycles	Type Frequency	Cycles * Freq
ALU	1.0	X 50%	= 0.5
Load	1.5	X 20%	= 0.3
Store	1.0	X 10%	= 0.1
Branch	1.5	X 20%	= 0.3
CPI:			1.2

Pipelined: cycle time = 1ns.

Delay for 1M instr:  $1.2 \times 10^6 \times 1\text{ns} + 4\text{ns}$

Single cycle: CPI = 1.0, cycle time = 4.5ns.

Delay for 1M instr:  
 $4.5 \times 10^6\text{ns}$

## Pipelined CPU Summary

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Improve cycle time

Concerns:

Structural Hazards

Control Hazards

Data Hazards



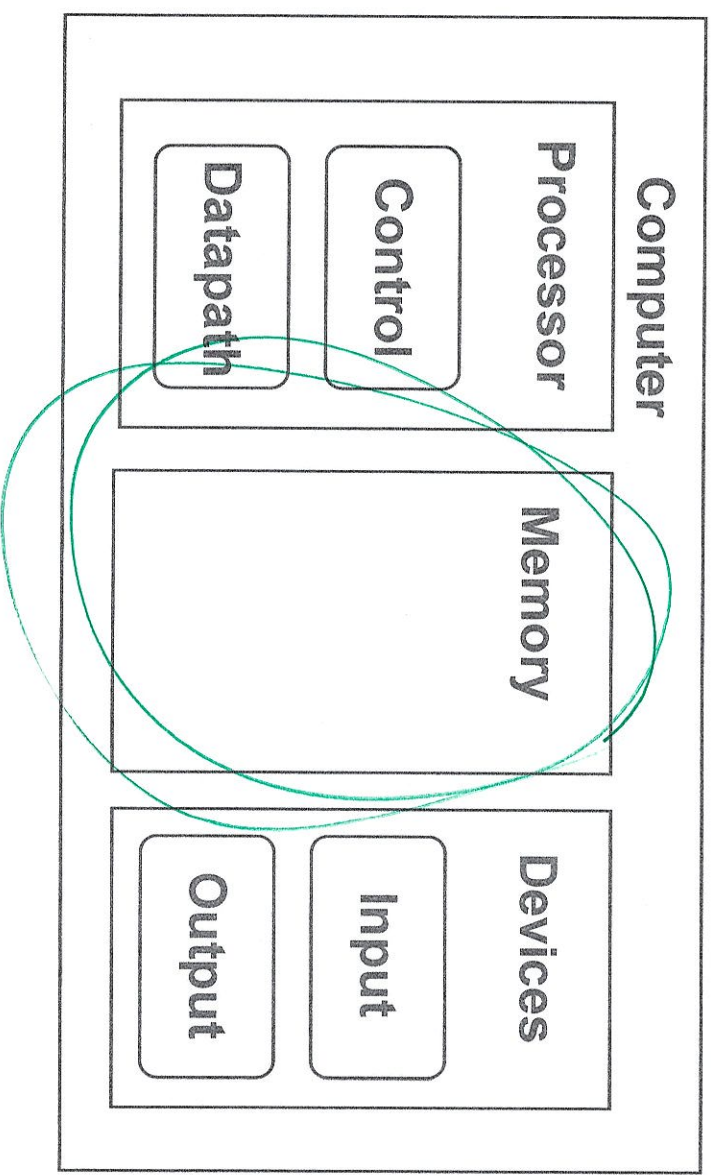
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# Memory Hierarchy: Caches, Virtual Memory

Readings: 5.1-5.4, 5.8

Big memories are slow

Fast memories are small



Need to get fast, big memories

# Random Access Memory

Read/Write

Dynamic Random Access Memory (DRAM)

High density, low power, cheap, but slow

Dynamic since data must be "refreshed" regularly

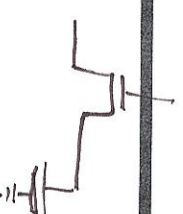
Random Access since arbitrary memory locations can be read

Static Random Access Memory

Low density, high power, expensive

Static since data held as long as power is on

Fast access time, often 2 to 10 times faster than DRAM



Technology	Access Time	Cost/Capacity
SRAM	1-7 cycles	10,000x
DRAM	100 cycles	200x
Disk	10K – 10M cycles	1x