

Review Problem 6

❖ Register X0 has the address of a 3 integer array.

Set X15 to 1 if the array is sorted (smallest to largest), 0 otherwise.

```
ADD    X15, X31, X31      // initialize to 0
LDUR   X1, [X0, #0]       // array[0]
LDUR   X2, [X0, #8]       // array[1]
LDUR   X3, [X0, #16]      // array[2]

CMP     X1, X2             //
B.GE    UNSORTED          //
CMP     X2, X3
B.GE    UNSORTED
CMP     X1, X3
B.GE    UNSORTED
ADDI    X15, X31, #1       // set to 1 - sorted!
UNSORTED:
```

Labels

Labels specify the address of the corresponding instruction

Programmer doesn't have to count line numbers

Insertion of instructions doesn't require changing entire code

```
// X0 = N, X1 = sum, X2 = I
-6 -3 ADD X1, X31, X31 // sum = 0
-5 -2 ADD X2, X31, X31 // I = 0

TOP:
-4 -1 CMP X2, X0 // Check I vs N
-3 0 B.GE END +4 // end when !(I<N)
-2 +1 ADD X1, X1, X2 // sum += I
-1 +2 ADDI X2, X2, #1 // I++
0 +3 B TOP -4 // next iteration
END:
+1 +4
```

Notes:

Branches are PC-relative

$$PC = PC + 4 * (\text{BranchOffset})$$

BranchOffset positive -> branch downward. Negative -> branch upward.

Labels Example

Naively: $PC = PC + 4$

Compute the value of the labels in the code below.

Branches: $PC = PC + 4 * (\text{BranchOffset})$

```
// Program starts at address 100
LDUR X0, [X31, #100]

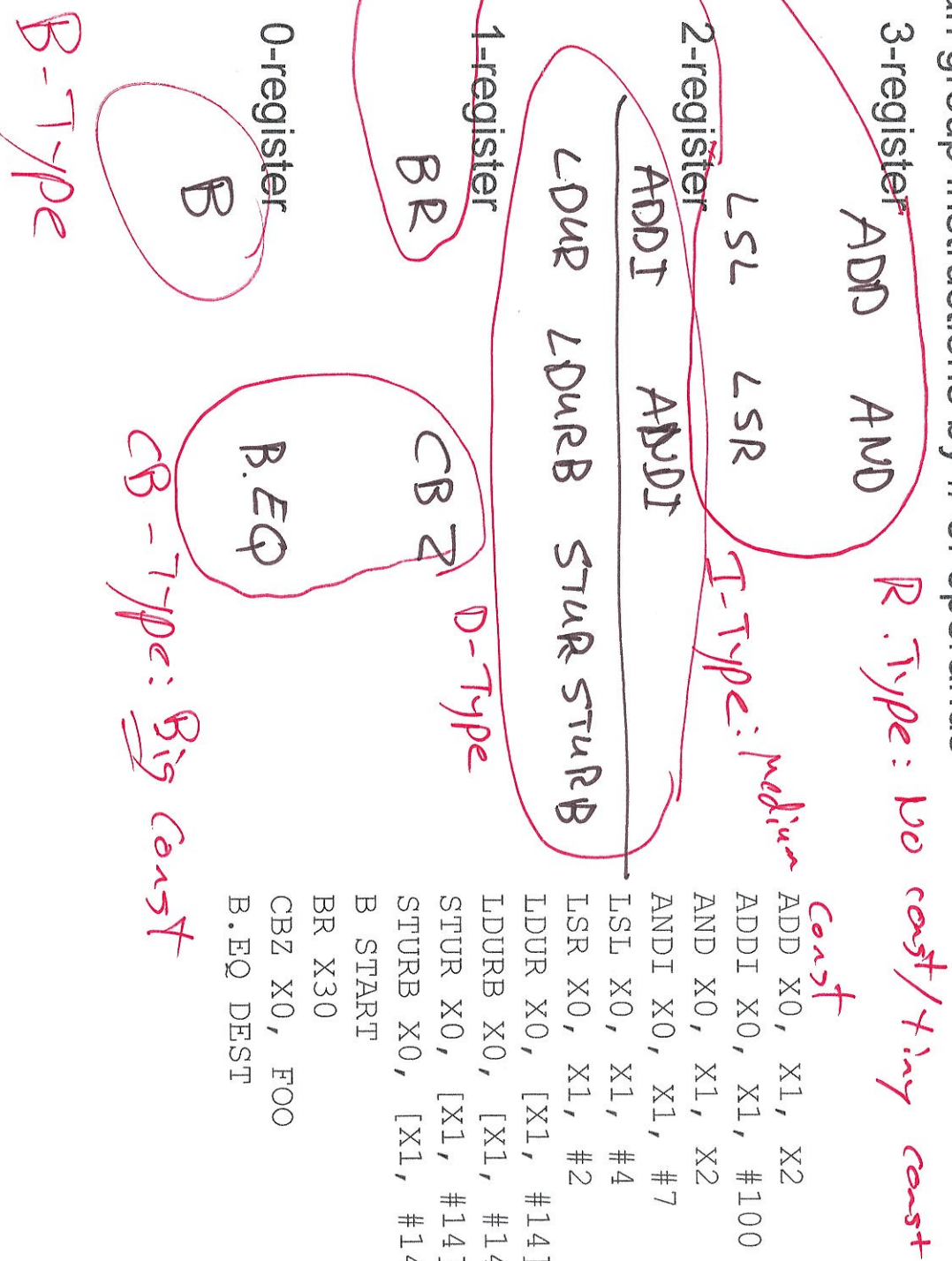
LOOP:
    LDURB X1, [X0, #0]
    CBZ X1, END +9
    CMPI X1, #97
    B.LT NEXT +5
    CMPI X1, #122
    B.GT NEXT +3
    SUBI X1, X1, #32
    STURB X1, [X0, #0]

NEXT:
    ADDI X0, X0, 1
    B LOOP -9

END:
```

Instruction Types

Can group instructions by # of operands



```

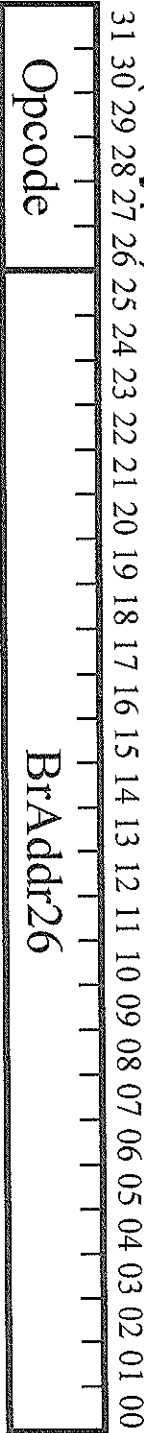
ADD X0, X1, X2
ADDI X0, X1, #100
AND X0, X1, X2
ANDI X0, X1, #7
LSL X0, X1, #4
LSR X0, X1, #2
LDUR X0, [X1, #14]
LDURB X0, [X1, #14]
STUR X0, [X1, #14]
STURB X0, [X1, #14]
B START
BR X30
CBZ X0, FOO
CBZQ DEST
  
```

Instruction Formats

All instructions encoded in 32 bits (operation + operands/immediates)

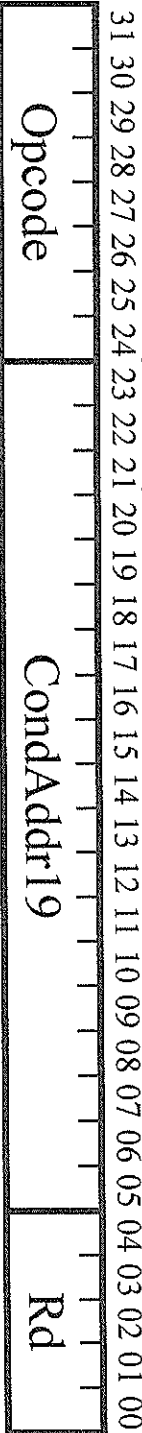
Branch (B-Type)

Instr[31:21] = 0A0-0BF



Conditional Branch (CB-Type)

Instr[31:21] = 2A0-2A7, 5A0-5AF



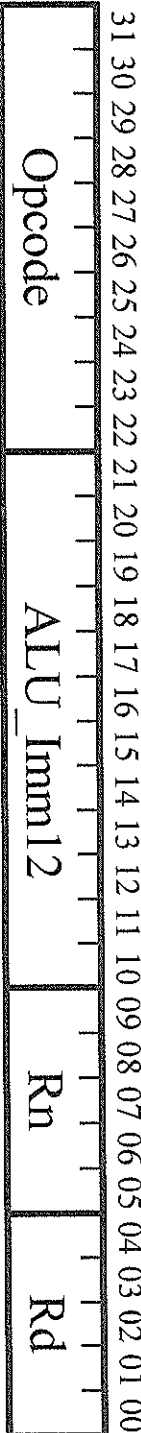
Register (R-Type)

Instr[31:21] = 450-458, 4D6-558, 650-658, 69A-758



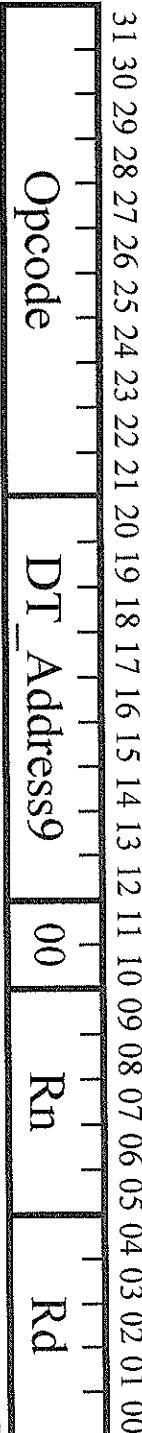
Immediate (I-Type)

Instr[31:21] = 488-491, 588-591, 688-691, 788-791



Memory (D-Type)

Instr[31:21] = 1C0-1C2, 7C0-7C2



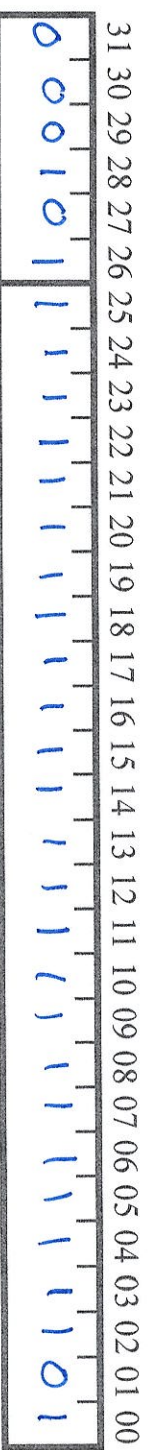
B-Type

Used for unconditional branches



0x05: B

$$B \text{ } -3 \quad // \quad PC = PC + 4 * -3$$



B: 05₁₆

- 3

CB-Type

Used for conditional branches

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Opcode	CondAddr19	Rd
--------	------------	----

Reg or Cond. Code

0x54: B.cond
0xB4: CBZ
0xB5: CBNZ

CBZ X12, -3 // if (X12==0) PC = PC + 4*-3

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

1011:0100	111111111111111101	01100
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CBZ B4 -3 X12

Condition Codes
0x00: EQ (==)
0x01: NE (!=)
0x0A: GE (>=)
0x0B: LT (<)
0x0C: GT (>)
0x0D: LE (<=)

B.LT -5 // if (lessThan) PC = PC + 4*-5

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0101:0100	1111111111111111011	01011
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B. 54 -5 .LT 0B

R-Type

Used for 3 register ALU operations and shift

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Opcode	Rm	SHAMT	Rn	Rd
--------	----	-------	----	----

Op2 Shift amount Op1 Dest
(0 for shift) (0 for non-shift)

0x450: AND
0x458: ADD
0x4D6: SDIV, shamt=02
0x4D8: MUL, shamt=1F

ADD X3, X5, X6 // X3 = X5+X6

0x550: ORR

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0x558: ADDS
0x650: EOR

1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

0x658: SUB
0x69A: LSR

ADD 458 X6 0 X5 X3

0x69B: LSL

LSL X10, X4, #6 // X10 = X4<<6

0x6B0: BR, rest all 0's but Rd

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0x750: ANDS
0x758: SUBS

1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

LSL = 69B 0 #6 X4 X10

I-Type

Used for 2 register & 1 constant ALU operations

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

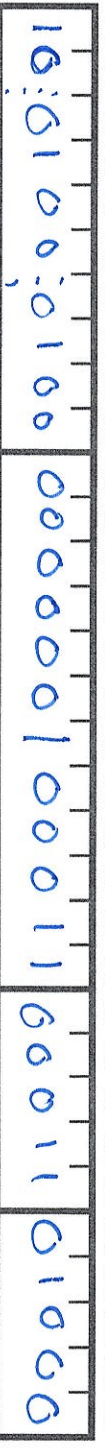


Constant - Op2 Op1 Dest

- 0x244: ADDI
- 0x248: ANDI
- 0x164: ADDIS
- 0x168: ORRI
- 0x344: SUBI
- 0x348: FORI
- 0x2C4: SUBIS
- 0x2C8: ANDIS

ADDI X8, X3, #35 // X8 = X3+35

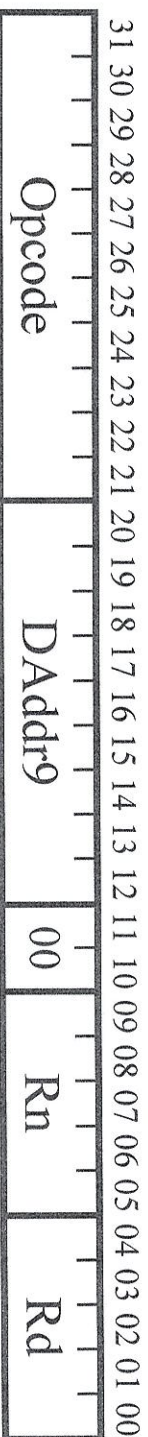
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00



ADDI 244 #35 X3 X8

D-Type

Used for memory accesses



Address Constant

Address Reg Target Reg

- 0x1C0: STURB
- 0x1C2: LDURB
- 0x7C0: STUR
- 0x7C2: LDUR

LDUR X6, [X15, #12] // X6 = Memory[X15+12]



LDUR 7C2 #12 0 X15 X6