THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

This exam paper must not be removed from the venue

Venue _____

Seat Number _____

Student Number |__|__|__|__|__|__|__|__|

Family Name _____

First Name _____

School of Information Technology and Electrical Engineering

SAMPLE MID-SEMESTER EXAMINATION #5

Semester One Mid-semester Examinations, 2020

CSSE2010/CSSE7201 Introduction to Computer Systems

This paper is for St Lucia Campus students.

Examination Duration: 60 minutes

Reading Time: 10 minutes

Exam Conditions:

This is an Open Book Examination

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

Calculators - Casio FX82 series or UQ approved (labelled)

Materials To Be Supplied To Students:

1 x Multiple Choice Answer Sheet

Instructions To Students:

Answer all questions on the supplied "True/False and Multiple Choice Answer Sheet".

Choose the answer which best answers the question or completes the statement. Correct answers will be awarded one mark. Incorrect, missing or multiple answers will be awarded zero marks.

Total number of questions for the paper: 25

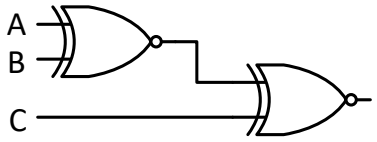
1. What is -75_{10} expressed in 8-bit excess-128 format?
   (a) 00110101
   (b) 01001011
   (c) 10110100
   (d) 10110101
   (e) 11001011

2. What is the minimum number of octal digits needed to represent the number $1ACED2010_{16}$?
   (a) 7
   (b) 9
   (c) 11
   (d) 12
   (e) None of the above

3. A 5-bit number in two's complement format can represent integers from
   (a) –32 to 31
   (b) –31 to 31
   (c) –16 to 15
   (d) –15 to 15
   (e) 0 to 31

4. Which of the following statements about binary number representations is FALSE?
   (a) Any 8-bit two's complement number can be converted to excess-128 representation by inverting the sign-bit
   (b) Any negative n-bit two's complement number can be converted to ones' complement representation by subtracting 1
   (c) Any negative n-bit ones' complement number can be converted to two's complement representation by adding 1
   (d) Any negative n-bit ones' complement number can be converted to signed-magnitude representation by inverting all bits except the sign-bit
   (e) None of the above

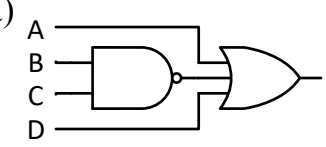
5. What function is implemented by the following circuit?

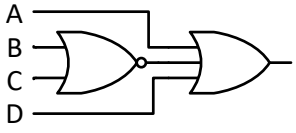


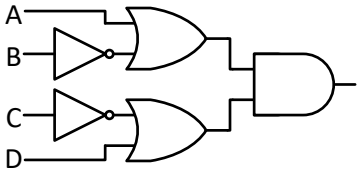
   (a) $\overline{A \oplus B} \oplus C$
   (b) $A \oplus B \oplus \overline{C}$
   (c) $\overline{A} \oplus \overline{B} \oplus \overline{C}$
   (d) $A \oplus B \oplus C$
   (e) None of the above

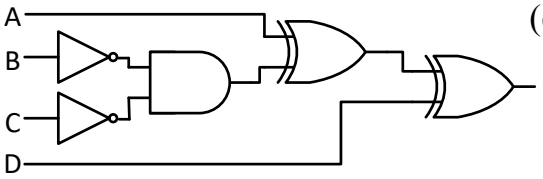
6. Which of the following logic functions is identical to $\overline{\overline{A.\overline{B}}.C}.(C + \overline{A}.B)$?
   (a) $\overline{A}.C + B.C$
   (b) $A.\overline{B}.C + \overline{A}.B.\overline{C}$
   (c) $A \oplus B \oplus C$
   (d) C
   (e) 0 (False)

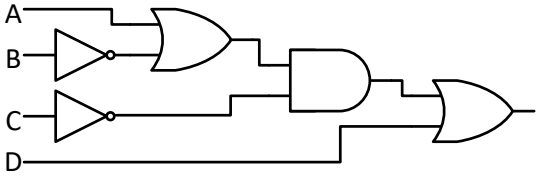
7. Which of the following logic circuits is an implementation of the function $A + \overline{B}\,.\,\overline{C} + D$?

(a) 

(b) 

(c) 

(d) 

(e) 

8. Which of the following truth tables is equivalent to the function

$X = A.(B.\overline{C} + \overline{\overline{A}.(B + \overline{C})})$

(a)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(b)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(c)

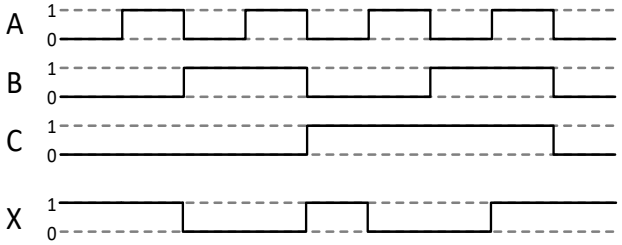
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(d)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(e) None of the above

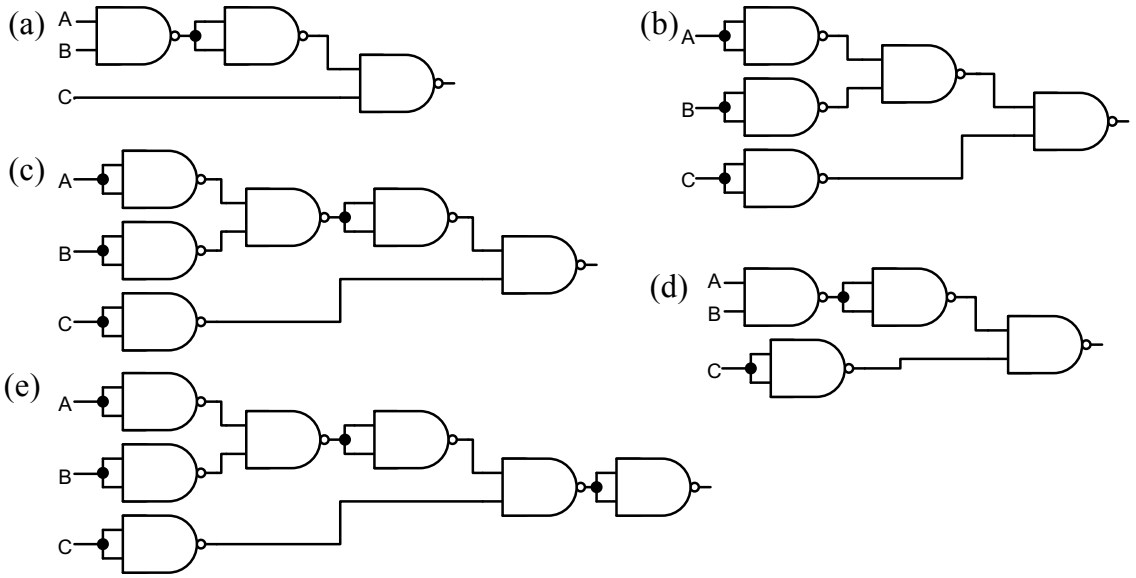
9. Which of the following expressions is NOT equivalent to the following timing diagram?



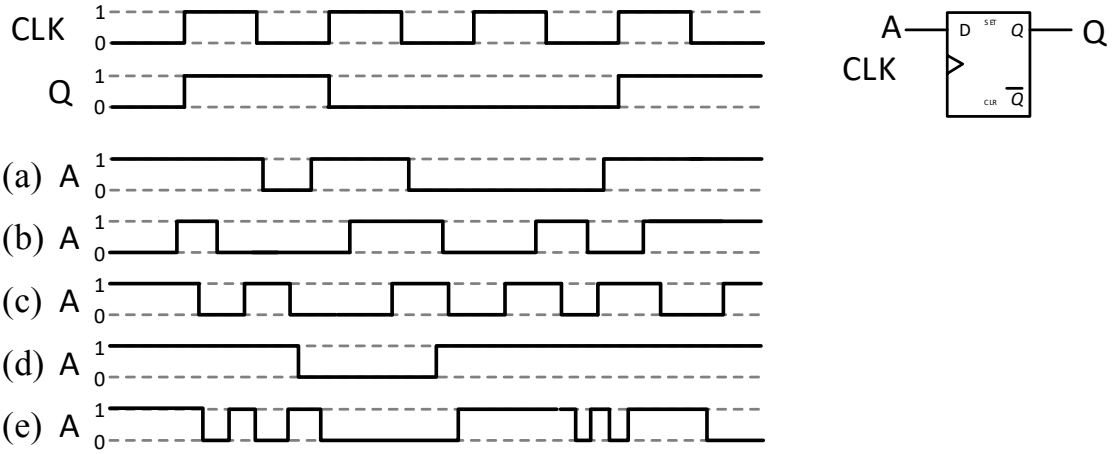
(a) $\overline{B}\,.\,(\overline{A} + \overline{C}) + A.B.C$
(b) $\overline{B}\,.\,\overline{C} + C.(\overline{A} \oplus B)$
(c) $\overline{A}\,.\,\overline{B} + A.(\overline{B} \oplus C)$
(d) $\overline{A}\,.\,\overline{B} + \overline{C}\,.\,\overline{B} + A.(B \oplus \overline{C})$
(e) None of the above

10. Which of the following is a sum-of-products expression equivalent to $(\overline{A} + B).\overline{(C + B.D)}$?
    (a) $\overline{A}.\overline{B}.\overline{C} + \overline{A}.\overline{C}.\overline{D} + B.\overline{C}.\overline{D}$
    (b) $\overline{A}.\overline{B}.\overline{C} + \overline{A}.\overline{C}.\overline{D}$
    (c) $\overline{A}.\overline{C} + B.\overline{C} + \overline{A}.\overline{B}.\overline{D}$
    (d) $\overline{A}.\overline{C}.\overline{BD} + B.\overline{C}.\overline{BD}$
    (e) None of the above

11. Which of the following implements a 3-input NOR gate ($\overline{A + B + C}$) using only 2-input NAND gates?



12. Consider the flip-flop circuit shown below and the associated CLK and output (Q) signals. Which timing diagram shows input (A) values over time which would have resulted in the given output (Q)?

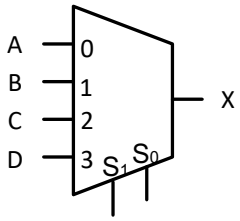


13. What is the result of adding the 7-bit two's complement numbers 1011001 and 0101111?
    (a) 0000000
    (b) 0001000
    (c) 1110110
    (d) 1110111
    (e) None of the above

14. Which of the following operations will result in overflow in 5-bit two's complement arithmetic?
    (a) 01000 + 01000
    (b) 11111 + 00001
    (c) 11000 + 01111
    (d) 11101 + 11010
    (e) None of the above

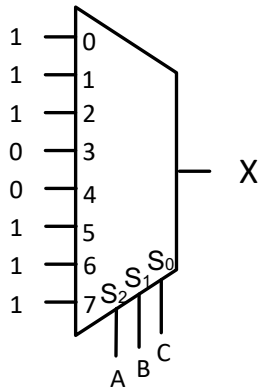
15. Consider the binary addition operation 110111 + 101001. Which of the following statements is true if the numbers are interpreted as two's complement?
    (a) The result is negative and no overflow occurs
    (b) The result should be negative but overflow occurs
    (c) The result is positive and no overflow occurs
    (d) The result is positive but overflow occurs
    (e) The result is zero

16. Consider the following multiplexer. What must the inputs A,B,C,D be so that the multiplexer implements the function $X = S_1 \oplus S_0 \oplus (G.S_1)$?



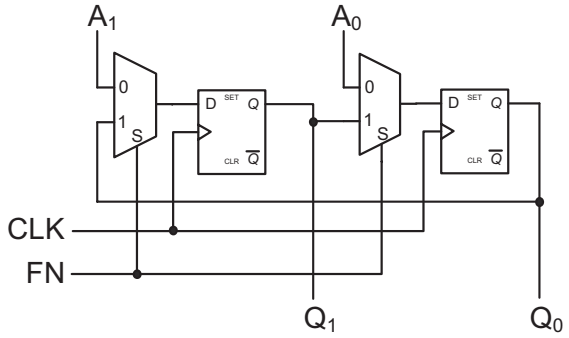
    (a) A= 1 B= 1 C= G D= $\overline{G}$
    (b) A= 0 B= 1 C= G D= $\overline{G}$
    (c) A= 1 B= 0 C= $\overline{G}$ D= G
    (d) A= 0 B= 1 C= $\overline{G}$ D= G
    (e) None of the above

17. Consider the following multiplexer. Which of the following statements is TRUE? (+ indicates the logical OR operation)



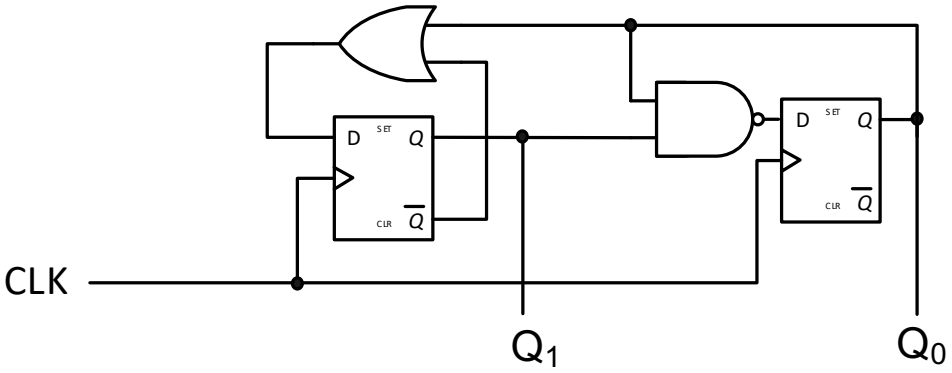
    (a) If A is 0, $X = \overline{B + C}$ If A is 1, $X = B.C$
    (b) If A is 0, $X = \overline{B.C}$ If A is 1, $X = \overline{B + C}$
    (c) If A is 0, $X = B + C$ If A is 1, $X = \overline{B.C}$
    (d) If A is 0, $X = \overline{B.C}$ If A is 1, $X = B + C$
    (e) None of the above

18. Consider the circuit below. If A_1 is 0 and A_0 is 1, what are the values of Q_1 and Q_0 after five rising clock edges if FN is 0 for two rising clock edges then 1 for three rising clock edges?



(a) $Q_1 = 0$ $Q_0 = 0$
(b) $Q_1 = 0$ $Q_0 = 1$
(c) $Q_1 = 1$ $Q_0 = 0$
(d) $Q_1 = 1$ $Q_0 = 1$
(e) Insufficient information is provided to determine the values

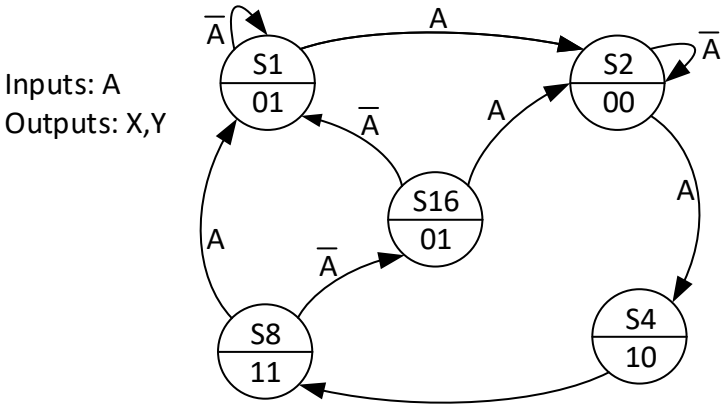
19. What sequence will the following synchronous counter count through, if it starts at $Q_1Q_0 = 00$?



(a) Q_1Q_0: 00 → 01 → 11 → 10 → 11 → …
(b) Q_1Q_0: 00 → 10 → 00 →…
(c) Q_1Q_0: 00 → 11 → 01 → 11 → …
(d) Q_1Q_0: 00 → 11 → 10 → 01 → 00 → …
(e) Q_1Q_0: 00 → 11 → 10 → 01 → 11 → …

20. What is the minimum number of flip-flops needed to implement a state machine which counts through the sequence 00000→00001→00011→11000→00001→… ?
(a) 2
(b) 3
(c) 4
(d) 5
(e) 32

21. Consider the state diagram below.



Which of the following is an equivalent state table?

(a)

Current State	Input (A)	Next State	Outputs (X,Y)
S1	0	S1	01
S1	1	S2	01
S2	0	S2	00
S2	1	S4	00
S4	0	S8	10
S4	1	S8	10
S8	0	S16	11
S8	1	S1	11
S16	0	S1	01
S16	1	S2	01

(b)

Current State	Input (A)	Next State	Outputs (X,Y)
S1	0	S1	01
S1	1	S2	01
S2	0	S2	00
S2	1	S4	00
S4	0	S8	10
S4	1	S8	10
S8	0	S1	11
S8	1	S16	11
S16	0	S1	01
S16	1	S2	01

(c)

Current State	Next State		Outputs (X,Y)
	A=0	A=1	
S1	S1	S2	01
S2	S2	S4	00
S4	S4	S8	10
S8	S16	S1	11
S16	S1	S2	01

(d)

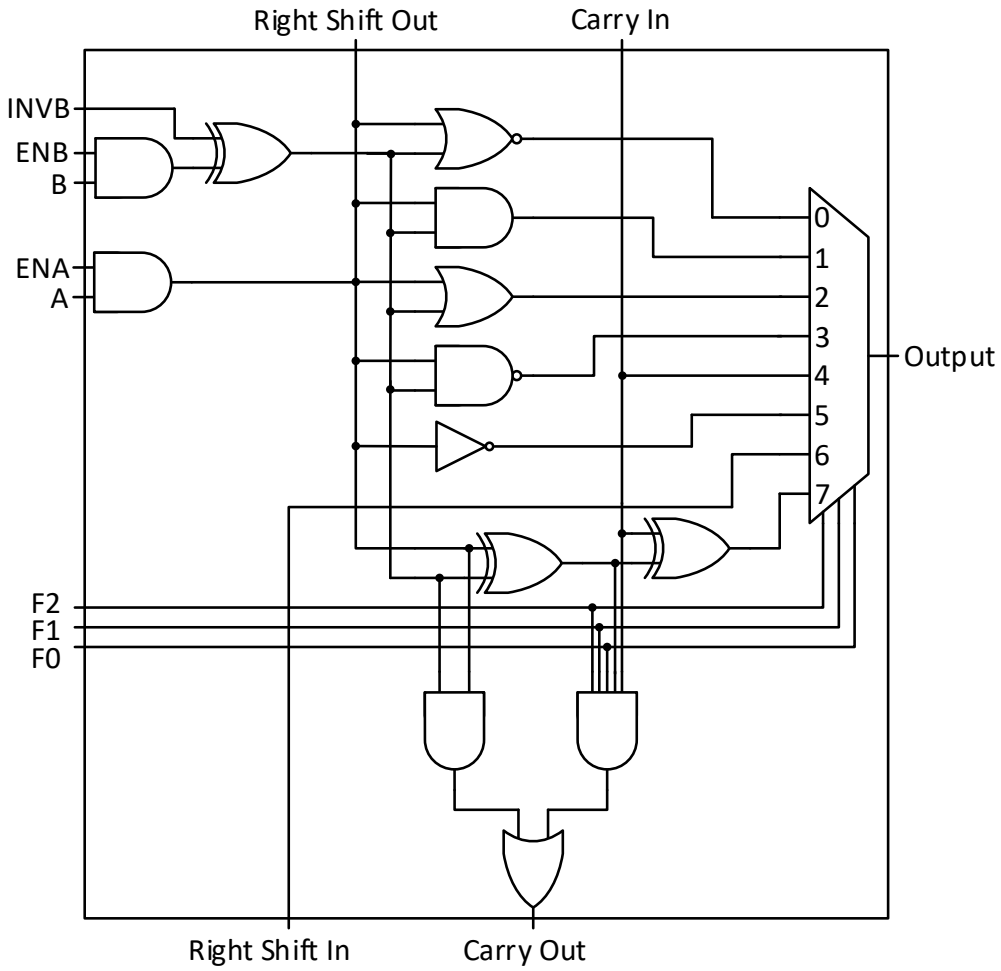
Current State	Next State		Outputs (X,Y)
	A=0	A=1	
S1	S1	S2	01
S2	S2	S4	00
S4	S8	S8	01
S8	S16	S1	11
S16	S1	S2	01

(e) None of the above

22. What is the minimum number of flip-flops needed to build the state machine shown in question 21?
    (a) 1
    (b) 2
    (c) 3
    (d) 4
    (e) 5

23. Consider the state machine represented by the state diagram in question 21 above. What sequence of states is traversed if the machine starts in state S1 and A goes through the sequence 110011 (i.e. two 1's followed by two 0's followed by two 1's)?
    (a) S1→S1→S2→S4→S8→S16→S2
    (b) S1→S2→S4→S8→S1→S2→S4
    (c) S1→S2→S2→S2→S4→S8→S16
    (d) S1→S2→S4→S8→S16→S2→S4
    (e) None of the above

24. Consider the ALU bit slice below.



For an ALU made up of 8 of the bit slices above, which of the following control input settings will result in the ALU output being $A \oplus B$? (The "Right Shift In" control input refers to that for the most significant bit; the "Carry in" control input refers to that for the least significant bit.)

(a) ENA = 1, ENB = 1, INVB = 0, $F_2 = 0$, $F_1 = 0$, $F_0 = 0$, Right Shift In = 0, Carry in = 0
(b) ENA = 1, ENB = 1, INVB = 1, $F_2 = 0$, $F_1 = 0$, $F_0 = 0$, Right Shift In = 0, Carry in = 0
(c) ENA = 1, ENB = 1, INVB = 1, $F_2 = 0$, $F_1 = 1$, $F_0 = 0$, Right Shift In = 0, Carry in = 0
(d) ENA = 1, ENB = 1, INVB = 0, $F_2 = 1$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 0
(e) None of the above

25. For the ALU in question 24, which of the following control input settings will <u>NOT</u> result in the ALU output being the constant value –1 (negative one)?

(a) ENA = 0, ENB = 0, INVB = 0, $F_2 = 0$, $F_1 = 0$, $F_0 = 0$, Right Shift In = 1, Carry in = 0
(b) ENA = 0, ENB = 0, INVB = 1, $F_2 = 0$, $F_1 = 1$, $F_0 = 0$, Right Shift In = 0, Carry in = 1
(c) ENA = 1, ENB = 0, INVB = 0, $F_2 = 0$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 1
(d) ENA = 1, ENB = 1, INVB = 1, $F_2 = 0$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 0
(e) ENA = 0, ENB = 1, INVB = 1, $F_2 = 1$, $F_1 = 0$, $F_0 = 1$, Right Shift In = 0, Carry in = 1