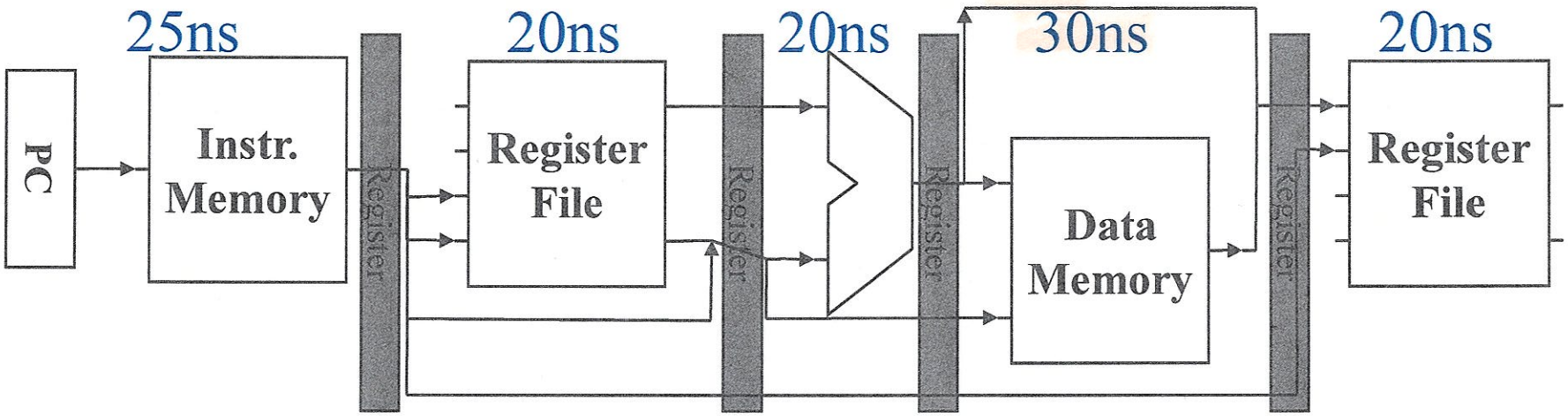
Review Problem 29

- The pipelined CPU has the stage delays shown
  - Is it better to speed up the ALU by 10ns, or the Data Memory by 2ns?

- Does you answer change for a single-cycle CPU?

Yes. This speeds up longest path.



Solution #3: Branch Delay Slot

Redefine branches: Instruction directly after branch always executed

Instruction after branch is the **delay slot**

Compiler/assembler **fills** the delay slot

Ex #1

```
ADD X1, X0, X4
CBZ X2, FOO
```

ADD X1, X0, X4

No waste

Ex #2

```
SUB X2, X0, X3
ADD X1, X0, X4
CBZ X1, FOO
```

SUB X2, X0, X3

Ex #3

```
ADD X1, X0, X4
CBZ X1, FOO
   ADD X1, X3, X3
   …
FOO:
   ADD X1, X2, X0
```

either one, pick the one most likely to be useful given CBZ T/NT odds

Assume 50% taken branch

waste ½ cycle

Ex #4

```
ADD X1, X0, X4
CBZ X1, FOO
```

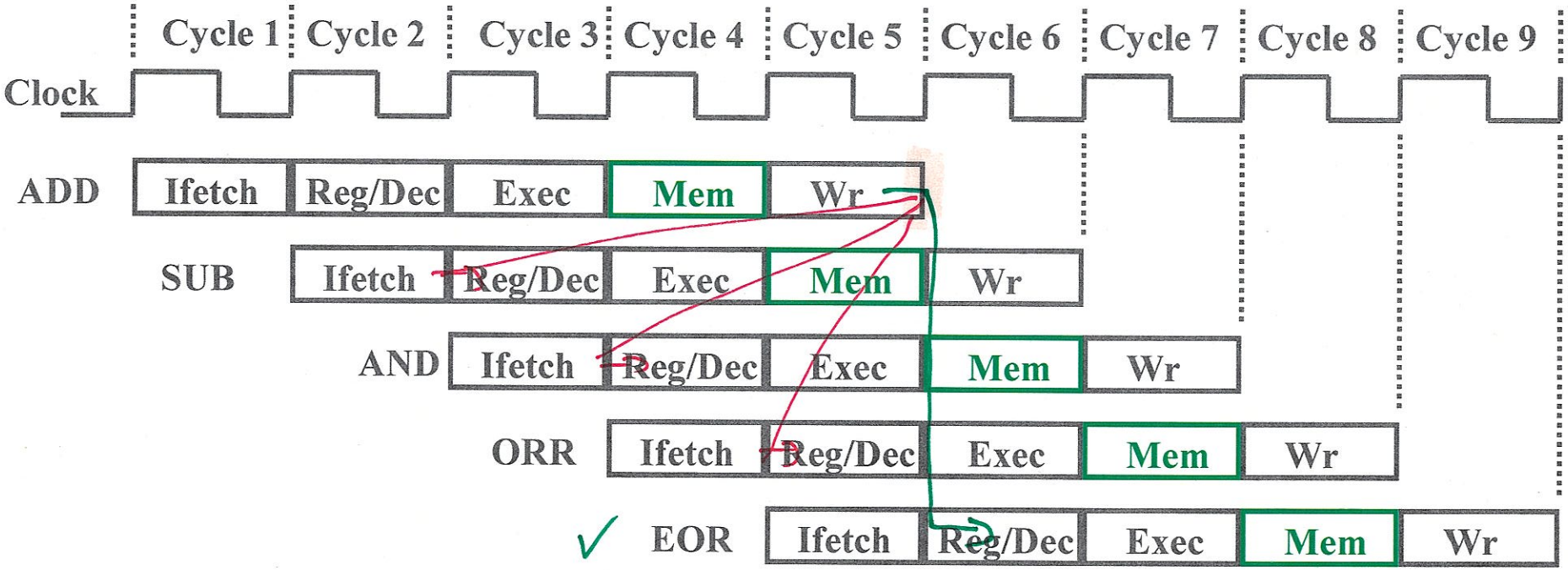
ADD X31, X31, X31

waste 1 cycle

Data Hazards

Consider the following code:

ADD X0, X1, X2
SUB X3, X0, X4
AND X5, X0, X6
ORR X7, X0, X8
EOR X9, X0, X10

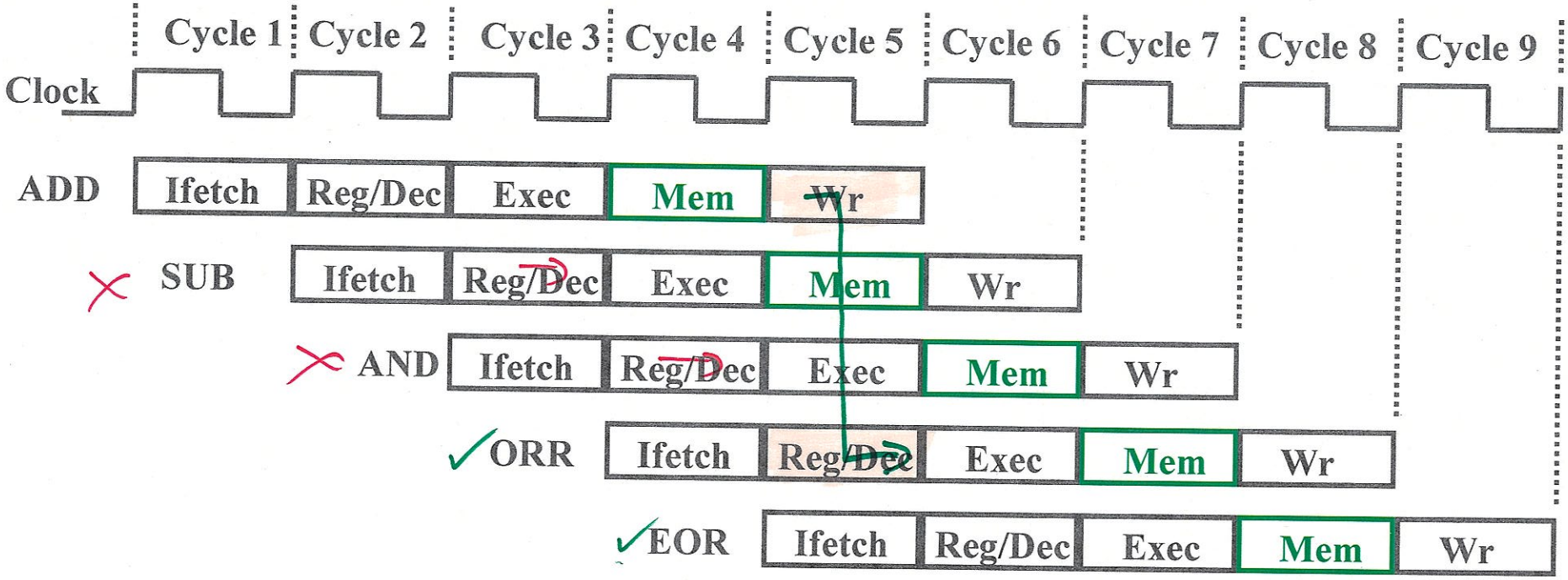


Design Register File Carefully

HACK!! Lab#4 invert the clock to the reg file

What if reads see value after write during the same cycle?

ADD X0, X1, X2
SUB X3, X0, X4
AND X5, X0, X6
ORR X7, X0, X8
EOR X9, X0, X10



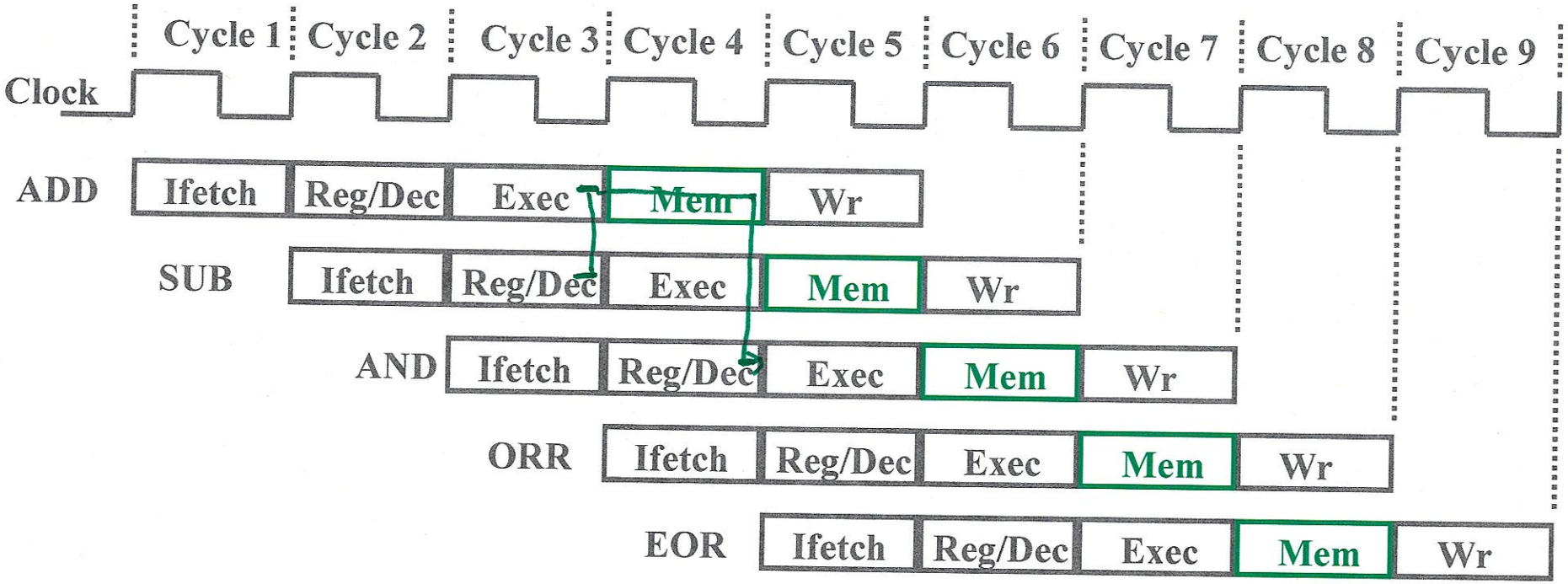
Forwarding

Add logic to pass last two values from ALU output to ALU input(s) as needed

Forward the ALU output to later instructions

ADD X0, X1, X2
SUB X3, X0, X4
AND X5, X0, X6
ORR X7, X0, X8
EOR X9, X0, X10

passing notes in the lab



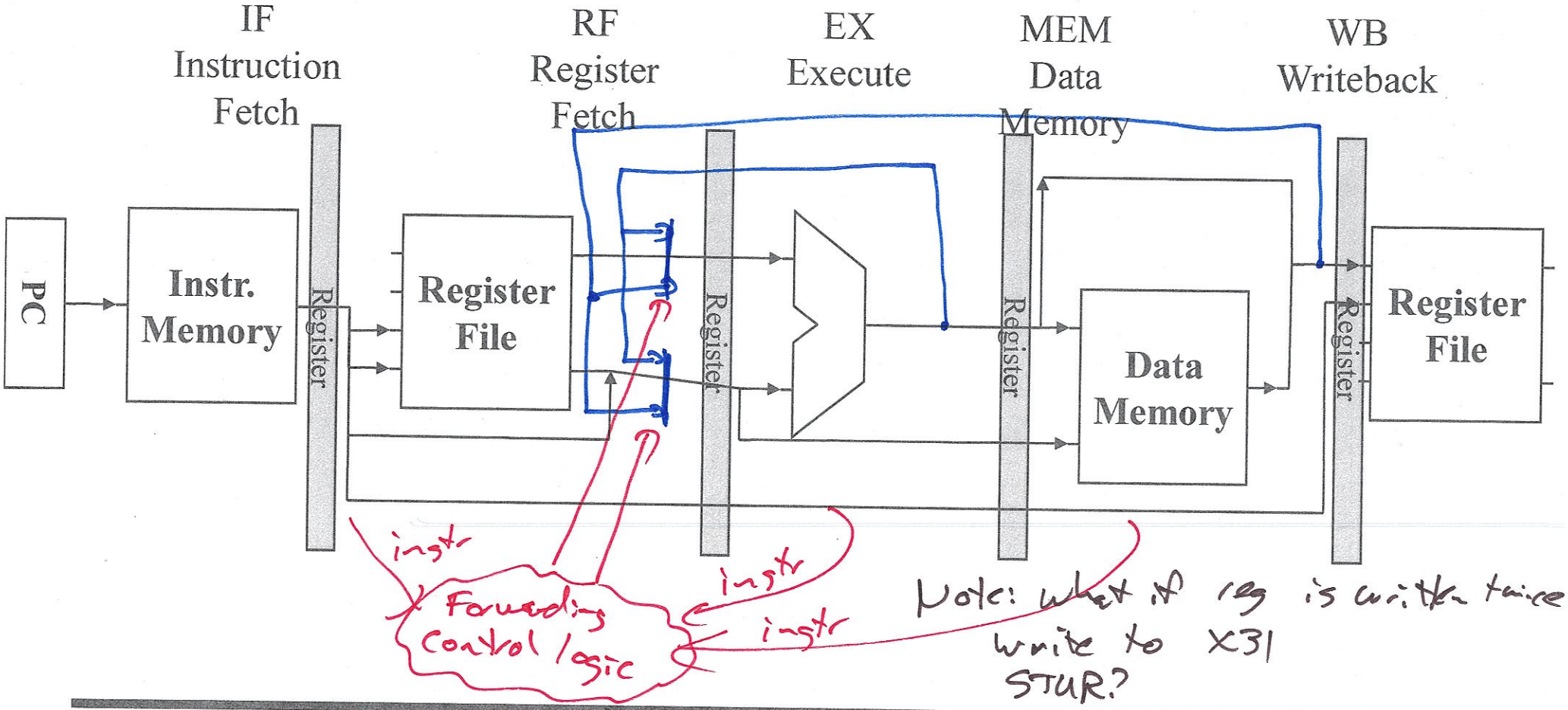
Note: Use THIS one, not the book one.

Forwarding (cont.)

Requires values from last two ALU operations.

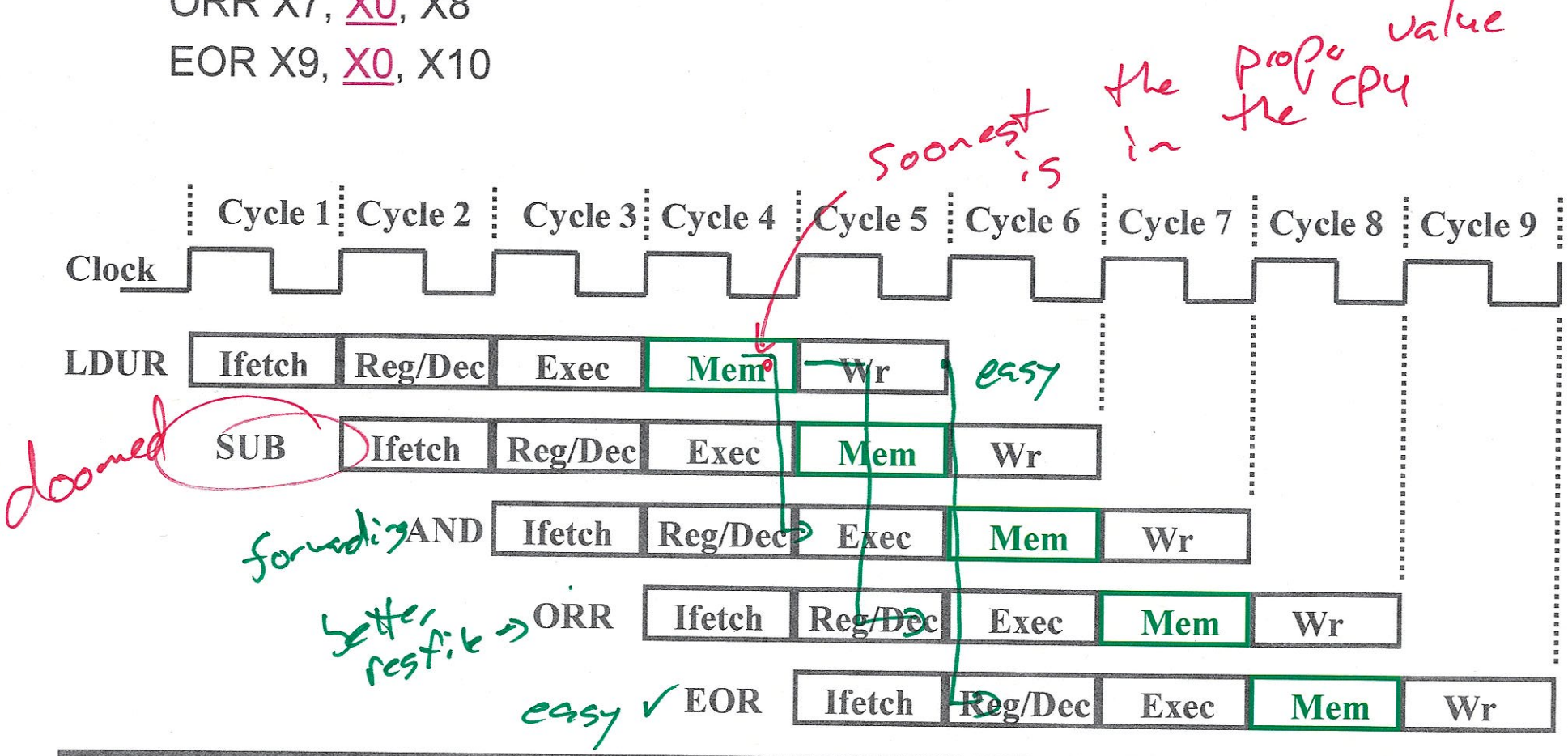
Remember destination register for operation.

Compare sources of current instruction to destinations of previous 2.



Data Hazards on Loads

LDUR X0, [X31, 0]
SUB X3, X0, X4
AND X5, X0, X6
ORR X7, X0, X8
EOR X9, X0, X10



Data Hazards on Loads (cont.)

Solution:

- Use same forwarding hardware & register file for hazards 2+ cycles later
- Force compiler to not allow register reads within a cycle of load
  - Fill delay slot, or insert no-op.

Reminder: Delay slot means "CPU is busted, programmer must deal with it!

Load delay slot: instr right after a load cannot read the load's targ register.

Branch delay slot: instr right after a branch always executes.