THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

This exam paper must not be removed from the venue

Venue _____

Seat Number _____

Student Number |__|__|__|__|__|__|__|__|

Family Name _____

First Name _____

School of Information Technology and Electrical Engineering

SAMPLE MID-SEMESTER EXAMINATION #2

Semester One Mid-semester Examinations, 2020

CSSE2010/CSSE7201 Introduction to Computer Systems

This paper is for St Lucia Campus students.

Examination Duration: 60 minutes

Reading Time: 10 minutes

Exam Conditions:

This is an Open Book Examination

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

Calculators - Casio FX82 series or UQ approved (labelled)

Materials To Be Supplied To Students:

1 x Multiple Choice Answer Sheet

Instructions To Students:

Answer all questions on the supplied "True/False and Multiple Choice Answer Sheet".

Choose the answer which best answers the question or completes the statement. Correct answers will be awarded one mark. Incorrect, missing or multiple answers will be awarded zero marks.

Total number of questions for the paper: 25

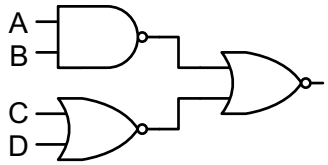
1. What is -27_{10} expressed in 7-bit two's complement format?
   (a) 0011011
   (b) 1011011
   (c) 1100100
   (d) 1100101
   (e) 1100110

2. 110_8 is equal to
   (a) 10001000_2
   (b) 68_{10}
   (c) 0x48
   (d) 6_{10}
   (e) None of the above

3. A 10-bit binary number in excess-512 representation can represent integers from
   (a) -512 to 511
   (b) -512 to 512
   (c) -511 to 511
   (d) -511 to 512
   (e) None of the above

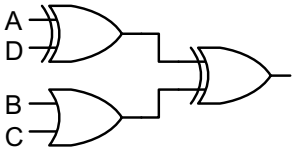
4. How can any n-bit binary number in one's complement representation be converted to excess-2^{n-1} representation?
   (a) By flipping the most-significant bit and then adding 1
   (b) By flipping the most-significant bit and then adding the value of the most-significant bit
   (c) By adding the value of the most-significant bit and then flipping the most-significant bit
   (d) By adding the value of the most-significant bit and flipping all the bits
   (e) By flipping all the bits except the most-significant bit

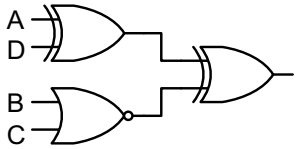
5. What function is implemented by the following circuit?

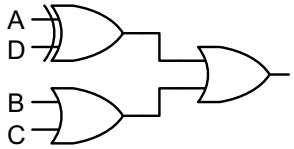


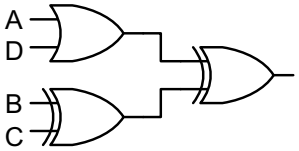
   (a) $\overline{(\overline{A.B})} + \overline{(\overline{C+D})}$
   (b) $\overline{\overline{(\overline{A.B})} + \overline{(\overline{C+D})}}$
   (c) $\overline{\overline{(\bar{A}.\bar{B})} + \overline{(\overline{C+D})}}$
   (d) $\overline{(\overline{A.B})} \oplus \overline{(\overline{C+D})}$
   (e) $\overline{(\overline{A.B})} \oplus (C \oplus D)$

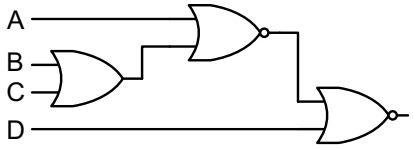
6. Which of the following circuits implements the function $A \oplus (B + C) \oplus D$

(a)


(b)


(c)


(d)


(e)


7. Which of the following logic functions is equivalent to $\overline{(A + B.\bar{C}).(\overline{\bar{A} + B})}$
   (a) $\bar{A} + B$
   (b) $\bar{A} + C + B$
   (c) $A.\bar{B}$
   (d) $\bar{A}.C + B$
   (e) None of the above

8. What is the truth table corresponding to $= \bar{A} \oplus \bar{B} \oplus \bar{C}$?

(a)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(c)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(d)

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(e)

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

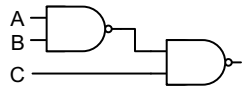
9. Consider the logic function represented by the following truth table:

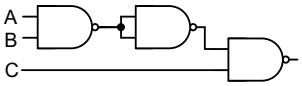
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

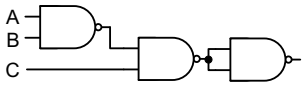
   Which of the following expressions is equivalent to the function represented by this table?
   (a) $\bar{A}.B + A.C$
   (b) $A.C + (B + C)$
   (c) $\bar{A}.B + C$
   (d) $\bar{A}.B + B.C + \bar{A}.C$
   (e) None of the above

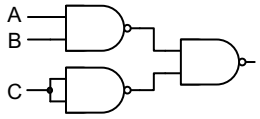
10. Which of the following logic functions is identical to $\overline{A} \oplus \overline{B}$?
   (a) $A.\overline{B} + \overline{A}.B$
   (b) $\overline{A}.\overline{B} + \overline{B}.\overline{A}$
   (c) $\overline{A} + \overline{B}$
   (d) $\overline{A \oplus B}$
   (e) None of the above

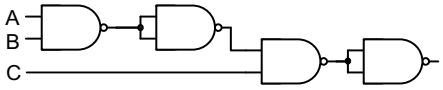
11. Which of the following implements a 3-input NAND gate ($\overline{A.B.C}$) using only 2-input NAND gates?

(a) 

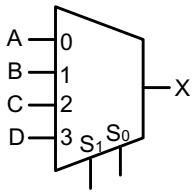
(b) 

(c) 

(d) 

(e) 

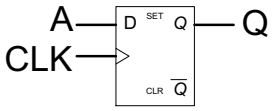
12. Consider the following multiplexer. What must the inputs A,B,C,D be so that the multiplexer implements the function $X = S_0 + (S_1 \oplus G)$?

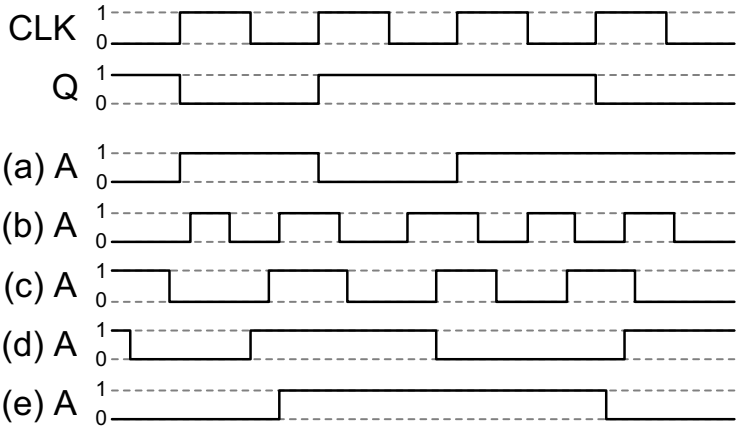


(a) A=1 B=G C=1 D=$\bar{G}$
(b) A=G B=$\bar{G}$ C=1 D=1
(c) A=$\bar{G}$ B=1 C=G D=1
(d) A=G B=1 C=$\bar{G}$ D=1
(e) None of the above

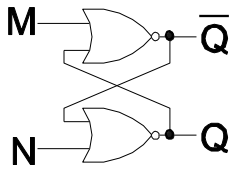
13. What is the result of adding the 6-bit two's complement numbers 101111 and 101001?
(a) 010000
(b) 010111
(c) 011000
(d) 111000
(e) None of the above

14. Consider the flip-flop circuit shown below and the associated CLK and output (Q) signals. Which timing diagram shows input (A) values over time which would have resulted in the given output (Q).





15. Which truth table correctly captures the behaviour of the following latch circuit?



(a)

M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	0	0

(b)

M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	1	1

(c)

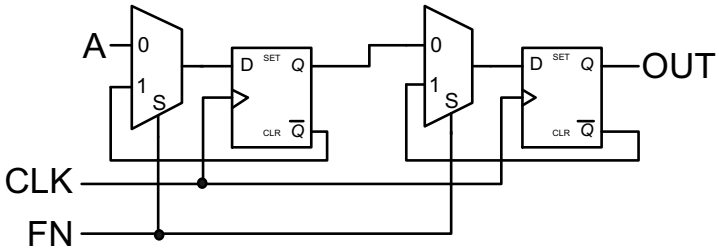
M	N	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

(d)

M	N	Q	$\overline{Q}$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

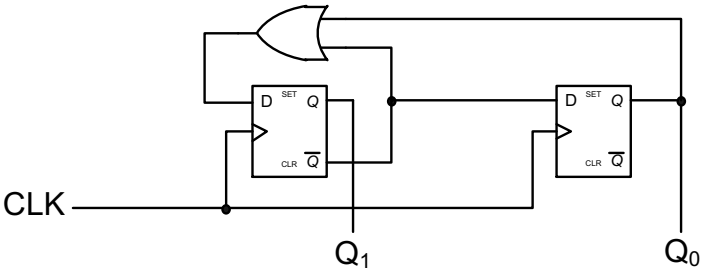
(e) None of the above

16. Which of the following statements about this shift register circuit is false?



(a) If FN is 0, the value of A will be transferred to OUT after two rising clock edges
(b) If FN is 1, OUT will toggle on each rising clock edge
(c) If FN is 0, data is shifted to the right on each rising clock edge
(d) If FN is 1, the value of A is irrelevant
(e) All of the above are true

17. What sequence will the following synchronous counter count through, if it starts at $Q_1Q_0 = 00$?



(a) Q_1Q_0: 00 → 01 → 11 → 10 → 10 → …
(b) Q_1Q_0: 00 → 01 → 11 → 00 → …
(c) Q_1Q_0: 00 → 11 → 01 → 00 → …
(d) Q_1Q_0: 00 → 11 → 10 → 00 → …
(e) None of the above

18. Which of the following operations will result in an overflow in 4-bit two's complement arithmetic?
(a) 0111+0111
(b) 1111+1111
(c) 1010+0110
(d) All of the above result in overflow
(e) None of the above

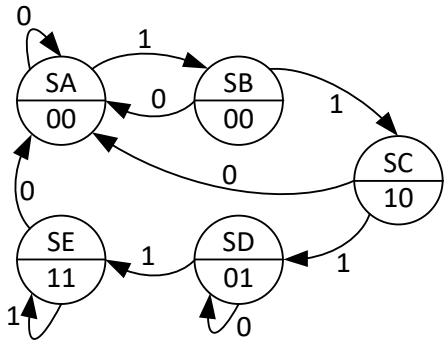
19. Consider the binary addition operation 1011 + 1111. Which of the following statements is true if the numbers are interpreted as two's complement?
    (a) The result is negative and no overflow occurs
    (b) The result should be negative but overflow occurs
    (c) The result is positive and no overflow occurs
    (d) The result should be positive but overflow occurs
    (e) The result is zero

20. Consider the following state table:

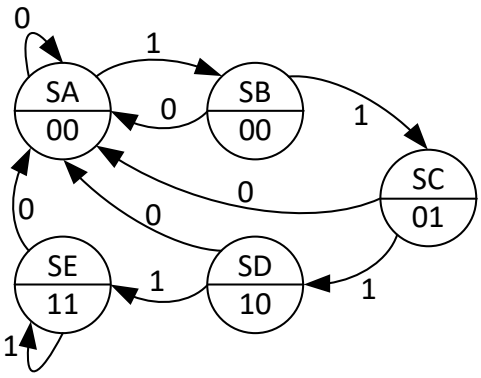
Current State	Next State		Outputs (X,Y)
	A=0	A=1	
SA	SA	SB	0 0
SB	SA	SC	0 0
SC	SA	SD	0 1
SD	SD	SE	1 0
SE	SA	SE	1 1

Which of the following state diagrams is an equivalent representation of this state table? (Input: A, Outputs: XY)

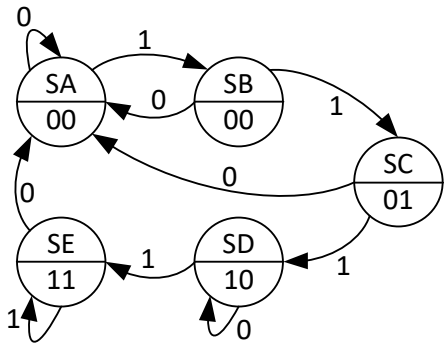
(a)



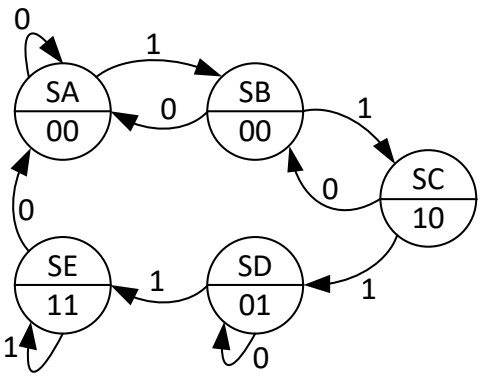
(b)



(c)



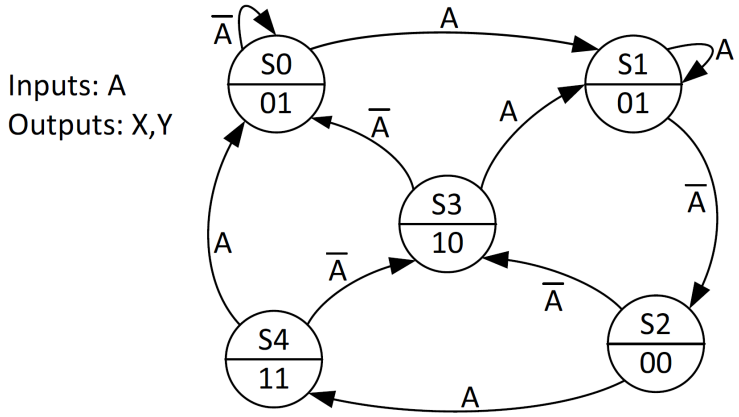
(d)



(e) None of the above

21. Consider the state machine represented by the state table in question 20 above. What is the minimum number of flip-flops needed to implement this state machine?
    (a) 2
    (b) 3
    (c) 4
    (d) 5
    (e) 7

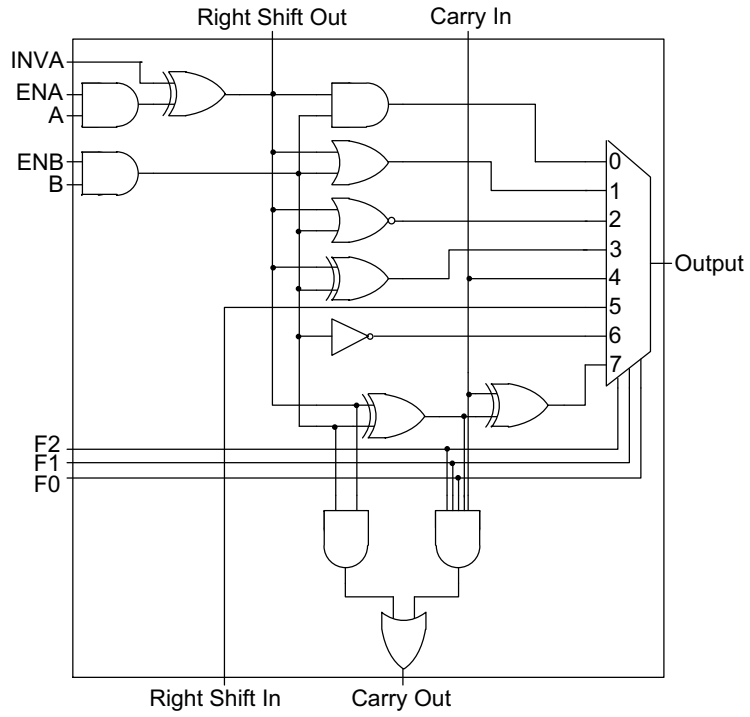
22. Consider the state machine represented by the state diagram below:



What sequence of states is traversed if the machine starts in state S0 and A goes through the sequence 11110000 (i.e. four 1's followed by four 0's)?

(a) S0→S1→S1→S1→S1→S2→S3→S0→S0
(b) S0→S1→S3→S1→S3→S0→S0→S0→S0
(c) S0→S1→S1→S1→S2→S3→S2→S0→S0
(d) S0→S1→S1→S1→S1→S2→S4→S3→S0
(e) None of the above

23. Consider the ALU bit slice below (not the same as seen previously).



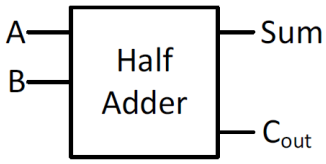
For an ALU made up of 8 of the bit slices above, which of the following control input settings will result in the ALU output being $\overline{A + B}$ (bitwise)? (The "Right Shift In" control input refers to that for the most significant bit; the "Carry in" control input refers to that for the least significant bit.)

(a) ENA=**1** ENB=**1** INVA=**0** F_2=**0** F_1=**0** F_0=**1** Right Shift In=**1** Carry in=**1**
(b) ENA=**1** ENB=**1** INVA=**0** F_2=**0** F_1=**1** F_0=**0** Right Shift In=**1** Carry in=**1**
(c) ENA=**1** ENB=**1** INVA=**1** F_2=**0** F_1=**0** F_0=**1** Right Shift In=**1** Carry in=**1**
(d) ENA=**1** ENB=**1** INVA=**1** F_2=**0** F_1=**1** F_0=**0** Right Shift In=**1** Carry in=**1**
(e) None of the above

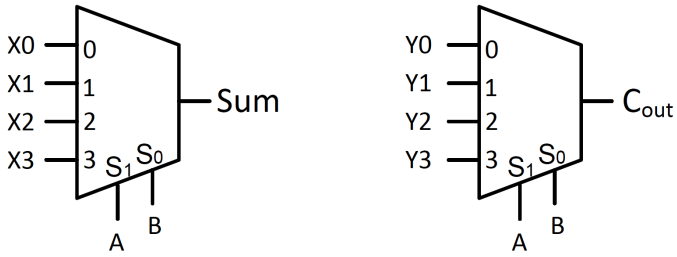
24. For an ALU made up of 8 of the bit slices shown in question 23 above, which of the following control input settings will **NOT** result in the ALU output being $\bar{B}$ (bitwise)?

    (a) ENA=**0** ENB=**1** INVA=**0** F_2=**0** F_1=**1** F_0=**0** Right Shift In=**0** Carry in=**0**
    (b) ENA=**0** ENB=**1** INVA=**1** F_2=**0** F_1=**1** F_0=**1** Right Shift In=**0** Carry in=**0**
    (c) ENA=**0** ENB=**1** INVA=**1** F_2=**1** F_1=**1** F_0=**0** Right Shift In=**0** Carry in=**0**
    (d) ENA=**0** ENB=**1** INVA=**1** F_2=**1** F_1=**1** F_0=**1** Right Shift In=**0** Carry in=**0**
    (e) All of the above result in the ALU output being $\bar{B}$ (bitwise)

25. Consider the half-adder shown below:



In the multiplexer circuit below, what values do the multiplexer inputs X0,X1,X2,X3 and Y0,Y1,Y2,Y3 need to take on in order for the circuit to implement a half-adder?



(a)

X0	**0**
X1	**0**
X2	**0**
X3	**1**

Y0	**0**
Y1	**1**
Y2	**1**
Y3	**0**

(b)

X0	**0**
X1	**1**
X2	**1**
X3	**0**

Y0	**0**
Y1	**0**
Y2	**1**
Y3	**1**

(c)

X0	**0**
X1	**1**
X2	**1**
X3	**0**

Y0	**0**
Y1	**0**
Y2	**0**
Y3	**1**

(d)

X0	**0**
X1	**1**
X2	**1**
X3	**0**

Y0	**1**
Y1	**0**
Y2	**0**
Y3	**0**

(e) None of the above

END OF PAPER