

Introduction to Embedded Systems

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Exercise 2 – Data Buses

Overview

- ▶ **Basics**
- ▶ **Hamming Code**
- ▶ **I²C**
- ▶ **Profibus**

Basics

Task 1: a) – c)



Task 1: a)

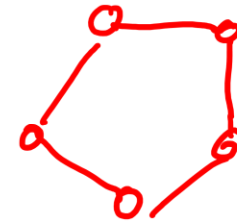
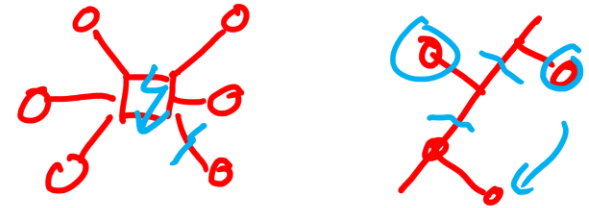
a) Name two advantages that the **star topology** has over the **bus topology**.

Adv.

- no collision
- no implicit broadcast
- only one single point of failure
- multiple sender at the same time

Disadv.

- we have a single point of failure
 - more wiring
 - we need a central station
- } overall more expensive



Task 1: b)

=> avoid long sequences of 1s

b) Use the 4B/5B table to encode the message 000000111111.
 $0 \quad 3 \quad 15 = 7$

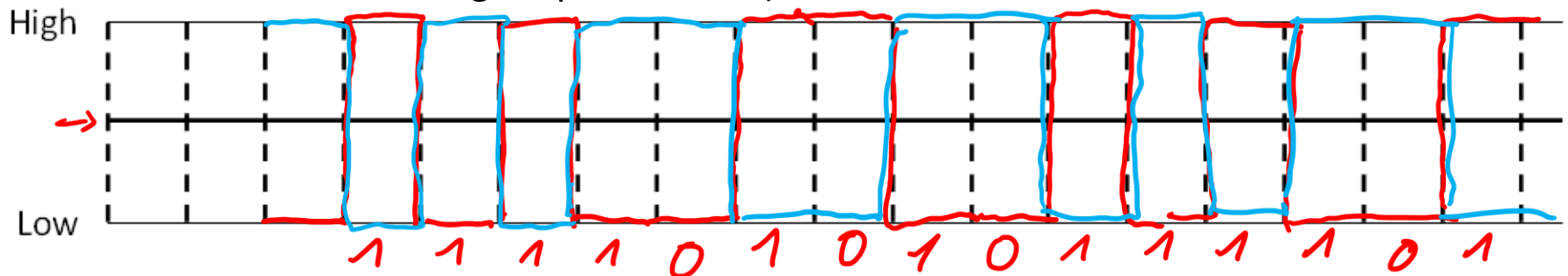
Name	4B	5B	Name	4B	5B	Name	5B	Desc
0	0000	11110	8	1000	10010	Q	00000	Quiet
1	0001	01001	9	1001	10011	I	11111	Idle
2	0010	10100	A	1010	10110	J	11000	Start #1
3	0011	10101	B	1011	10111	K	10001	Start #2
4	0100	01010	C	1100	11010	T	01101	End
5	0101	01011	D	1101	11011	R	00111	Reset
6	0110	01110	E	1110	11100	S	11001	Set
7	0111	01111	F	1111	11101	H	00100	Halt

11110 | 10101 | 11101

=> provided in the exam $\frac{4}{5}$

=> 80% of data rate

Then draw the signal diagram using **Differential NRZI** (Differential NRZ with inverted semantics: a level change represents a 1).

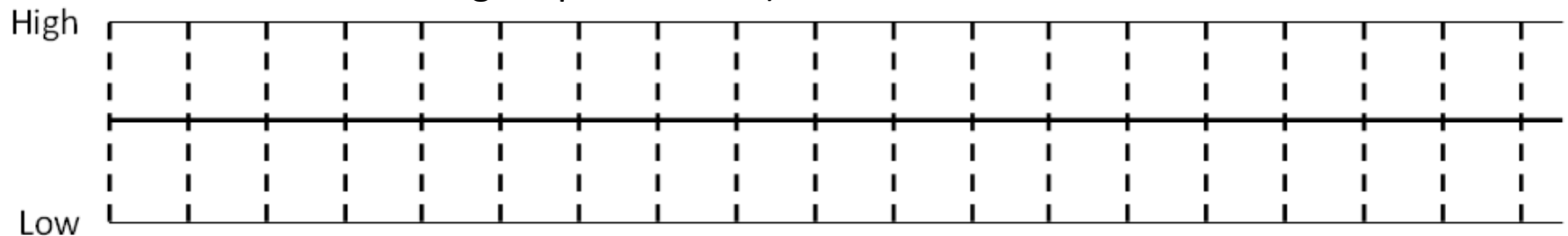


Task 1: b)

b) Use the 4B/5B table to encode the message **000000111111**.

Name	4B	5B	Name	4B	5B	Name	5B	Desc
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3	0011	10101	B	1011	10111	K	10001	Start #2
4	0100	01010	C	1100	11010	T	01101	End
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6	0110	01110	E	1110	11100	S	11001	Set
7	0111	01111	F	1111	11101	H	00100	Halt

Then draw the signal diagram using **Differential NRZI** (Differential NRZ with inverted semantics: a level change represents a 1).



Task 1: c)

c) What are the names of the two sublayers of **Layer 2** (OSI-Model)? What are their tasks?

Medium Access Control

- defines how/when participants ^{send via} access the communication medium

↳ - Freq. DMA

- Time - Hybrid
- Code

↳ CSMA → CD
↳ CR

Logical Link Control

- defines frame format
- provide flow control
- error detection/correction
- defines IDs/addresses

7 Application

6 Presentation

5 Session

4 Transport

3 Network

2 Data Link

1 Physical

Hamming-Code

Task 2: a) – b)



Task 2: a)

a) Calculate the even parity Hamming code of the following bit sequence: 11001110

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Value	?	?	1	?	1	0	0	?	1	1	1	0		
p_1	0		1		1		0		1		1			
p_2		1	1			0	0			1	1			
p_4				1	1	0	0					0		
p_8								1	1	1	1	0		
	0	1	1	1	1	0	0	1	1	1	1	0		

Task 2: b)

b) Correct and extract the 11 bit data sequence from this Hamming code protected sequence (even parity): 100100101100011

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Value	1	0	0	1	0	0	1	0	1	1	0	0	0 1	1	1
p_1	<u>1</u>		0		0		<u>1</u>		<u>1</u>		0		0 1		<u>1</u>
p_2		0	0			0	<u>1</u>			<u>1</u>	0			<u>1</u>	<u>1</u>
p_4				<u>1</u>	0	0	<u>1</u>					0	0 1	<u>1</u>	<u>1</u>
p_8								0	<u>1</u>	<u>1</u>	0	0	0 1	<u>1</u>	<u>1</u>

$\Rightarrow 00011100011$

- One error correction

- two error detection

$$1 + 4 + 8 = \underline{13}$$

Inter-Integrated Circuit

Task 3: a) - e)

I^2C

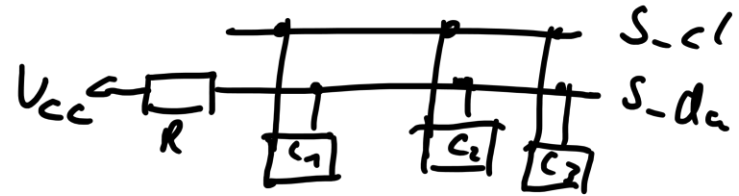


Task 3: a) – c)

a) What topology does I²C use?

Bus-Topology

b) What does Wired-AND mean?



a zero is dominant on
the bus

c) What is the basic MAC concept? Why are there no collisions when multiple senders start at the same time?

- Master/Slave

- Multiple Master

↳ CSMA/CR with Wired-AND

Task 3: d)

d) Use a block scheme to depict the following communication: **A** sends three participants **B**, **C** and **D** a data byte each. After **A** sent the third data byte, it starts **querying** **B**, **C** and **D** for a one byte response. Indicate who controls the data line for each block.

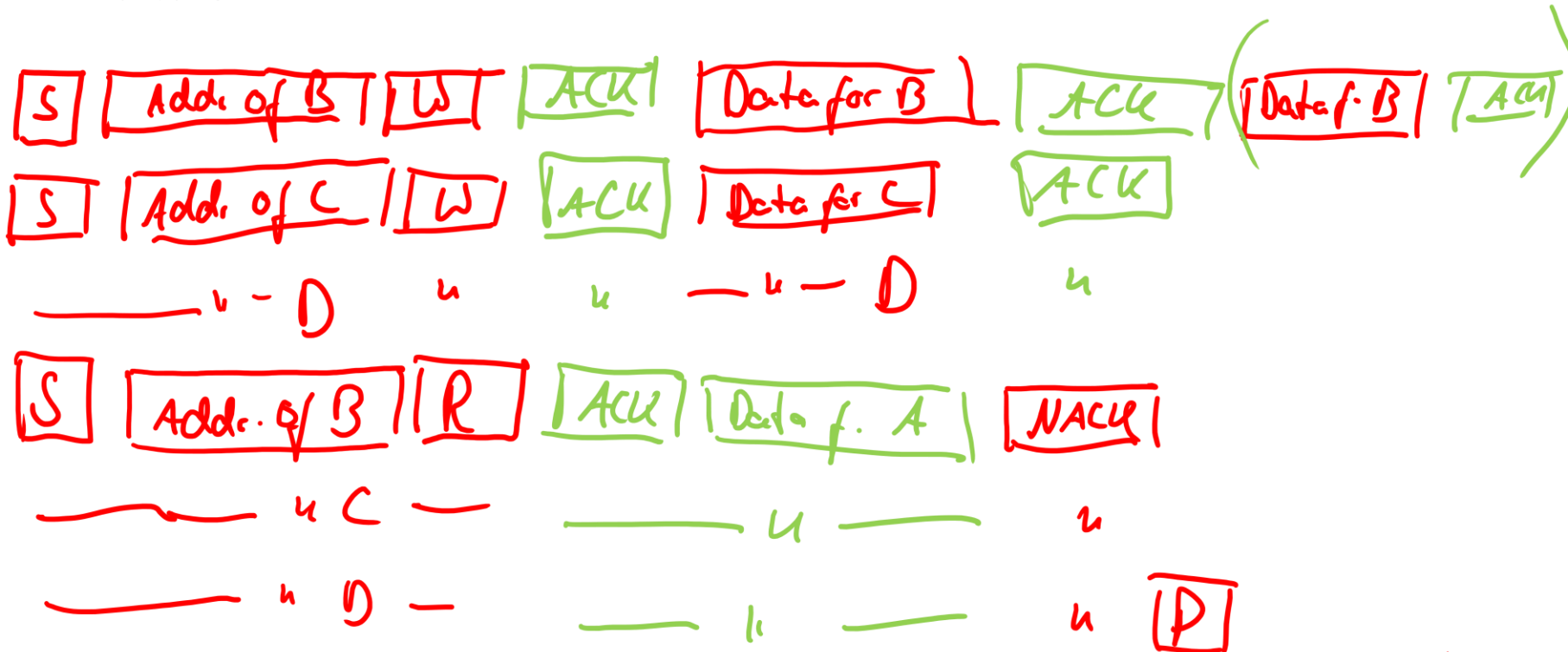
- ▶ Start-Flag S 1 bit "1"
- ▶ Stop-Flag P 1 bit "0"
- ▶ Address of X Addr. of X 7 bit
- ▶ Data for X Data for X 8 bit
- ▶ Read/Write-Flag R / W 1 bit
= 1 = 0
- ▶ ACK/NACK-Flag ACK NACK 1 bit
= 0 = 1

Task 3: d)

Master

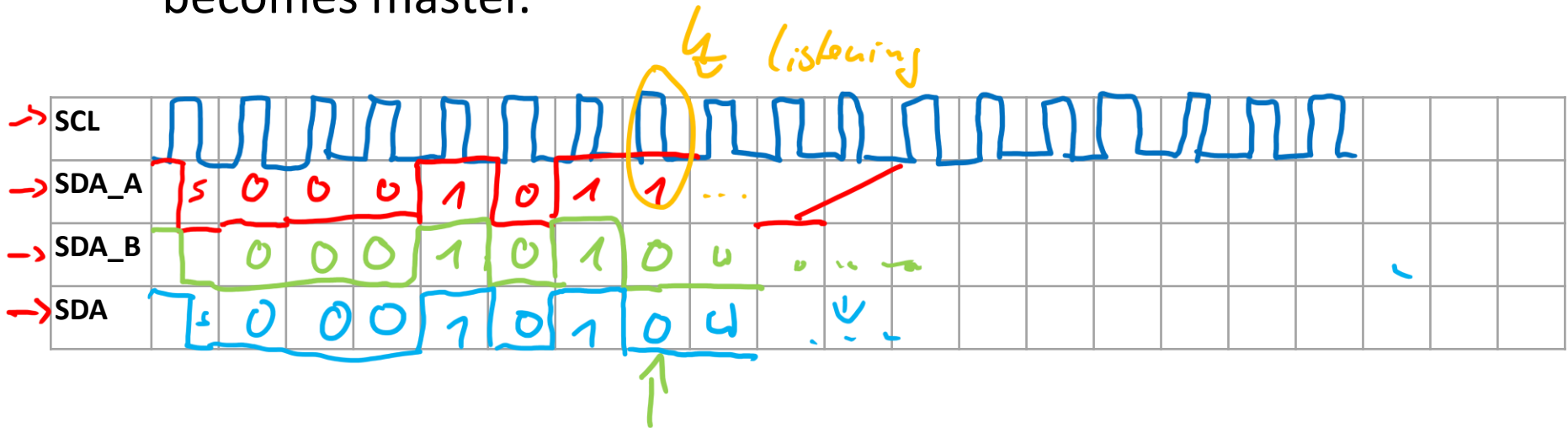
Slaves

- ▶ **A sends** data bytes to **B, C** and **D**.
- ▶ **A reads** data bytes from **B, C** and **D**.
- ▶ **Indicate** who controls the data line for each block.



Task 3: e)

- **A** (address = **0x0a**) and **B** (address = **0x0b**) want to send messages to each other at the same time. **A**'s message is **0xaa** while **B**'s message is **0xbb**. Assume their clocks are perfectly synchronous, there is no transmission delay and they start at the exact same time. Draw SCL, SDA_A, SDA_B and SDA until the first transmission is complete. **Mark** the bit that decides who becomes master.



Profibus

Task 4



Task 4

a) What is the topology of Profibus and how is medium access controlled?

- Bus topology

- Master / Slave

- Multiple Masters : Tokenbus

