September 19, 2024

EAST WEST UNIVERSITY

Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Final Examination, Summer 2024

Course: CSE360 – Computer Architecture, Section 1
Instructor: Md. Nawab Yousuf Ali, PhD, Professor, CSE Department
Full Marks: 40
Time: 1 Hour 30 Minutes

Note: There are EIGHT questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin.

1. Consider a magnetic disk drive with 6 platters. The upper surface of each platter contains 2048 tracks and lower surface of each platter contains 512 tracks. 128 sectors per track. Sector size is 8 KB. The average seeking time is 6.5 ms, the track-to-track access time is 3.5 ms, and the drive rotates at 12000 RPM.
   a) What is the capacity of the disk drive?
   b) What is the average access time?

   [CO2, C3, Mark: 2+3]

2. Convert the infix expression, (A+B)*C-(D-E)*((F+G)/H) to the postfix notation using Dijkstra's algorithm. Show the sequence of the steps in the stack. [CO2, C3, Mark: 5]

3. Convert the postfix expression **ABC*EF-/+** the infix notation. Show the sequence of steps of conversion. [CO3, C3, Mark: 5]

4. Analyze and compare zero-, one-, two-, and three- address machines by writing programs to compute the following expression for each of the four machines. [CO3, C2, Mark: 5]

$$X = (A + \frac{B}{C} - D)/(E - F * G)$$

The instructions available for use are as follows:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOV (X←Y)	MOVE (X←Y)
POP M	STORE M	ADD(X←X+Y)	ADD(X←Y+Z)
ADD	ADD M	SUB (X←X-Y)	SUB(X←Y-Z)
SUB	SUB M	MUL (X←X *Y)	MUL (X←Y*Z)
MUL	MUL M	DIV(X←X/Y)	DIV(X←Y/Z)
DIV	DIV M		

5. Compute the following expression using stack. [CO3, C3 Mark: 5]
(A*B-C) - (D + E) + F*G - H

6. A non-pipelined processor has a clock rate of 3.5 GHz and an average CPI (cycles per instruction) of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 2 GHz. What is the MIPS rate for each processor? [CO4, C Mark: 5]

Consider a 16-bit processor in which the following appears in main memory, starting at location 243:

354	Load to AC	Mode
355	8XY	
356	Next instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 387. There is also a base register that contains the value 238. The value of 7XY in location 244 may be part of the address calculation. Assume that location 535 contains the value 8F0, location 536 contains the value 810, and so on. Determine the effective addresses and the operands to be loaded for the following addressing modes.

a. Direct
b. Indirect
c. PC relative
d. Displacement
e. Register indirect

[NB: XY is the last two digits of your ID, e.g., if your ID is 2021-40-997, then the value of X is 9 and Y is 2]

8. Consider a four-stage pipeline processor. The number of cycles needed by the four instructions namely I1, I2, I3, and I4 for the stages S1, S2, S3, and S4 are given in the table below. Show the diagram of instructions executions and calculate the number of cycles needed to execute the instructions.

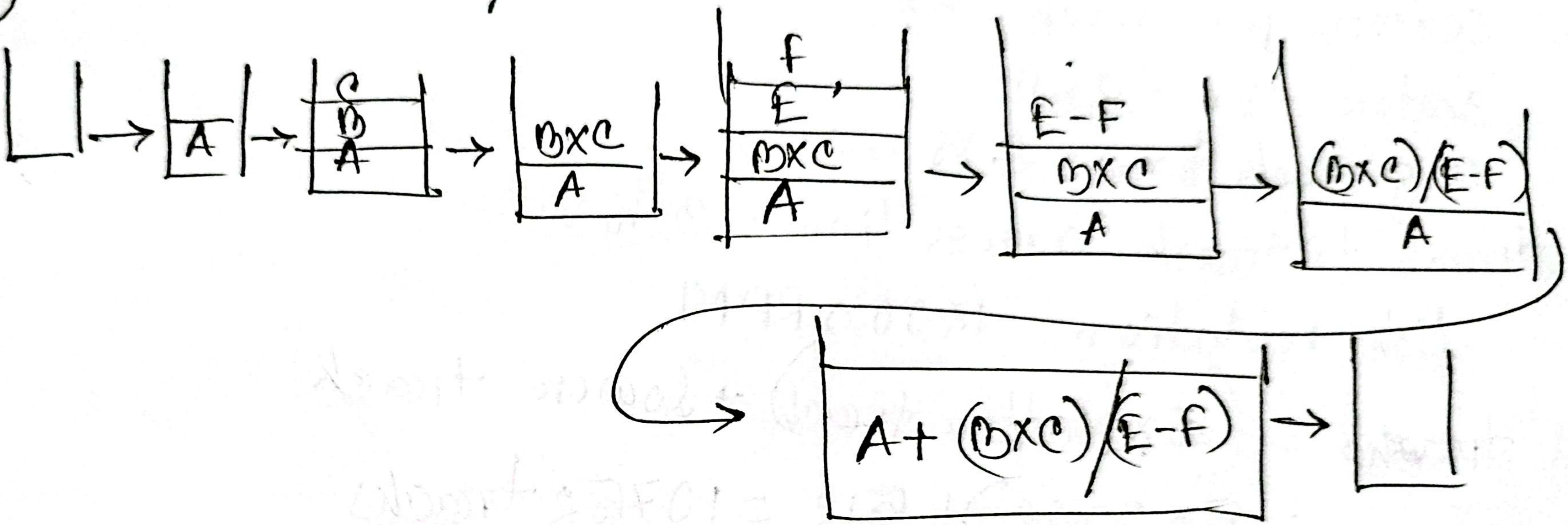
	S1	S2	S3	S4
I1	1	2	1	2
I2	2	3	2	1
I3	2	2	1	3
I4	1	3	2	1

Q7 No	Question	EA	operand
a	Direct	819	1876
b	indirect	1876	2933
c	pc relative	1175	2232
d	displacement	1057	2114
e	Reg. indirect	387	1444

= [illegible] ms

= 9 ms

3) ABC * EF - / +



(c) non pipeline, clock rate = 3.5 GHz

CPI = 4

pipeline (5 stage), clock rate = 2 GHz

$$\text{MIPS (non pipeline)} = \frac{\text{clock rate}}{\text{CPI}}$$

$$= \frac{3.5 \times 10^3 \text{ MHz}}{4}$$

$$= 875 \text{ MIPS}$$

$$\text{MIPS (pipeline)} = \frac{2 \times 10^3 \text{ MHz}}{1} = 2000$$

(3) no of platters = 6

platters in upper part = 2048 tracks

lower " = 512

sectors of per tracks = 128

sector size = 8KB = 8×1024

avg seek time = 6.5 ms

track-to-track access time = 3.5 ms

disk rotation = 12000 RPM

∴ tracks per surface = upper - lower

= 2048 - 512

= 1536

capacity of disk drive

= no of surface × ~~sectors per~~ sectors per track × track per surface ×

no of byte in each sector

= 6×1536 × 8×1024 ×128 ~~26.17~~ 33.17

= ~~72 MB~~ 9GB